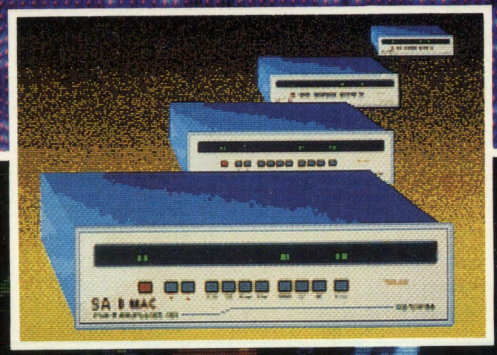
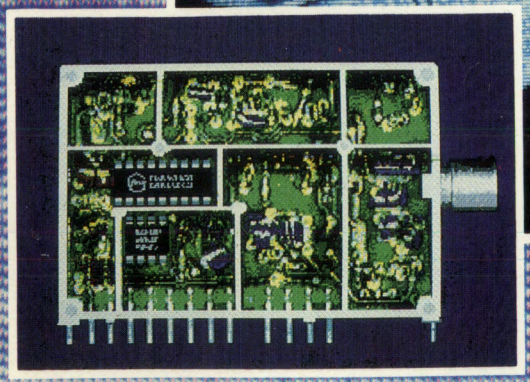
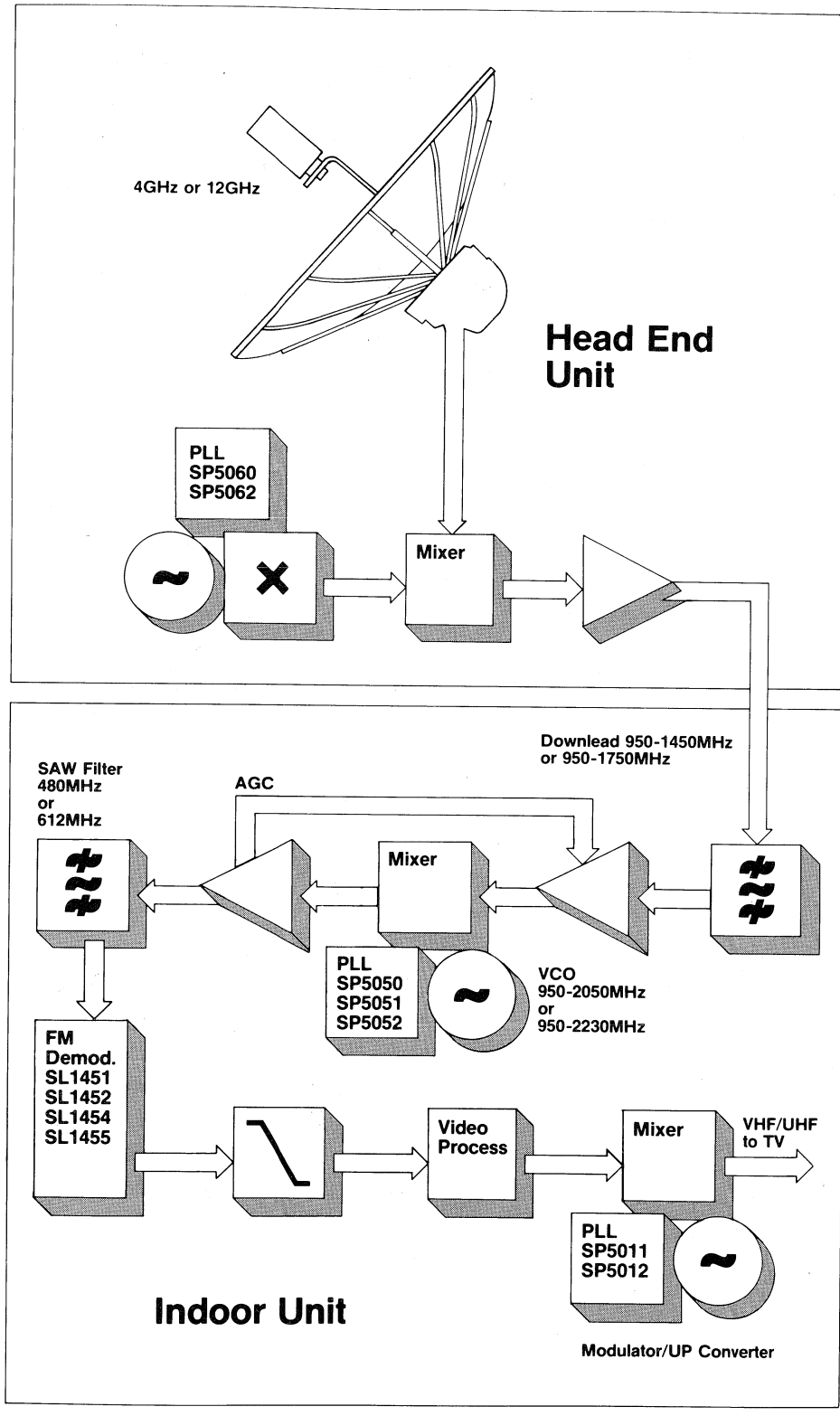
SATELLITE CABLE & TV

IC Handbook





Plessey Semiconductors



A typical satellite receiver

SATELLITE CABLE & TV
IC Handbook

Contents

PLESSEY
Semiconductors

Product index

High Speed Dividers

Type	Function	Supply Voltage (Typ.)	Frequency	Process	Page
SP4541	÷256, TTL O/P	5V	1GHz	Bipolar	156
SP4632	÷64, VHF/UHF, high sensitivity, ECL O/P	5V	1GHz	Bipolar	158
SP4633	÷64, non-self oscillating, high sensitivity ECL O/P, ESD protection on-chip	5V	1GHz	Bipolar	161
SP4653	÷256, VHF/UHF, high sensitivity, ECL O/P	5V	1GHz	Bipolar	164
SP4656	÷128 low power, low radiation, ECL O/P, ESD protection on-chip	5V	1.2GHz	Bipolar	167
SP4660	÷256, VHF/UHF, high sensitivity, ECL O/P, ESD protection on-chip	5V	1GHz	Bipolar	171
SP4665	÷64/256, switchable, high sensitivity, ECL O/P	5V	1GHz	Bipolar	174
SP4666	÷64/256, switchable, high sensitivity, with low pass filter on-chip	5V	1GHz	Bipolar	178
SP4676	÷128/136, ÷64/68, very low power, high sensitivity	5V	950MHz	Bipolar	182
SP4678	÷128/136, ÷64/68, low power, high sensitivity	5V	1.2GHz	Bipolar	186
SP4731	÷64, high sensitivity, high output ECL O/P	5V	1.3GHz	Bipolar	190
SP4740	÷256, TTL O/P	5V	1.3GHz	Bipolar	193
SP4751	÷256, high sensitivity, high output swing (ECL)	5V	1.3GHz	Bipolar	196
SP4902	÷2, low power, high sensitivity	5V	2.5GHz	Bipolar	199
SP4904	÷4, low power, high sensitivity	5V	2.5GHz	Bipolar	202
SP4908	÷8 prescaler	5V	2.5GHz	Bipolar	346
SP4914	÷128 prescaler	5V	2.5GHz	Bipolar	205
SP4916	÷512 prescaler	5V	2.5GHz	Bipolar	208
SP4982	÷8192 prescaler	5V	2.5GHz	Bipolar	349

Satellite TV Receiver Circuits

Type	Function	Supply Voltage (Typ.)	IF Frequency (MHz)	Process	Page
SL1451	PLL demodulator with threshold extension	8.2V	380-700	Bipolar	140
SL1452	Wideband FM detector	5V	300-1000	Bipolar	142
SL1454	Wideband FM detector for low IF	5V	70-150	Bipolar	146
SL1455	Quadrature detector with threshold extension	5V	380-700	Bipolar	150
SL1488	Video buffer amp with AGC and black level clamp	12V/56mA		Bipolar	343

Television IF

Type	Function	Process	Page
SL1430	Ultra linear pre-amplifier, 22dB gain 50MHz, differential output optimised for driving surface acoustic wave filters	Bipolar	133
SL1431	Similar to SL1430 but internally derived NPN tuner AGC signal output	Bipolar	136
SL1432	AS SL1431 but for PNP tuners	Bipolar	136

TV/Cable/Satellite Tuner PLL Circuits

Type	Function	Supply Voltage (Typ.)	Frequency	Process	Page
SP5000	Single chip frequency synthesiser with 3 wire control	5V	102MHz	Bipolar	211
SP5003[1]	I²C bus-controlled frequency synthesiser	5V	1300MHz	Bipolar	216
SP5004[1]	I²C bus-controlled frequency synthesiser	5V	1300MHz	Bipolar	219
SP5011	8-channel cable/satellite PLL up/down converter for USA	5V	See data	Bipolar	222
SP5012	8-channel cable/satellite PLL up/down converter for UK and Europe	5V	See data	Bipolar	222
SP5050	PLL tuning controller for satellite receivers, 3 wire serial data bus	5V	1.8GHz	Bipolar	226
SP5051	PLL tuning controller for satellite receivers, 3 wire serial data bus	5V	2.0GHz	Bipolar	226
SP5052	PLL tuning controller for satellite receivers, 3 wire serial data bus	5V	2.3GHz	Bipolar	231
SP5060	Fixed modulus frequency synthesiser for satellite receivers	5V	2.0GHz	Bipolar	236
SP5062	Fixed modulus frequency synthesiser for satellite receivers	5V	2.3GHz	Bipolar	240
SP5510[1]	Bi-directional I²C bus-controlled synthesiser	5V	1.3GHz	Bipolar	245
TDA5030A	VHF mixer oscillator/VHF IF preamplifier/ IF amplifier	5V	70-470MHz	Bipolar	253

1. Purchase of Plessey's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the systems conform to the I²C Standard Specification as defined by Philips.

Product index (continued)

DBS TV Signal Decoding (MAC)

Type	Function	Supply Voltage (Typ.)	Process	Page
MV1710	MAC video circuit	5V	CMOS	72
MV1720	MAC control circuit	5V	CMOS	75
MV1730	MAC sound circuit	5V	CMOS	79
MV1740	MAC Teletext decoder	5V	CMOS	83
MV95308	8-bit 30MHz video DAC	5V	CMOS	120
SP973T8	30MHz TTL/CMOS 8-bit flash ADC	12V	Bipolar	249

Teletext

Type	Function	Character Set	Supply	Process	Page
MR9710	Data acquisition	-	+5V,15mA/+12V,72mA	NMOS	46
MR9735-002	625-line video generator	English	+5V,15mA/+12V,72mA	NMOS	52
MR9735-003	625-line video generator	German	+5V,15mA/+12V,72mA	NMOS	52
MR9735-004	625-line video generator	Swedish/Finnish	+5V,15mA/+12V,72mA	NMOS	52
MR9735-005	625-line video generator	Danish	+5V,15mA/+12V,72mA	NMOS	52
MR9735-006	625-line video generator	Italian	+5V,15mA/+12V,72mA	NMOS	52
MV1812	Teletext data acquisition (all packets)	-	+5V,10mA	CMOS	87
MV1815	625-line single chip Teletext decoder	Fourteen languages (see Note 1 below)	+5V	CMOS	99
MV1830	Teletext Data Buffer	-	+5V,10mA	CMOS	111
MV1826	Single chip VPS decoder	-	-0.3V to 7V	CMOS	339
SL9100	Teletext data slicer and clock regenerator	-	+5V,44mA/+12V,11mA	Bipolar	152
ZNA134J	625/525 line sync. pulse generator	-	+5V,100mA	Bipolar	256
ZNA234E	TV pattern generator	-	+5V,135mA	Bipolar	264

1. English, German, Swedish/Finnish, Italian, French (Belgian), Spanish, Czech, Polish, Rumanian, Hungarian, Turkish, Serbo Croat, Danish, American.

Display/Touch Switching

Type	Function	Supply Voltage	Supply Current	Process	Page
CT2200	32-number LED display driver, drives two 7-segment common anode LED arrays, 5-bit binary input; 1-32 display O/P, sinking 20mA per segment; 13 direct drive O/Ps	5V	5mA	NMOS	13
ML237B	Negative 6-channel touch switch for Neon	33V	5mA	PMOS	16
ML238B	Positive 8-channel touch switch for LED/Neon	33V	6mA	PMOS	18
ML239B	Negative 8-channel touch switch for Neon	33V	6mA	PMOS	21

Remote Control

Type	Function	Supply Voltage (Typ.)	Supply Current (Typ.)	Process	Page
ML920[1]	Receiver: 20 programmes, 3 DAC, 6 other controls	16V	8mA	PMOS	23
ML922[1]	Receiver: 10 programmes, 3 DAC, 3 other controls	16V	8mA	PMOS	26
ML923[1]	Receiver: 16 channel selection codes with single analog output	16V	6mA	PMOS	29
ML924[1]	Receiver: 5 digital outputs programmed by six control lines. Three selectable output modes	16V	6mA	PMOS	33
ML926[1]	Receiver: 4 bit binary, 16 code momentary output	15V	4mA	PMOS	40
ML927[1]	Receiver: As ML926 but operates from second set of 16 codes	15V	4mA	PMOS	40
ML928[1]	Receiver: 4 bit binary 16 code latched output	15V	4mA	PMOS	42
ML929[1]	Receiver: As ML928 but operates from second set of 16 codes	15V	4mA	PMOS	42
MV500	32-code PPM transmitter, three switchable data rates	+3V to 10.5V	500μA	CMOS	64
MV601	32-code PPM receiver to complement MV500	5V	1.4mA	CMOS	67
SL486	Infra-red preamplifier	10V	6mA	Bipolar	124
SL490B	32-code PPM transmitter, infra-red, ultrasonic or radio	9V	6mA	Bipolar	129

1. Old product - not recommended for new designs.

Video Graphics

Type	Function	Supply Voltage	Process	Page
ZN454E	Triple 4-bit video DAC, can provide 4096-colour palette with resolution up to 1024 x 1280 pixels. 100MHz update rate	+5V,-5V	Bipolar	275

Product list - alpha numeric

DBS TV Signal Decoding ICs

The First Chip-Set for a Multi-Standard MAC Decoder

INNOVATION THROUGH COOPERATION

Developing a DBS TV transmission decoder to handle signals encoded in accordance with any of the present European MAC packet standards (CMAC, DMAC and D2MAC), and to also descramble and decrypt was quite a challenge. It took the combined resources and expertise of Nordic VLSI, Plessey Semiconductors, and Philips. Nordic VLSI, with their unrivalled experience of MAC decoding designed the decoder and developed most of its 1.5 micron CMOS circuitry. Plessey Semiconductors will manufacture three of the full custom VLSI CMOS ASICs at the heart of the decoder and also supply a Teletext full custom VLSI CMOS ASIC.

This unique cooperation has led to the availability of the first-ever chip set for constructing an advanced multi-standard MAC decoder which can enormously increase the market applicability of TV sets through its most innovative feature — multi-standard operation that meets all the requirements of today's European satellite TV market.

MAIN FUNCTIONS OF THE MULTI-STANDARD MAC DECODER

The main part of the decoder comprises four full custom VLSI CMOS ASICs from Plessey Semiconductors; MAC control circuit MV1720, MAC video circuit MV1710, MAC sound circuit MV1730 and MAC Teletext circuit MV1740. These are complemented by several Philips ICs; a MAC Analog (MACAN) circuit TDA8734 which performs analog signal processing and includes functions such as data slicing, clock recovery and video clamping, a microcomputer comprising a microprocessor (e.g. the 16-bit 68070) plus RAM and ROM, and a conditional access control module incorporating a PCB80C51 8-bit microcontroller.

Standard Plessey/Philips ICs are also used in video D to A and A to D conversion: MV95308/TDA8702 in the DAC, SP973T8 in the ADC. D to A conversion of the stereo sound signal (dual DAC TDA1541A and SAA7220 for filtering the sound signal.

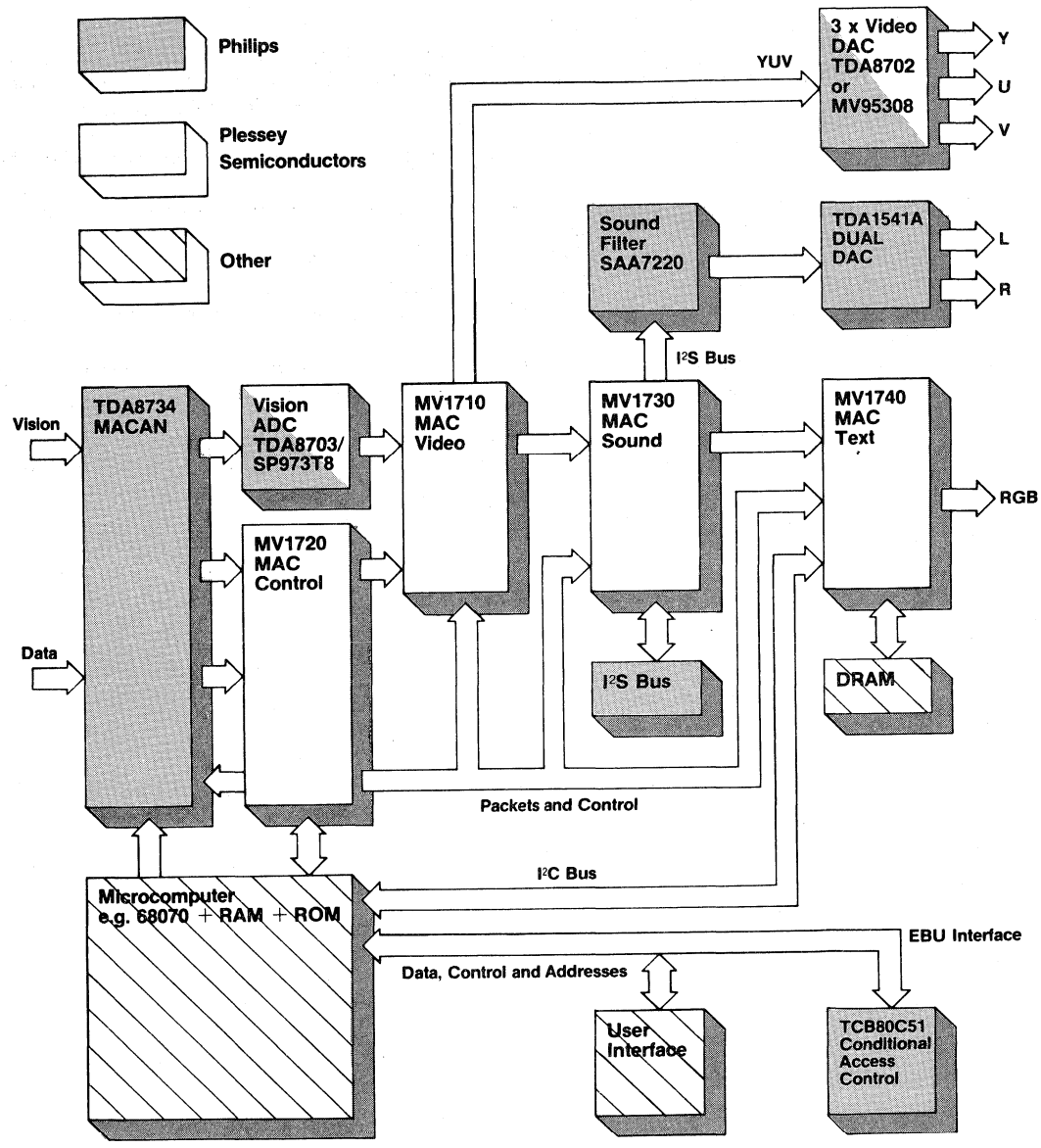
The conditional access control module handles both over-air and/or local addressing for decryption. It can either be detachable or can form a permanent part of the TV set. In either case, it's connected to the microcomputer via the EBU interface.

The user interface, in its minimum form, consists of pushbuttons and LEDs. A more advanced version would incorporate a keyboard for controlling menus and service identification data displayed on the screen of the TV set.

AN INNOVATIVE DESIGN THAT'S ALSO FUTURE-PROOF

In addition to being able to handle all of today's European DBS TV transmission standards, the architecture of this advanced multi-standard MAC decoder also facilitates extensions and will be able to accommodate the requirements of additional satellite TV services that may be defined in the future.

ICs for Television



Block diagram of the multi-standard MAC decoder incorporating ICs from Philips and Plessey Semiconductors.

UNIQUE FEATURES OF A DECODER BUILT WITH THE CHIP SET

- Implements the full CMAC/DMAC/D2MAC packet standard
- Can handle the standard MAC format for picture plus up to eight mono or four stereo sound channels
- Is compatible with any TV set architecture
- A conditional access control feature allows descrambling and decryption of sound and vision signals (Pay TV) and Teletext. This feature can handle several broadcasts simultaneously and meets the requirements of the new Part 6 of the EBU specification. Entitlements can be addressed over-air, via a smart-card or via a keyboard
- Single- and double-cut conditional access descrambling of the vision signal as specified by the EBU
- Very flexible packet multiplexing allows full-field sound/data transfer of up to 50 high quality sound channels at a rate of nearly 20Mbit/s
- All packet addresses in the selected data bursts are Golay decoded
- The configuration data can be changed without disrupting the service
- Can handle Teletext in accordance with the EBU specification during the frame interval or in the packet multiplex
- A second vision signal aspect ratio and decompression ratio will allow future high-definition TV (aspect ratio 16:9) to be accommodated whilst retaining compatibility with present standards (aspect ratio 4:3)
- Linear or companded sound signals can be decoded
- Processing of 1st and 2nd level error protection of the sound signal, including error concealment
- Digital mixing allows simultaneous processing of stereo sound and commentary channels
- Sound quality comparable with compact disc
- The decoder is software controlled

Technical Data

PLESSEY
Semiconductors

CT2200

5-BIT BINARY TO 13-SEGMENT DECODER/DRIVER

The CT2200 is an N-channel MOS integrated circuit, designed to directly drive two 7-segment LEDs to display the numbers 1 to 32, with leading zeros suppressed. The circuit is ideal for applications such as the programme number display of a television receiver. The display is controlled by a 5-bit binary input port, weighted so that the number shown (1-32) is one more than the binary input (0-31) to avoid programme 0. The 5 lines can come from a remote control receiver or from any other source of continuous 5-bit data.

Common anode LEDs can be driven directly with a current limiting resistor in series with each output (see Fig.5) or by using some other form of brightness control (see Fig.6). By driving each segment individually the interference problems associated with multiplexed displays are avoided.

A blanking input is provided so that the display can be turned off or can be made to flash with an external pulsed signal.

Only 13 lines are needed for two 7-segment displays because segment Tf is never lit for the numbers 1 to 32 and so does not need to be decoded and driven. Segment identification is shown in Fig.2.

The 13 outputs of the output encoder drive the gates of large output transistors to give two states: OFF and SINK CURRENT; as there can be up to 12 outputs on at once, each sinking 20mA, four 0V pins are provided to reliably carry this current. **ALL FOUR PINS (3, 7, 18, 22) MUST BE CONNECTED TO 0V.**

The number of segments required for each character is shown in Fig.3.

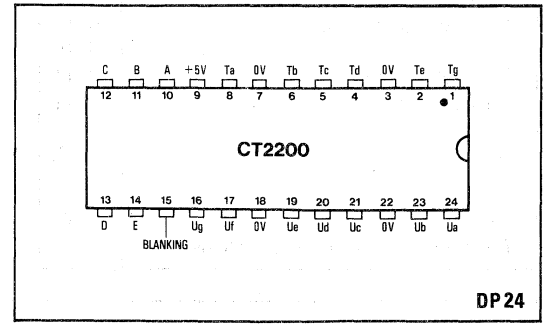


Fig.1 Pin connections - top view

FEATURES

- Direct Segment Drive — Non-Multiplexed
- 5V Supply
- Blanking Input
- Leading Zero Suppressed
- Minimum Segment Pattern per Character
- 20mA Drive per Segment
- 5-Bit Binary Input

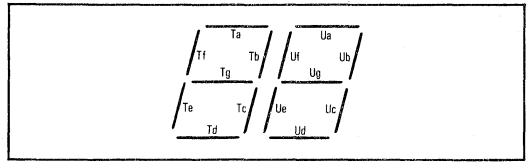


Fig.2 Segment identification

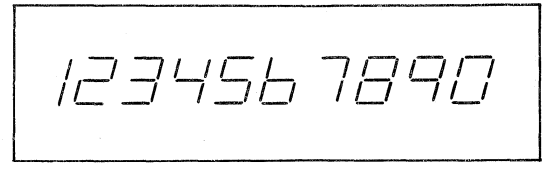


Fig.3 Character representation

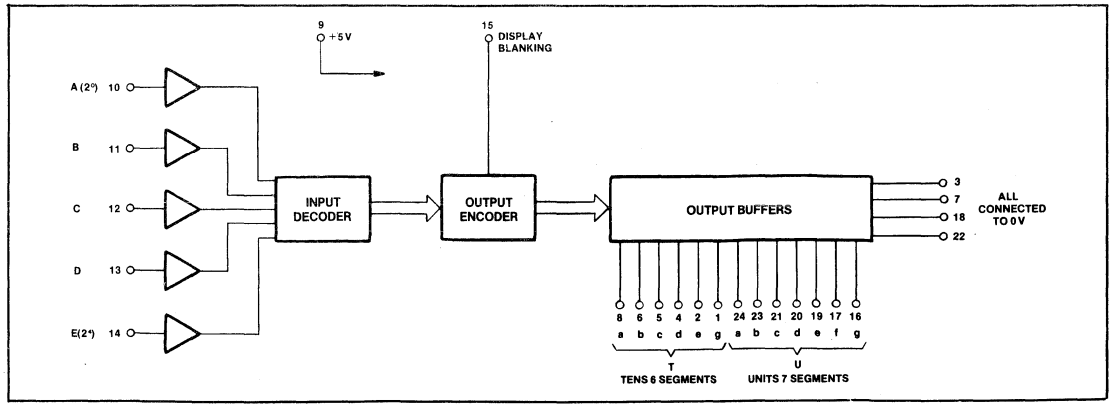


Fig.4 Block diagram

ELECTRICAL CHARACTERISTICS (see Fig.5)

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{DD} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	9	4.5	5	5.5	V	
Supply current	9			5	mA	
Input voltage high	10-14	4			V	
Input voltage low	10-14			0.8	V	
Leakage current	10-14			10	μA	$V_{IN} = +5V$
Capacitance	10-14			10	pF	
Output voltage	1, 2, 4-6, 8, 16, 17, 19-21 23, 24			1	V	Sinking 20mA
Recommended series resistor (if used)			120		Ω	

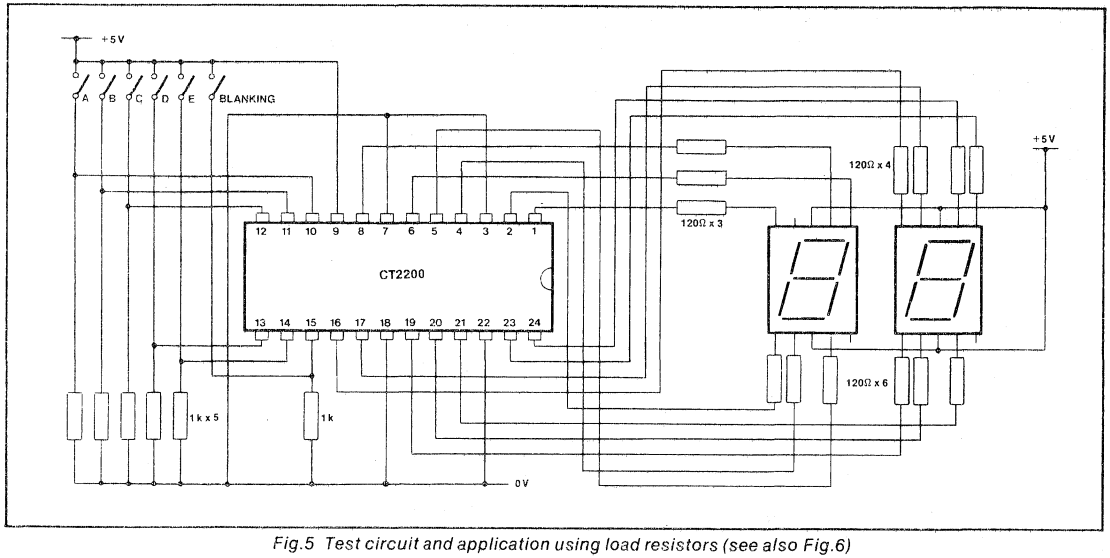


Fig.5 Test circuit and application using load resistors (see also Fig.6)

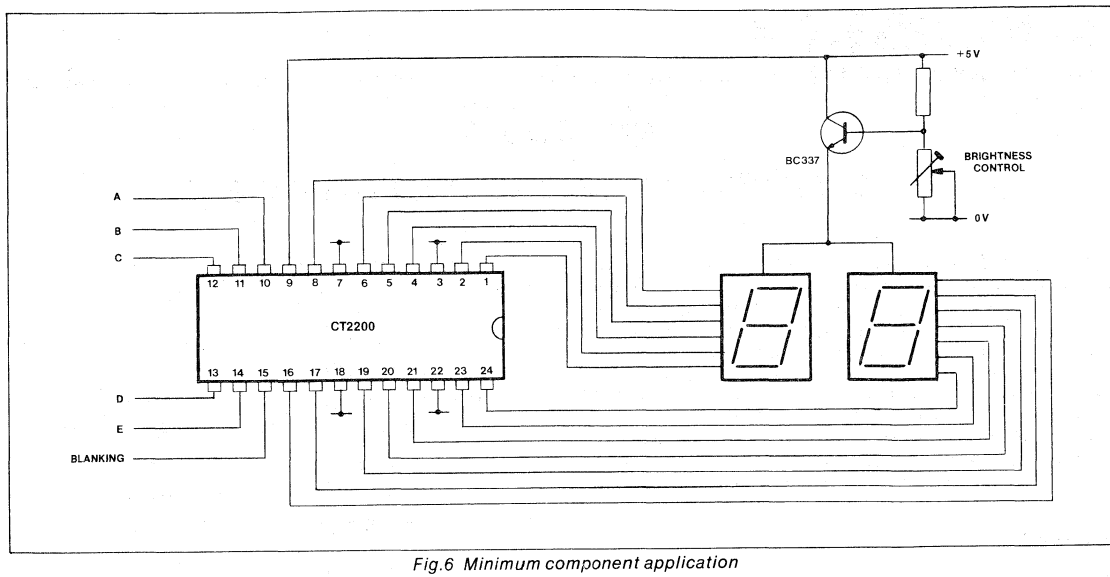


Fig.6 Minimum component application

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Input or output voltage	+7V
Output current	30mA
Ambient operating temperature	−10°C to +65°C
Storage temperature	−55°C to +125°C

PLESSEY
Semiconductors

ML237B

6-CHANNEL TOUCH CONTROL INTERFACE

The ML237B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates - replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML237B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

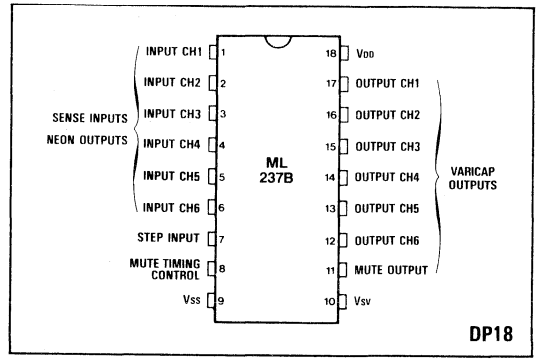


Fig.1 Pin connections - top view

FEATURES

- 6-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selected Channel 1 on Power-up
- Channels Are Selected With a Negative (or Earth) Input

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-10° C to +85° C
Supply, V_{SS}-V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

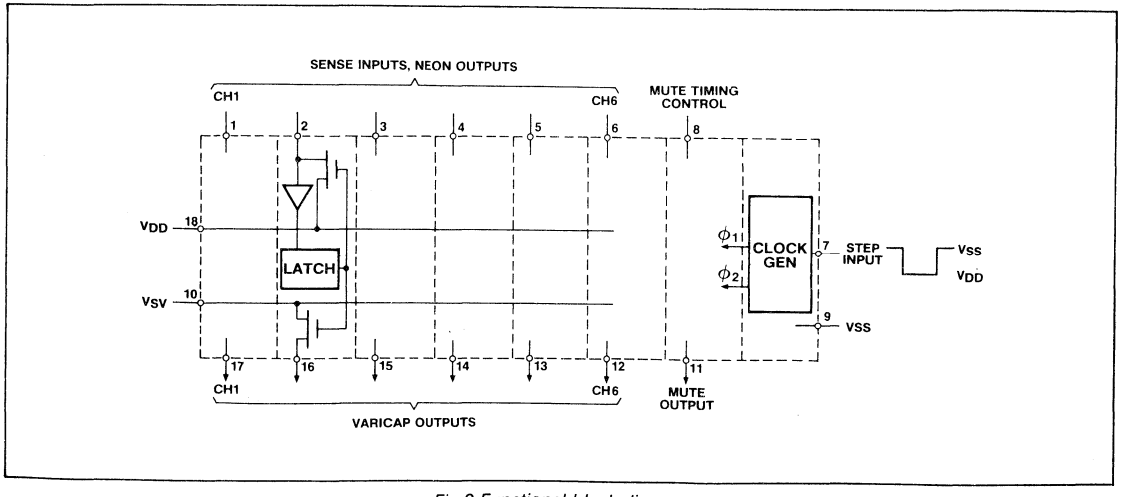


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current			1	μA	$V_{IN} = V_{SS}$
Output leakage			1	μA	V_{OUT} = 0
Mute switch O/P leakage			10	μA	V_{OUT} = 0
Supply current		5	8	mA	
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
Step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
Mute switch R_{ON}		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1000	μA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68 μF
Step pulse level	0		V_{SS} −29	V	

NOTES

The mute timing can be increased by using a higher value of capacitor (C_M)

Touch plate selection:

Tm ≃ Cm x 0.6ms/nF

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_S

Stepping selection:

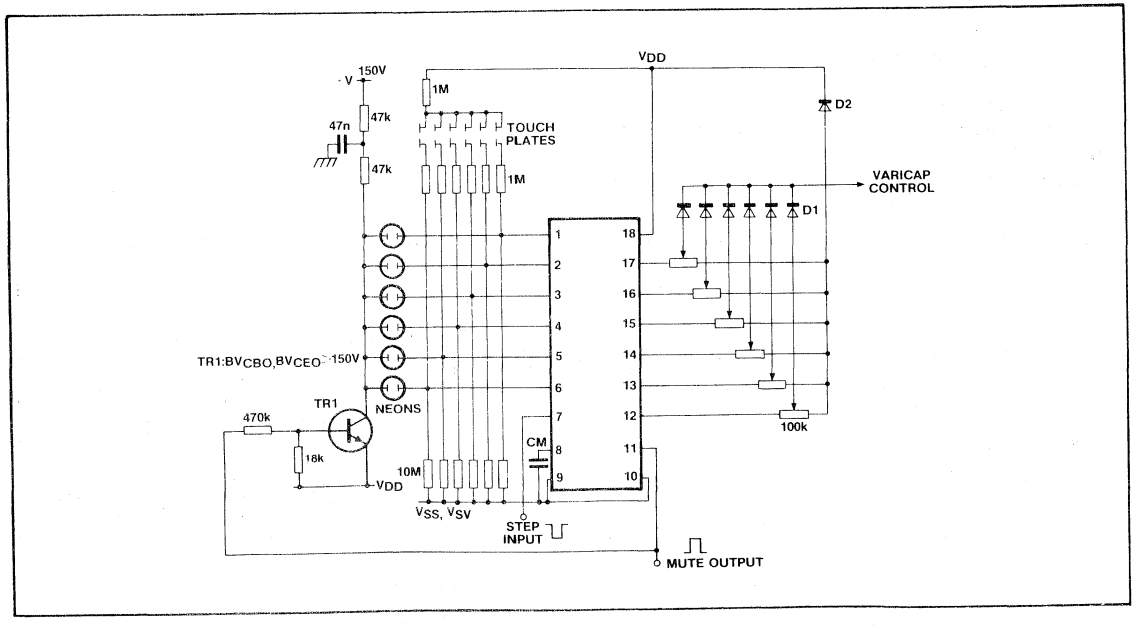


Fig. 3 Typical applications using neons as channel indicators

PLESSEY
Semiconductors

ML238B

8-CHANNEL TOUCH CONTROL INTERFACE

The ML238B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates - replacing conventional mechanical push-buttons for channel selection. Neons or LEDs may be used to indicate the selected channel, while the latched output of the ML238B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel to advance by one.

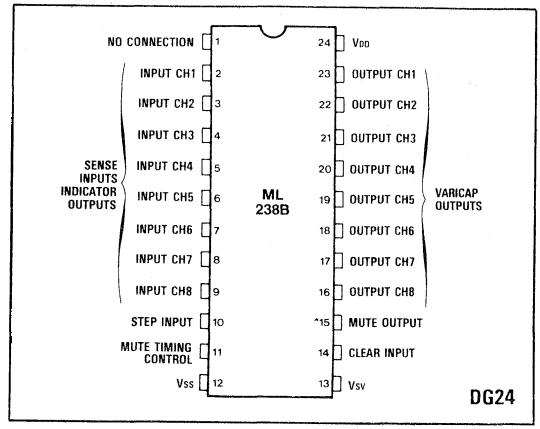


Fig.1 Pin connections - top view

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10°C to +65°C
Storage temperature	-10°C to +85°C
Supply, V_{SS}-V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

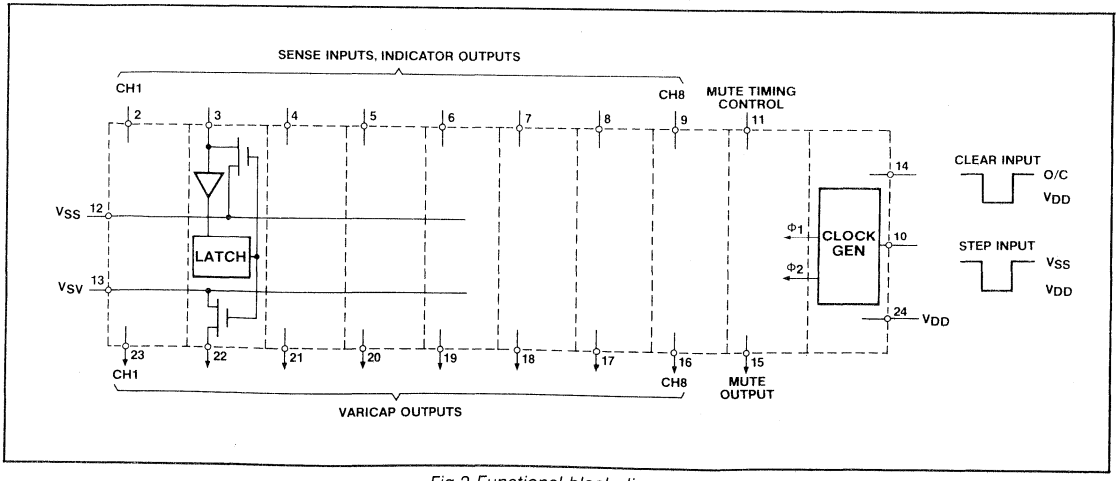


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

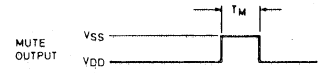
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Output leakage			1	µA	V_{out} = 0
Supply current		6	9	mA	
Input current			1	µA	V_{in} = 0V
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
R_{ON} of indicator switch		180	300	Ω	I_{OUT} = 10mA
I/P threshold	0.4	0.5	0.6	V_{SS}	
Step pulse level	0		V_{SS} –29	V	
T_S step pulse width	0.2			ms	>.0 5 Tm
Clear pulse level	0		V_{SS} –29	V	
Clear pulse width	0.2			ms	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
T_m mute timing		400		ms	Cm = 0.68µF
Step I/P current	10		1000	µA	V_{in} = 0
Mute O/P leakage			10	µA	V_{OUT} = 0

NOTES:

The mute timing can be increased by using a higher value of capacitor (C_m) (See Fig.4).

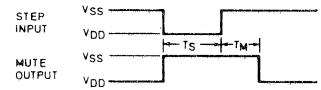
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

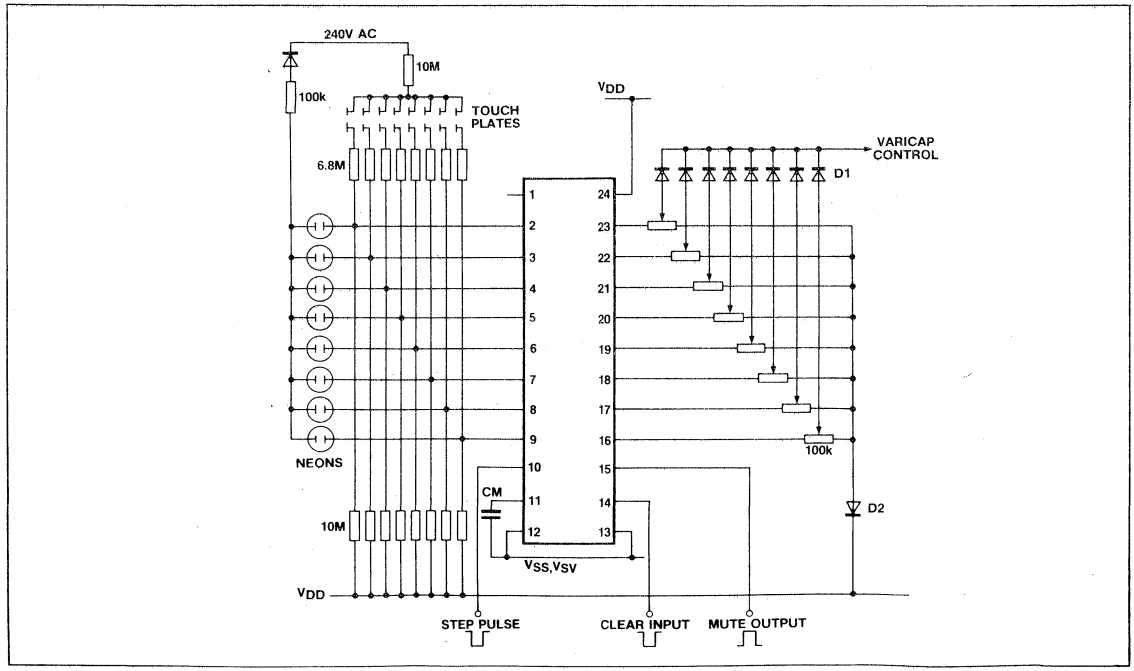


Fig.3 Typical applications using neons as channel indications

APPLICATION NOTES

Application using LEDs as channel indicators

In applications where the use of mains is not desired channel selection can be made by using the +30V V_{SS} supply as a compromise but at the expense of reduced input sensitivity. In this case LEDs can be used as channel indicators.
The 1.2kΩ and 820Ω resistors limit the LED current to 10mA, whilst the diode ensures less than 1μA leakage when the LED is reverse biased. It is desirable to have a 1MΩ resistor between the touch plates and the input as a safeguard against static.
On selection of a channel, the potential divider chain comprising the 1MΩ resistor, the finger resistance and the 10MΩ resistor sets the threshold voltage on the input pin. When the channel is selected the IC provides a current source to the LED.

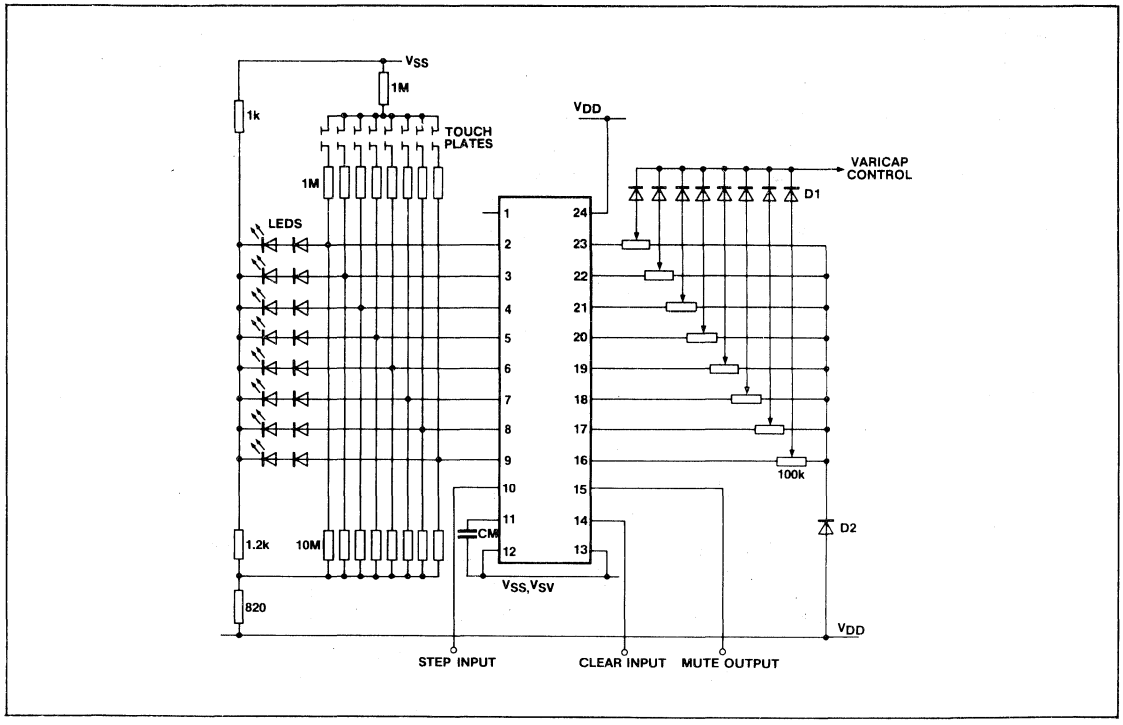


Fig. 4 Low voltage, improved sensitivity using LED indicators

PLESSEY
Semiconductors

ML239B

8 – CHANNEL TOUCH CONTROL INTERFACE

The ML239B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML239B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1
- Channels are Selected with a Negative (or Earth) Input

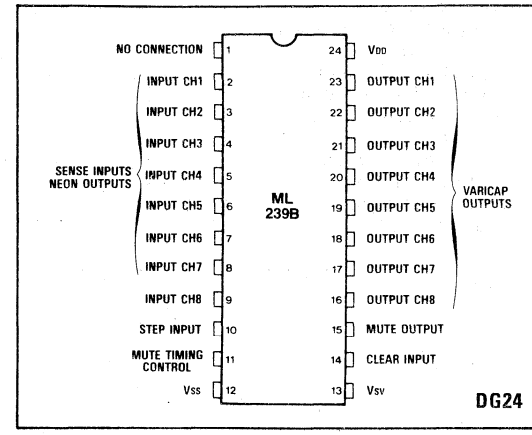


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
V_{SS}–V_{DD} supply	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

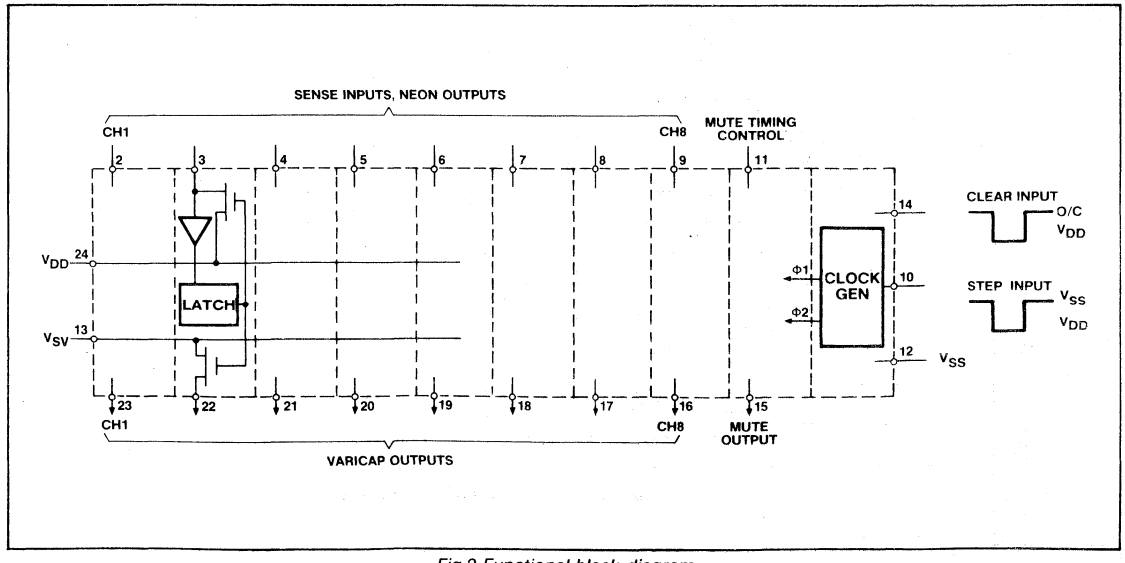


Fig.2 Functional block diagram

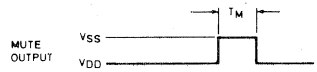
ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Step, clear pulse level	0		V_{SS} –29	V	
Input current			1	µA	V_{IN} = V_{SS}
Output leakage			1	µA	V_{OUT} = 0
Mute switch O/P leakage			10	µA	V_{OUT} = 0
Supply current		6	9	mA	
R_{ON} of varicap switch		50	1000	Ω	I_{OUT} = 10mA
Clear step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1	mA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68µF

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m)

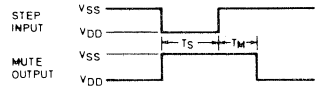
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

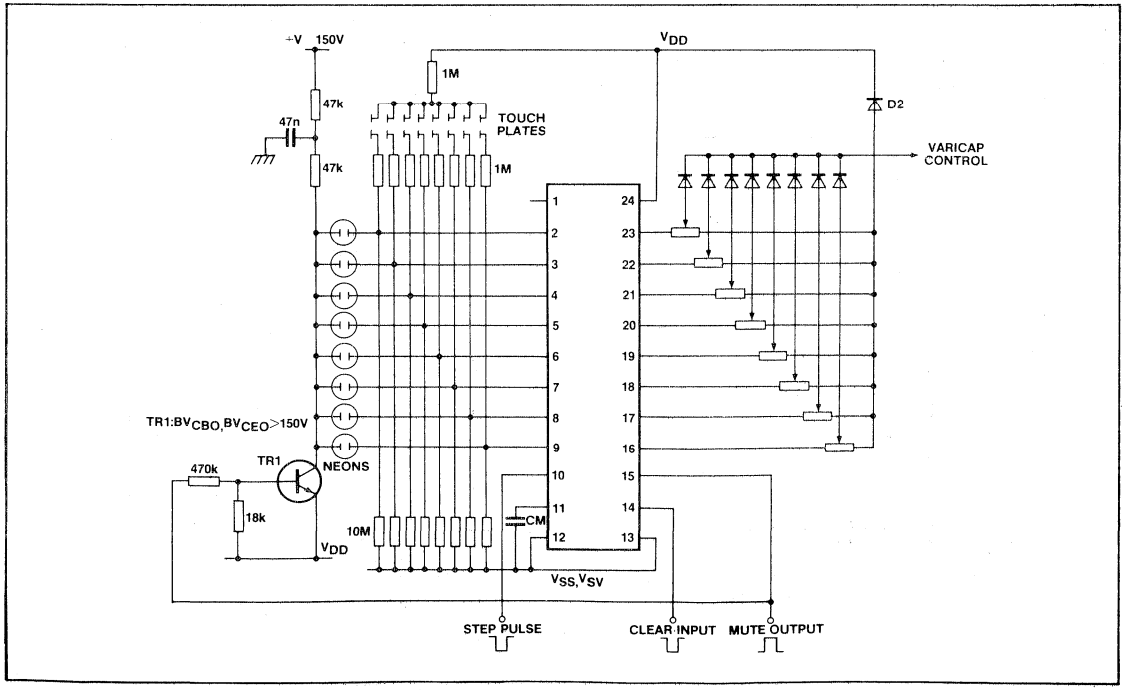


Fig. 3 Typical applications using neons as channel indications

PLESSEY
Semiconductors

ML920

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML920 decodes the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 20 programme memory or one of three D/A converters.

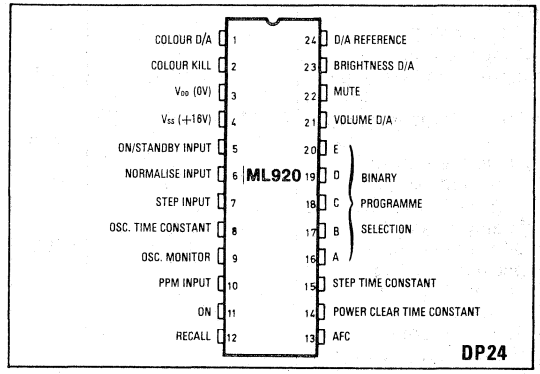


Fig.1 Pin connections (top view)

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 5 bit binary, 20 programmes
- Analogue controls: 3 static current mirror converters, 32 step with normalise level
- Other outputs: On, Recall Display, AFC, Mute, Colour Kill, Oscillator Monitor
- Local inputs: On/Standby, Step, Normalise

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used with Ultrasonic or Infra-Red System
- Up to 20 Programmes with Latched Binary Output
- 3 D/A Outputs with Normalise Level at 3/8 of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Colour Kill, Recall etc.

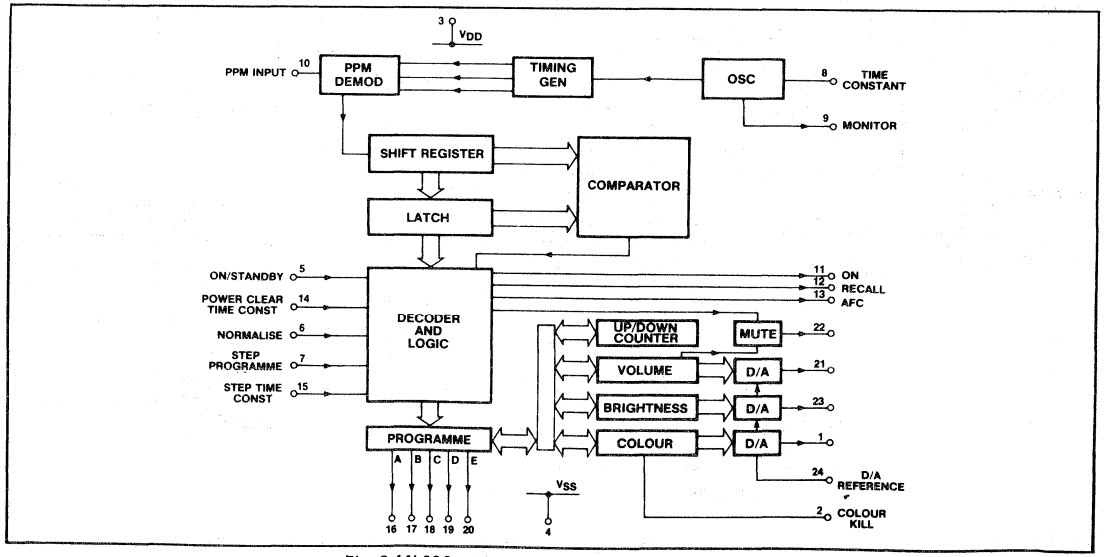


Fig. 2 ML920 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):

V_{SS} = 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5, 6, 7,	−1		0	V	
low		V_{DD}		V_{DD}+3.5	V	
Output logic level high	2, 11-13, 16-20, 22	−1		0	V	50k to V_{DD}
low		V_{DD}		V_{DD}+0.5	V	50k to V_{DD}
Analogue output current range (pins 1, 21, 23)	1, 21, 23	0		$\frac{31}{8}$	I_{REF}	3.9k to V_{DD}
Analogue step size	1, 21, 23	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{REF}	$V_{out} < V_{DD}$ +5V
D/A reference, I_{REF}	24	−250	−345	−455	μA	33k to V_{DD}
Oscillator timing	9		1.5k		Hz	C = 22n, R=100k See note 1
Power clear time constant	14		400		ms	C = 4.7μ R=100k
Step time constant	15		1		s	C = 470n R = 3.3M
Monitor output 'high'	9	−1		0	V	Internal load
'low'		V_{DD}		V_{DD}+0.5	V	provided
PPM input level high		-1		0	V	
PPM input level low	10	V_{DD}		-6	V	
PPM input pulse width		1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$

Note 1. Rosc (Pin 8) is 56k-156kΩ, 2fmon (Pin 9) = $f_{osc} \simeq \frac{1}{0.15CR}$ ±20%

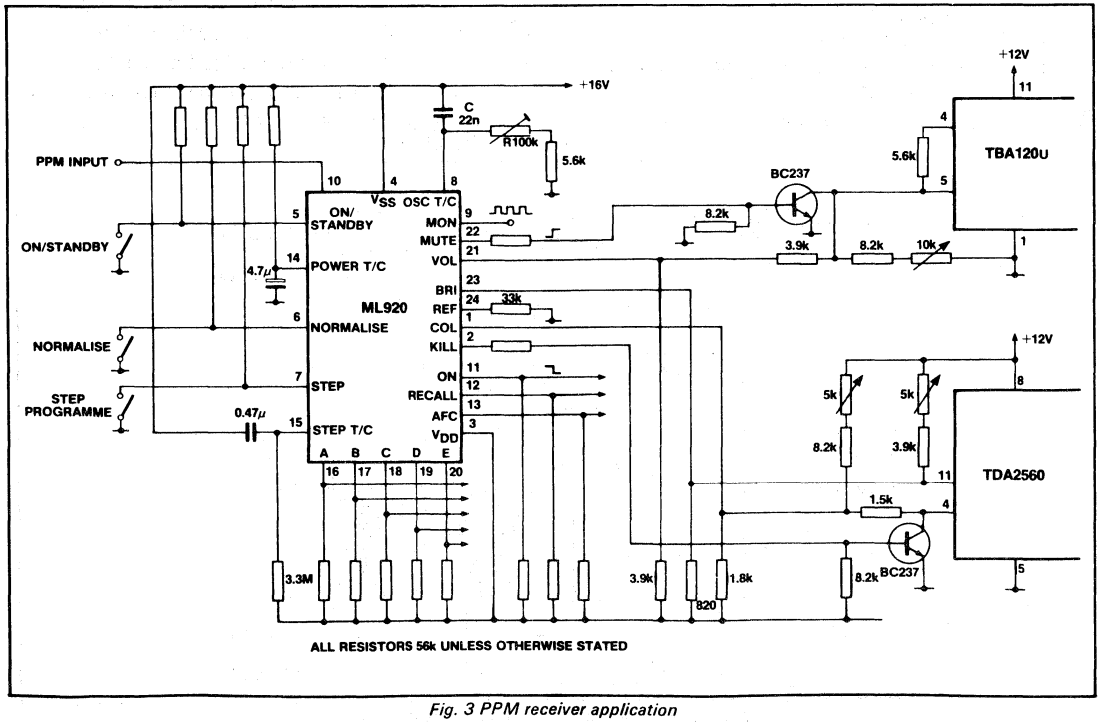


Fig. 3 PPM receiver application

PIN FUNCTIONS

Negative Logic: 0 is 0V (V_{SS}), 1 is −17V (V_{DD})

1, 21, 23. Colour, Volume, Brightness
These three outputs are from three 5 bit current mirror D/A converters. They are referenced to the current drawn from pin 24, I_{ref}, and give 32 steps, $I_{ref}/8$ per step, from 0 to 31/8 I_{ref}. The outputs will be set to 12/8 I_{ref} by the NORMALISE input, the normalise code from the transmitter, or when the ON output goes to a 1.

2. Colour kill
This output gives a logic 0 when the COLOUR D/A output is zero.

3. V_{DD}
−17V power supply

4. V_{SS}
0V power supply

5. On/Standby input
A 1 on this pin will toggle pin 11 (ON O/P), generate RECALL and AFC, normalise VOLUME, BRIGHTNESS and COLOUR, reset MUTE and set channel code 00000.

6. Normalise input
A 1 will normalise the VOLUME, BRIGHTNESS and COLOUR outputs. A RECALL signal is generated and MUTE is reset.

7. Channel step
The channel code will step up by 1 as long as this pin is held at logic 1. The time period between steps is defined by an RC constant attached to pin 15. On reaching 20 the next step returns to 1. On output is set to ON, and AFC is generated. If the TV goes from Standby to ON, RECALL is generated and VOLUME, BRIGHTNESS and COLOUR are normalised. If VOLUME is not 0, MUTE is reset.

8. Oscillator time constant
An RC time constant is formed for the clock timing by connecting external components, one resistor and one capacitor, to this pin. Adjusted so that period of output on pin 9 is 1/20 of 0 interval of incoming PPM.

9. Oscillator monitor
This output is a division of two of the oscillator, and and is available for testing and setting purpose.

10. PPM I/P
The output of the front end amplifier is connected here such that the signal is in the form of positive pulses separated by time periods whose length define the data. With no signal, PPM input is at a low level.

11. On O/P
Open drain output. Logic 1 denotes TV set ON: Logic 0 TV set standby. Set to 1 when channel number changes. Set to 0 by power clear or by transmitter selected Standby. Toggle to opposite state by manual ON/STANDBY control.

12. Recall O/P
Open drain output. A 1 may be used to trigger an on-screen display. A static output is generated by the manual controls ON/STANDBY and NORMALISE.
A pulse is generated by any channel change if the circuit switches to ON at the time, and by RECALL and NORMALISE commands from the transmitter.

13. AFC O/P
Open drain output. Logic 1 can inhibit the tuner AFC.
A static output is generated bymanual ON/STANDBY control. A pulse is generated by any channel number change.

14. Power clear
A capacitor and resistor connected here define the time delay for the power clear circuit, which normalises all D–A outputs etc.

15. Channel step time constant
An R–C time constant defines the time period between increments of the channel number when stepping.

16 –20. Channel outputs
5 Outputs encode 20 channel numbers in binary code

EDCBA
Channel 1 is 00000
Channel 20 is 10011

E is first and A is last in the PPM pulse train.
Channel 1 is set when ON goes to a 1

21. Volume.
See Pin 1

22. Mute O/P
This will change state (toggle) on reception of a mute command and VOLUME O/P is zero MUTE O/P is held at 0.

23. Brightness
See Pin 1

24. D/A Reference
A current drain I_{ref}, set by a single external resistor will set the nominal step of the D/A outputs to $I_{ref}/8$.

Transmitter code	Function
EDCBA	
00000	Programme 1
00001	Programme 2
00010	Programme 3
00011	Programme 4
00100	Programme 5
00101	Programme 6
00110	Programme 7
00111	Programme 8
01000	Programme 9
01001	Programme 10
01010	Programme 11
01011	Programme 12
01100	Programme 13
01101	Programme 14
01110	Programme 15
01111	Programme 16
10000	Programme 17
10001	Programme 18
10010	Programme 19
10011	Programme 20
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute
11010	Recall
11011	Normalise
11100	Colour −
11101	Programme Step −
11110	Volume −
11111	Brightness −

Table 1 Basic 32 command set

ABSOLUTE MAXIMUM RATINGS (Vss = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Operating voltage range, V_{DD}	−14V to −18V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

ML922

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML922 decodes the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 10 programme memory or one of three D/A converters.

The receiver timing may be set by adjusting the oscillator time constant to give 40 periods at pin 6 equal to a 0 interval on the received PPM input.

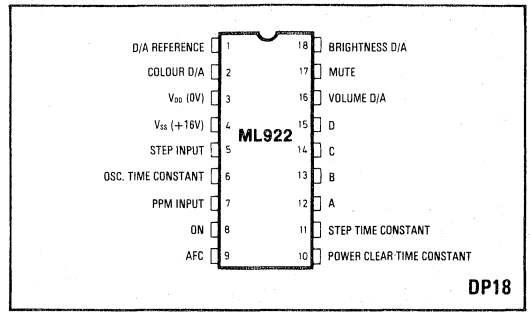


Fig.1 Pin connections - top view

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 10 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Etc.

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 4 bit binary, 10 programmes
- Other outputs: On, AFC, Mute
- Local inputs: Programme step

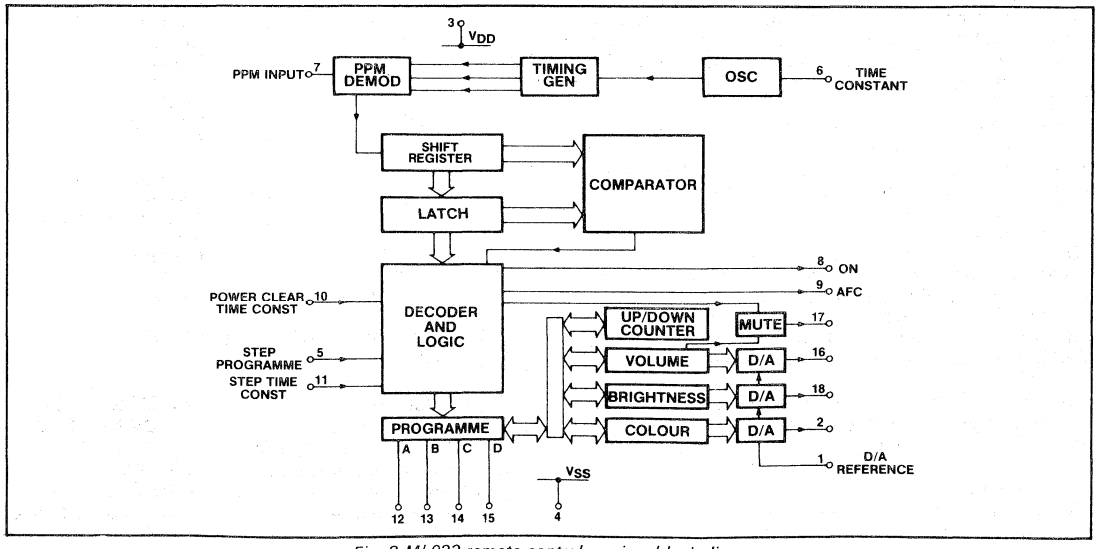


Fig. 2 ML922 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):

V_{SS} = 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5	−1		0	V	
low		V_{DD}		V_{DD} + 3.5	V	
Output logic level high	8, 9, 12-15, 17	−1		0	V	50k to V_{DD}
low		V_{DD}		V_{DD} + 0.5	V	50k to V_{DD}
Analogue output current range	2, 16, 18	0		$\frac{31}{8}$	I_{ref}	3.9k to V_{DD}
Analogue step size	2, 16, 18	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{ref}	$V_{out} < V_{DD}$ +5V
D/A reference, I_{REF}	1	−250	−345	−455	µA	33k to V_{DD}
Oscillator timing	6		3		kHz	C = 22n, R = 100k See note 1
Power clear time constant	10		400		ms	C = 4.7µ R = 100k
Step time constant	11		2		s	C = 470n R = 3.3M
PPM input level high	7	−1		0	V	
PPM input level low	7	V_{DD}		−6	V	
PPM input pulse width	7	1		$22T_{OSC}$	µs	

Note 1. $R_{osc.}$ (pin 6) is 56k-156kΩ. $f_{osc.} \simeq \frac{1}{0.15CR}$ ±20%

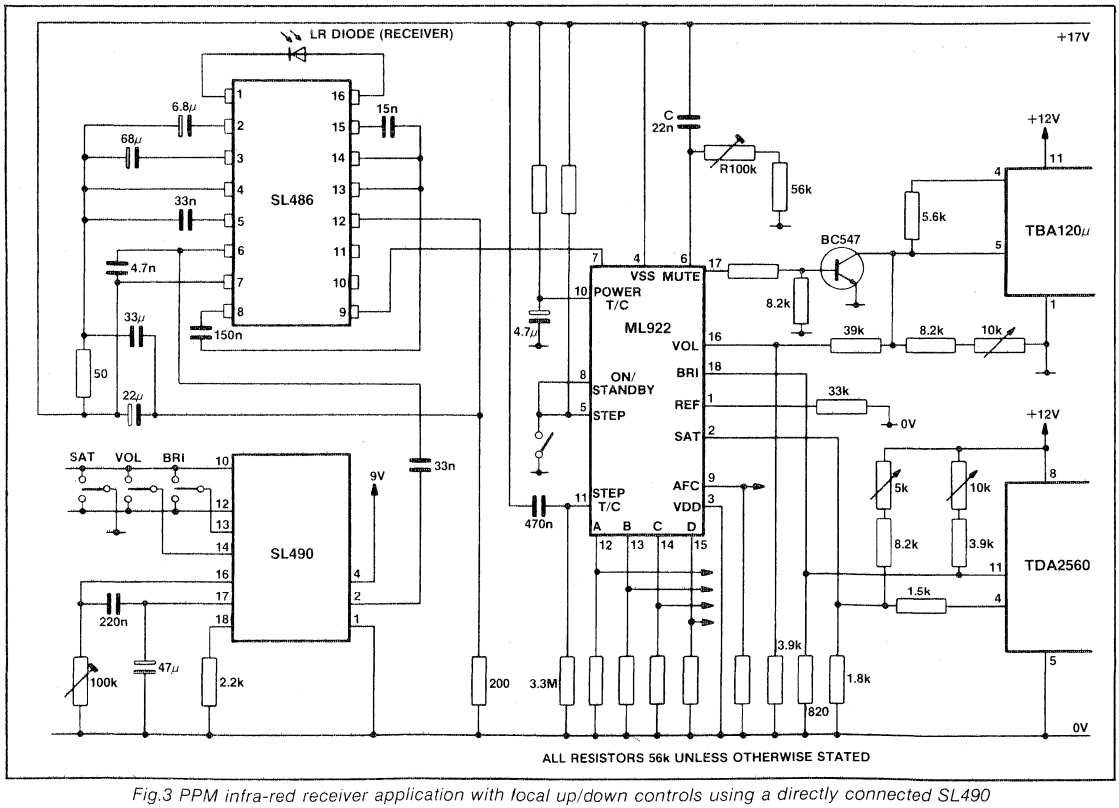


Fig.3 PPM infra-red receiver application with local up/down controls using a directly connected SL490

Note: Pin descriptions same as ML920.

Transmitter code	Function
EDCBA	
0000X	Programme 1
0001X	Programme 2
0010X	Programme 3
0011X	Programme 4
0100X	Programme 5
0101X	Programme 6
0110X	Programme 7
0111X	Programme 8
1000X	Programme 9
1001X	Programme 10
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute (Analogue 2)
11011	Normalise
11100	Colour —
11101	Programme Step —
11110	Volume —
11111	Brightness —

Table 1 Basic 21 command set for ML922

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

ML923

REMOTE CONTROL RECEIVER

The ML923 is an MOS/LSI monolithic integrated circuit for use as a receiver of remote control signals for television control. It accepts 24 of the 32 codes transmitted by the SL490 transmitter circuit in the Pulse Position Modulation (PPM) method of coding.

FEATURES

- 16 Channel Selection Codes
- Single Analogue Output
- Mute Output (Toggle)
- On-set Controls — Channel Step, ON, Reset
- Normalise to $\frac{3}{8}$ of Max Output on Analogue Output
- Outputs Provide Control of ON/STANDBY, Analogue Mute, and AFC Defeat
- Choice of Power-Up Function:
  a) Power Up to Standby State, Switch to ON State by Local or Remote Command and STANDBY by Remote Command.
  b) Power Up to ON State, Switch OFF with Solenoid Operated Mains Switch by Local or Remote Command.

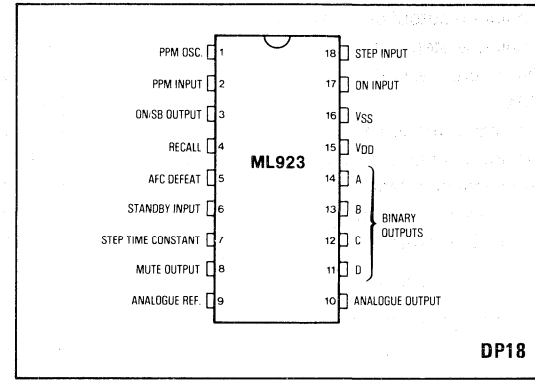


Fig.1 Pin connections (top view)

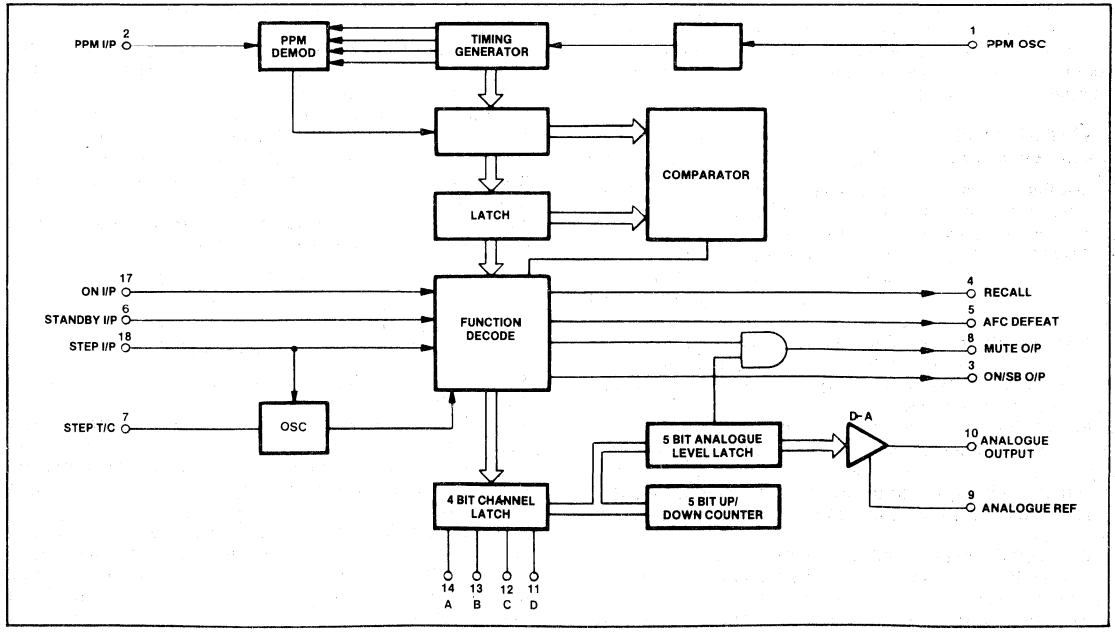


Fig.2 ML923 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -16V$

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1	14		18	V	
Supply current	1		6		mA	
Input logic level high	6, 17, 18	-1		0	V	
Input logic level low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	3, 4, 11, 14	-1.5		0V	V	50k to V_{DD}
Output logic level low	8	V_{DD}		$V_{DD}+0.5$	V	
Analogue output current range	10	0		$\frac{31}{8}$	1 Ref	3.9k to V_{DD}
Analogue step size	10	0	$\frac{1}{8}$	$\frac{1}{4}$	1 Ref	$V_{out} < V_{DD}+5V$
D/A reference, I ref	9	-250	-345	-455	mA	33kΩ to V_{DD}
PPM		15		150k	Hz	Typical TC
Oscillator frequency	1		3k		Hz	C = 22nF R = 100kΩ
On input or standby input time constant for power on	6 or 17	250		500	ms	
Step time constant	7		1		s	C = 470nF R = 3.3MΩ
PPM input level high	2	-1		0	V	
PPM input level low	2	V_{DD}		-6	V	
PPM input pulse width	2	1		22 T_{osc}	μs	$T = \frac{1}{f_{osc}}$

Note 1 R_{osc} (pin 5) is 56k-156kΩ $f_{osc} \simeq \frac{1}{0.15CR}$ ±20%

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillater may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same operating area).

Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code. Channel step time period is derived from an external time constant.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator Time Constant An RC Time Constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to the pin; the signal must consist of a normal low level with pulses to high level, corresponding to the PPM pulse from the transmitter.

3. ON/SB Output Open drain output. Logic '0' denotes onset. Logic '1' standby set. Set to '0' when channel number changes, and by ON input at logic '0', set to '1' by standby input or by transmitter selected OFF.

4. Recall O/P Open drain output. A '0' may be used to trigger an on-screen display. A '0' is output during an input at pin 17, ON input. The pulse to logic '0' is generated by any channel change if circuit switches to ON from Standby, and by recall and normalise commands from the remote transmitter.

5. AFC O/P Open drain output. A logic '0' can inhibit tuner AFC. A static output is generated by manual ON control. A pulse is generated by any channel number change.

6. Standby Input A logic '0' will select standby state and normalise the analogue output to 3/8 maximum and select programme 1. An RC time constant may be connected to select standby at power ON.

7. Channel Step Time Constant An RC time constant defines the time period between increments of the channel number when stepping.

8. MUTE Output This will change state (toggle) on receptin of a Mute command or will remain at logic '1' if the D-A output is zero. The output is reset by any channel change command.

9. Analogue Reference A current drain attached to this input will define the current step of the D-A output. The current is equal to 8 output current steps.

10. Analogue Output The output of a current mirror D-A convertor provides a current source of between 0mA and 1.3mA. It is variable in 32 steps, UP or DOWN. It is normalised to 3/8 maximum value by the ON/SB input, and by normalise command from the transmitter.

11, 12, 13, 14. Channel Selection Outputs These outputs encode the 16 channels in binary code.

	A	B	C	D
Channel 1	0	0	0	0
Channel 16	1	1	1	1

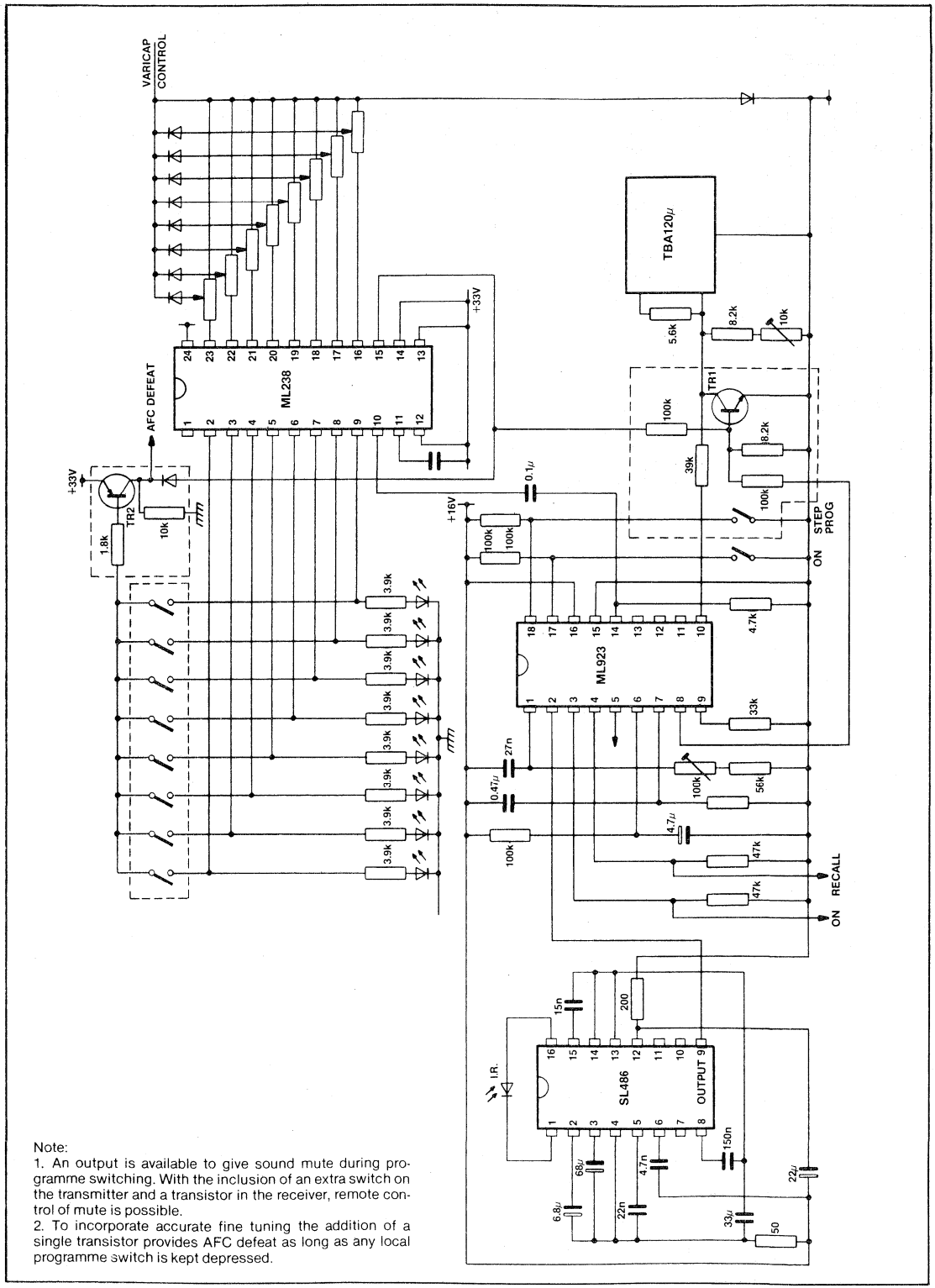
Set to channel 1 on set switch ON.

15. V_{DD} -14V to -18V power supply

16. V_{SS} 0V (Ground)

17. ON I/P A logic '0' will switch the ON/SB output to ON (logic '0'). Channel 1 is selected and analogue output is normalised to 3/8 maximum. An RC time constant may be connected to select set ON at power on. The AFC defeat signal is generated and Mute is reset.

18. Step Input The channel code will step up by 1 as long as the pin is held at logic '0'. The time period between steps is defined by an RC constant on pin 7. When the channel code reaches 16 it will go to 1 next step. A step input will set ON/SB output to ON and normalise the analogue output. Mute is reset if analogue = 0.



Note:
1. An output is available to give sound mute during programme switching. With the inclusion of an extra switch on the transmitter and a transistor in the receiver, remote control of mute is possible.
2. To incorporate accurate fine tuning the addition of a single transistor provides AFC defeat as long as any local programme switch is kept depressed.

Fig.3 Receiver application

CODE					FUNCTION
E	D	C	B	A	
0	0	0	0	0	Channel 1
0	0	0	0	1	Channel 2
0	0	0	1	0	Channel 3
0	0	0	1	1	Channel 4
0	0	1	0	0	Channel 5
0	0	1	0	1	Channel 6
0	0	1	1	0	Channel 7
0	0	1	1	1	Channel 8
0	1	0	0	0	Channel 9
0	1	0	0	1	Channel 10
0	1	0	1	0	Channel 11
0	1	0	1	1	Channel 12
0	1	1	0	0	Channel 13
0	1	1	0	1	Channel 14
0	1	1	1	0	Channel 15
0	1	1	1	1	Channel 16
1	0	1	0	1	Channel Step +
1	0	1	0	0	Analogue +
1	1	0	1	0	Recall
1	1	0	0	1	Mute (Toggle)
1	1	0	1	1	Normalise
1	1	0	0	0	OFF
1	1	1	0	1	Channel Step-
1	1	1	0	0	Analogue-

Table 1 Command set

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to -25V
Voltage at any input	+0.3V to -25V
Maximum power dissipation	600mW
Operating temperature range	-10° C to +65° C
Storage temperature range	-55° C to +125° C

PLESSEY
Semiconductors

ML924

REMOTE CONTROL RECEIVER

The ML924 is an MOS/LSI integrated circuit for use as a receiver of remote control signals generated by the SL490B transmitter circuit, using PPM (Pulse Position Modulation) encoding technique. The receiver has 5 digital outputs whose response to PPM codes may be programmed by six control lines. It has a handshake interface which provides communication with microprocessors and computers.

FEATURES

- 5 Open Drain Outputs with Enable
- Handshake or Interrupt Microprocessor and Computer Interface Signals
- On-Chip Oscillator
- 6 Control Lines to Programme Output Response
- 3 Selectable Output Modes

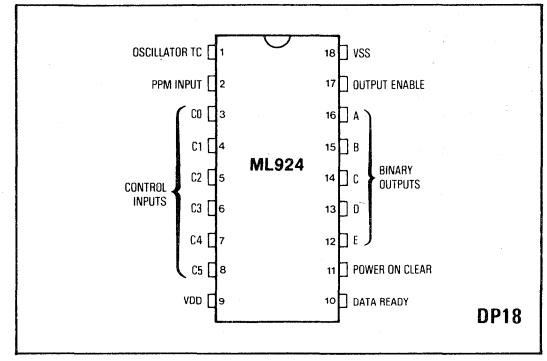


Fig.1 Pin connections (top view)

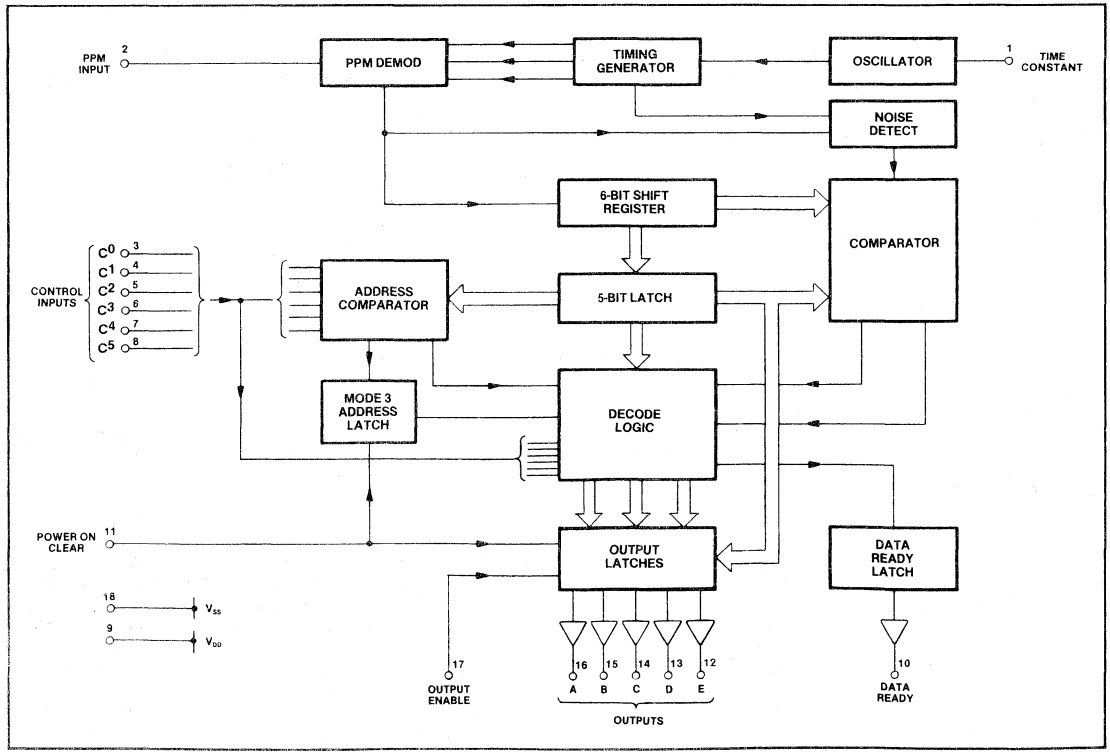


Fig.2 ML924 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
VSS = 0V; VDD = - 16V; T_{amb} = + 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	9	12		18	V	
Supply current	9		6		mA	
Input logic level high ('1')	3-8,17	-1		0	V	
Input logic level low ('0')		V_{DD}		V_{DD} + 3.5	V	
Output logic level high ('1')	10,12-16	-1		0V		
Output logic level low ('0')		V_{DD}		V_{DD} + 0.5	V	50k to V_{DD}
Oscillator frequency	1	15	3k	150k	Hz	Typical TC: C = 22nF, R = 100kΩ
PPM input level high	2	-1		0V		
PPM input level low		V_{DD}		-6V		
PPM input pulse width	2	1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$
Power clear time constant	11	1	400		ms	

NOTE

Rosc (Pin 1) is 56 kΩ to 156 kΩ, fosc $\simeq \frac{1}{0.15\,CR}$ ±20%

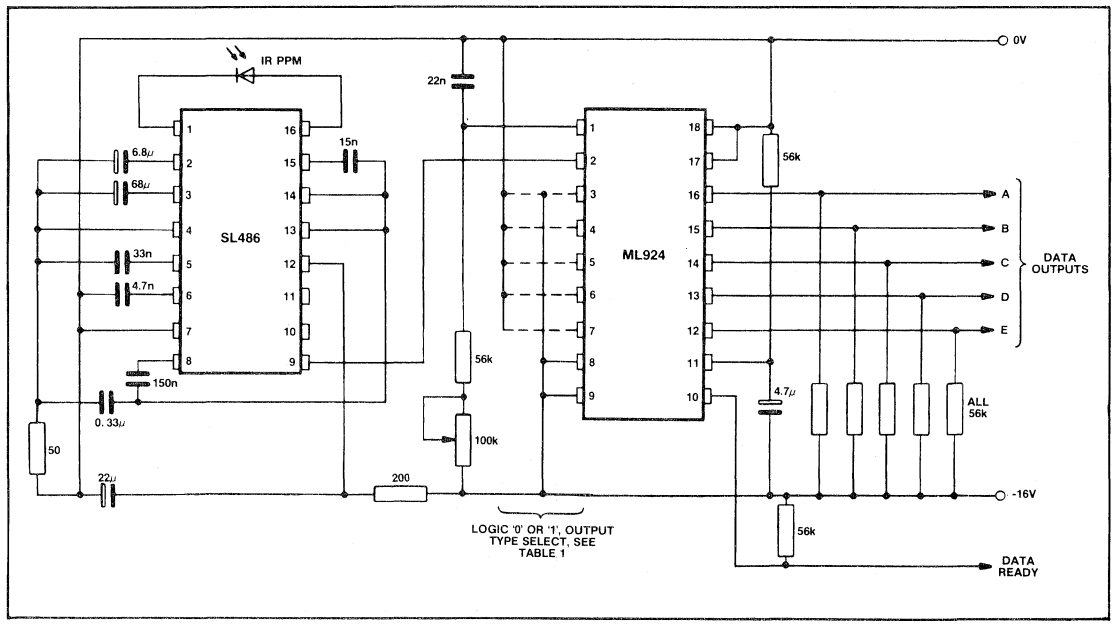


Fig.3 Application for receiving 32 codes, from SL490 transmitter, in mode 1

PIN FUNCTIONS

Positive Logic: Logic '1' = Vss, 0V Logic '0' = V_{DD}, -16V

1. Oscillator TC An RC time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to this pin; the signal must consist of a normal low level with pulses to the high state.

3-8. Control Word C_0 to C_5 Six control bits form the control word which programs the response of the five outputs (see Table 1).

9. V_{DD} -12V to -18V power supply.

10. Data Ready Open drain output. An output of logic '1' indicates the reception of a valid PPM word. It will remain at logic '1' for the duration of transmission.

11. Power Clear A capacitor and resistor connected to this pin define the time delay for the Power Clear Circuit.

12-16. Outputs E-A Open drain outputs which respond to the PPM input as defined in Table 1.

17. Output Enable A logic '1' will enable outputs A to E. A logic '0' will turn all outputs off.

18. Vss 0V (Ground).

APPLICATION NOTES

By setting combinations of logic states on the six control line inputs, C_0 to C_5 (pins 3 to 8), the outputs E to A (pins 12 to 16) on the ML924, can respond to the PPM input word (as shown in Fig.4) in three modes, detailed below:

Control Mode 1

Each output E to A directly corresponds to bits e to a in the PPM word. The type of output available can be either latched (LA) or momentary (M) according to the combination of C_0 to C_5 used, as given in Table 1. This mode allows direct control of all five bits on one receiver, by the 32 codes from an SL490B transmitter. Fig.3 shows the ML924 used in this mode in conunction with an SL486 infra-red pre-amplifier.

Control Mode 2

Bits a and b, in the PPM input word, address one of up to four (binary 0 to 3) receivers that has been correspondingly designated that number (W_1W_0), by bits C_0 and C_1 in the control word (Table 1). Bits c and d in the PPM input word, address one of four outputs D to A, on this addressed receiver (Table 1, note 2), via code V_1V_0. Output E is not used.

Bits C_2 to C_5, in the control word, select combinations of output types; either set/reset (S/R) or momentary (M) as shown in Table 1. The addressed output (V_1V_0) on the addressed receiver (W_1W_0) will either be reset by bit e of the PPM input word (logic '0'), or set (pulsed if momentary type output), if bit e is logic '1'.

This mode thus allows the state of up to 16 bits (4 each on 4 receivers), to be individually controlled by the PPM input word, with the 32 codes from an SL490B transmitter. Table 2(a) shows, in detail, the received code interpretation for mode 2.

Control Mode 3

The PPM input word can be interpreted as address or data, depending on the logic state of bit e. If bit e is logic '0', bits a to d address one of up to sixteen (binary 0 to 15) receivers that has been correspondingly designated that number ($U_3U_2U_1U_0$) by bits C_0 to C_3 in the control word (Table 1). If bit e is logic '1', then bits a to d correspond to the outputs A to D on the currently addressed receiver.

The output types can either be all latched (LA) or all momentary (M), depending on the logic state of control bits C_4 and C_5 (Table 1).

Output E of the currently addressed receiver is used as an address acknowledge output (true high), and will go high upon reception of a valid address code. This output will remain high until reception of an invalid address code, or a power-on reset. Thus, only one of the sixteen possible bit E outputs will be high at any one time.

In this manner, up to sixty-four bits (four bits each on sixteen receivers) can be individually controlled by the PPM input word, with the 32 codes from an SL490B transmitter. Fig.5 outlines the application diagram for mode 3, using the maximum possible number of receivers (for one PPM rate). Details of the input PPM code interpretation for mode 3 are given in Table 2(b).

In all modes, taking the output enable input (pin 17) low swithces off all the outputs, except data ready, but the device retains the data internally.

The momentary (M) type of output means that data is available during reception of the PPM input word only, i.e. after a valid word has been detected by the ML924. A valid word is realised when two successive identical PPM input words are detected. The DATA READY output is at logic '1' during the reception of a valid PPM input word. All momentary outputs will be returned to zero when reception of the valid PPM input word ceases (i.e. a successive word is different or absent from the preceding word). DATA READY will also return to the zero state. If the latched (LA) type of output has been chosen, the received data will be latched and retained when reception ceases. Note also that in mode 3 a valid (matched) received address code is also latched. Similarly, for a set/reset (S/R) type of output, data is retained when reception ceases.

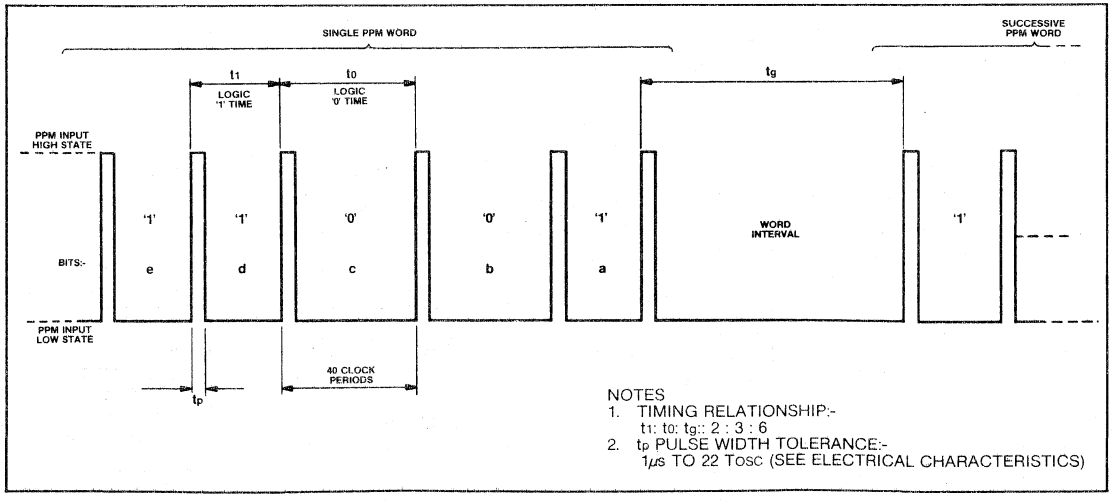


Fig.4 PPM input word format, showing 11001 example

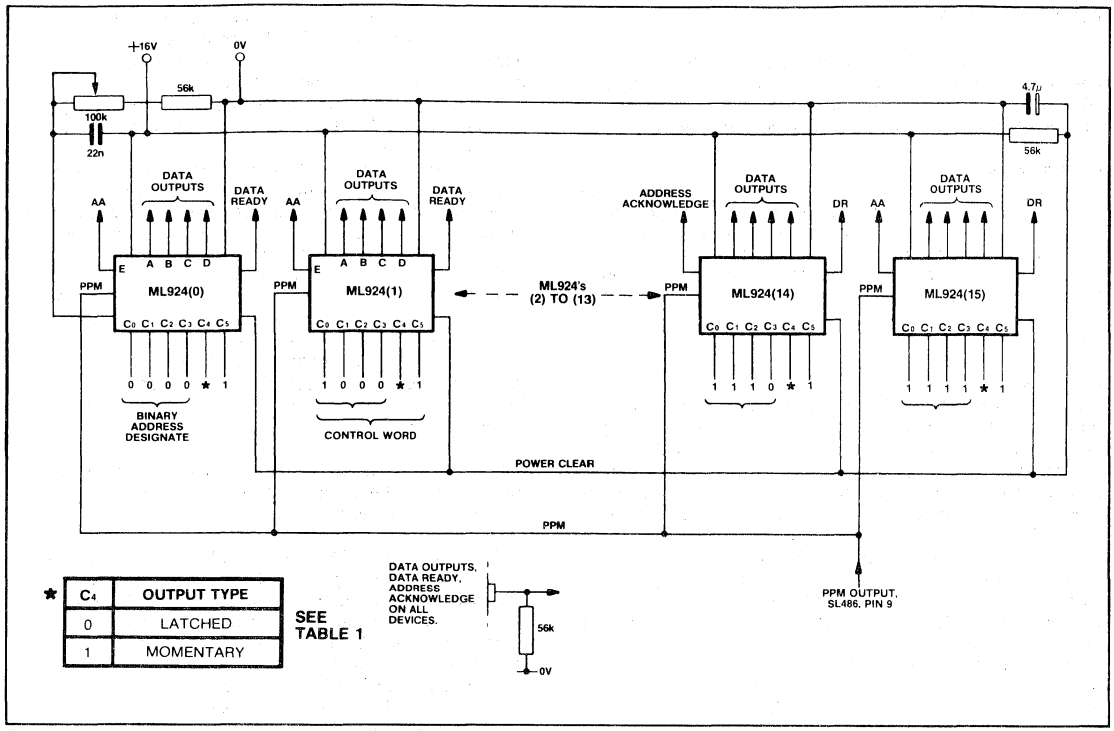


Fig.5 Application for controlling up to 64 bits in mode 3

Control word						Control mode	Output response					Interpretation of PPM input words	
C_5	C_4	C_3	C_2	C_1	C_0		E	D	C	B	A	e d c b a	e d c b a
0	0	0	0	0	0	1	LA	LA	LA	LA	LA	E D C B A	
0	0	0	0	0	1	1	LA	LA	LA	LA	M	PPM decoded on all outputs directly	
0	0	0	0	1	1	1	LA	LA	LA	M	M		
0	0	0	1	1	1	1	LA	LA	M	M	M		
0	0	1	1	1	1	1	LA	M	M	M	M		
0	1	1	1	1	1	1	M	M	M	M	M		
0	0	1	0	W_1	W_0	2	-	S/R	S/R	S/R	S/R	0 V_1 V_0 W_1 W_0	1 V_1 V_0 W_1 W_0
0	1	0	0	W_1	W_0	2	-	S/R	S/R	S/R	M	Output address / Receiver address	Output address / Receiver address
0	1	0	1	W_1	W_0	2	-	S/R	S/R	M	M	Resets an S/R type output. No effect on a momentary output.	Sets an S/R type output, or pulses a momentary output.
0	1	1	0	W_1	W_0	2	-	S/R	M	M	M		
1	0	U_3	U_2	U_1	U_0	3	AA	LA	LA	LA	LA	0 U_3 U_2 U_1 U_0	1 D C B A
1	1	U_3	U_2	U_1	U_0	3	AA	M	M	M	M	Receiver address Designates address mode	PPM data Sent to outputs on addressed receiver Designates data mode

Table 1 Interpretation of ML924 control word

NOTES
1. Control mode 1 : Direct response to the PPM code.
2. Control mode 2 : W_1W_0 is a 2 bit address for the receiver, designated W_1W_0 by the control word. V_1V_0 selects one of 4 outputs on the addressed receiver.

V_1	V_0	Addressed output
0	0	A (Pin 16)
0	1	B (Pin 15)
1	0	C (Pin 14)
1	0	D (Pin 13)

3. Control mode 3: $U_3U_2U_1U_0$ is a 4 bit address that selects, by means of 16 PPM codes, the receiver designated $U_3U_2U_1U_0$ by the control word, when bit e of the PPM code is '0'. If bit e is '1', the 4 outputs A to D on the currently addressed receiver are directly controlled by bits a to d.
4. Control mode 3: The E output of the receiver acts as an address acknowledge (AA) output. This goes high when a receiver detects a valid address instruction, and indicates that it will receive subsequent data transmission.

OPERATING NOTES

Receiver Oscillator

The receiver operates on a time scale fixed by an internal oscillator and its external components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receiver systems to respond to different transmission rates within the same area). If more than one ML924 is being used in a receiver system (control modes 2 or 3) the oscillators can be connected together, still allowing the receiver system timing to be set with one adjustment only. In other words, only one RC arrangement is needed, with pin 1 on all ML924's connected together for the devices constituting the single receiver system.

Setting Up Procedure

When designing a system using the SL490B/491 transmitters and the ML924 receiver, it is not necessary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33k from pin 16 of the SL490B/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula $t_o = 1.4CR$. Provided fairly close tolerance components are used for C1 and R1, then assembled transmitter units should be interchangeable without adjustment.

The timing components on the ML924 receiver can be selected using the formula

$$f_{rx} = \frac{1}{0.15CR} \text{ where } f_{rx} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

The value of R for the receiver should be between 47k and 200k, a typical arrangement being to use a 47k fixed resistor and a 100k pot as shown in Fig.6. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic '0' time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

Maximum Bit Control

In all modes, the maximum possible number of bits that can be controlled by one 32 code transmitter, can be increased by using more than one PPM rate. For example, it is possible to control a maximum of 128 bits in mode 3, by using 16 receivers operating on one PPM rate, and 16 receivers operating on a second PPM rate separated from the first by a fator of at least 2. If using an SL490B transmitter, a transmission rate of n and (nx2) may be incorporated in one device application, thus allowing 128 bits to be controlled by one 32 code transmitter.

PPM word bits	a b 1 1	a b 0 1	a b 1 0	a b 0 0	WoW1	c	d	e
Receiver address/ control word bits	Co C1 1 1	Co C1 0 1	Co C1 1 0	Co C1 0 0				
Sets an S/R type output to 1; pulses momentary output	31	30	29	28	VoV1	1 1 / D		1
	27	26	25	24	VoV1	0 1 / C		1
	23	22	21	20	VoV1	1 0 / B		1
	19	18	17	16	VoV1	0 0 / A		1
Resets an S/R type output to zero; no change momentary output	15	14	13	12	VoV1	1 1 / $\bar{D}$		0
	11	10	9	8	VoV1	0 1 / $\bar{C}$		0
	7	6	5	4	VoV1	1 0 / $\bar{B}$		0
	3	2	1	0	VoV1	0 0 / $\bar{A}$		0

Decimal equivalent codes (a) mode 2

ML924 output address

PPM word bits	a b 1 1	a b 0 1	a b 1 0	a b 0 0	c	d	e
Receiver address/ control word bits	Co C1 1 1	Co C1 0 1	Co C1 1 0	Co C1 0 0	C2	C3	
Output data	31	30	29	28	1	1	1
	27	26	25	24	0	1	1
	23	22	21	20	1	0	1
	19	18	17	16	0	0	1
Address data	15	14	13	12	1	1	0
	11	10	9	8	0	1	0
	7	6	5	4	1	0	0
	3	2	1	0	0	0	0

Decimal equivalent codes (b) mode 3

Table 2 ML924 received PPM code interpretation, for modes 2 and 3

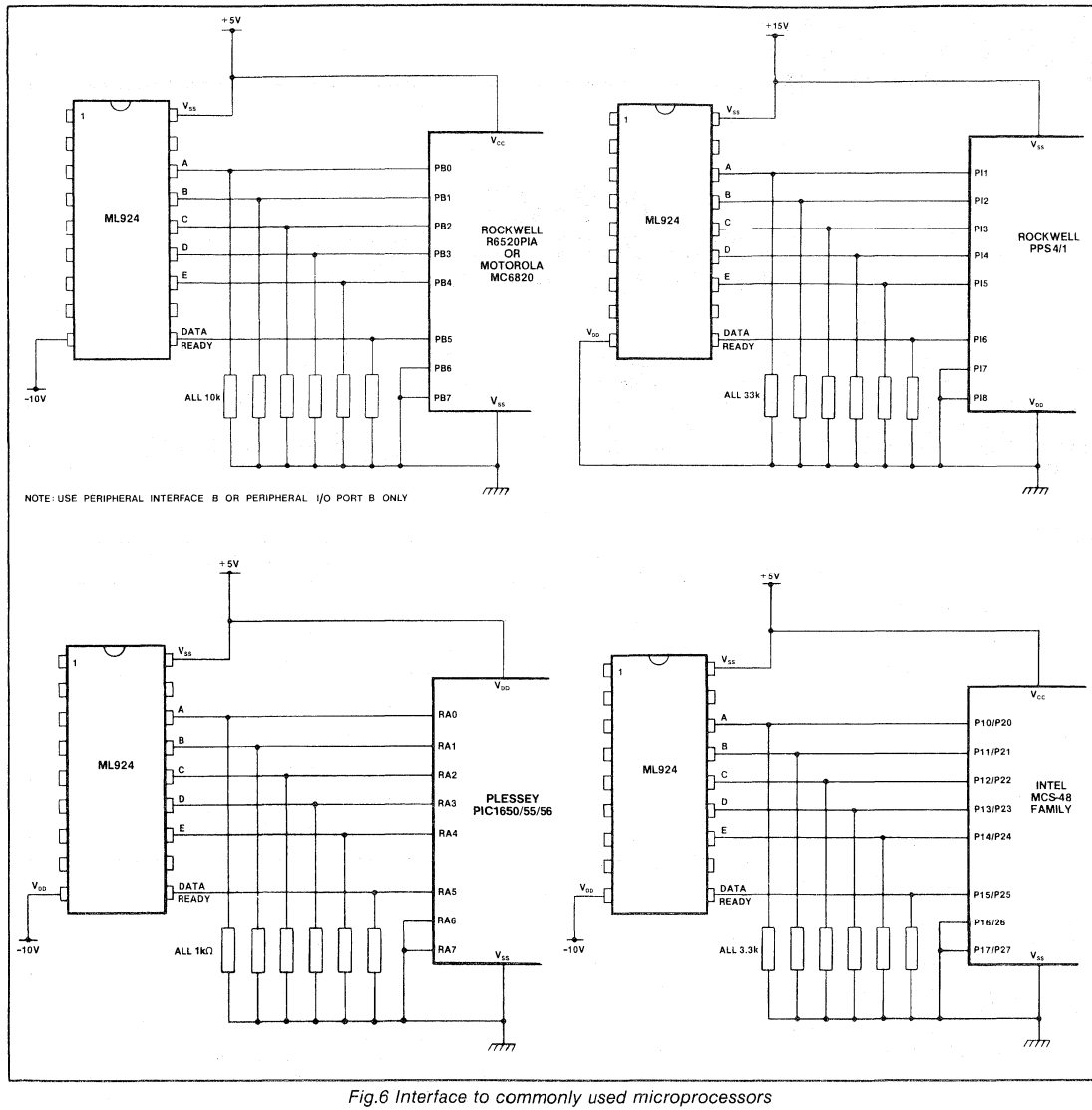


Fig.6 Interface to commonly used microprocessors

ML926/7

REMOTE CONTROL RECEIVERS (WITH MOMENTARY OUTPUTS)

The ML926 and ML927 are MOS LSI monolithic circuits for use as receivers of remote control signals for television control and many other applications. They are general purpose devices each receiving sixteen of the thirty-two codes transmitted by the SL490 circuit as pulse position modulation (PPM).

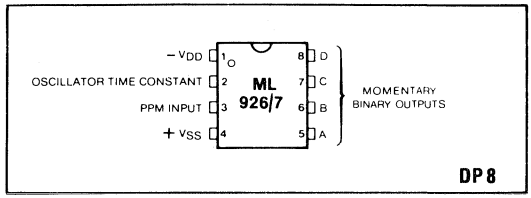


Fig.1 Pin connections (top view)

FEATURES

- Minimum Package Size – 8-Lead Minidip
- Four Outputs Indicate in Binary the Code Currently Being Received, and Are Switched Off (Low) When No Valid Code is Detected.
- On-Chip Oscillator
- High Power, Free Drain, Output Buffers

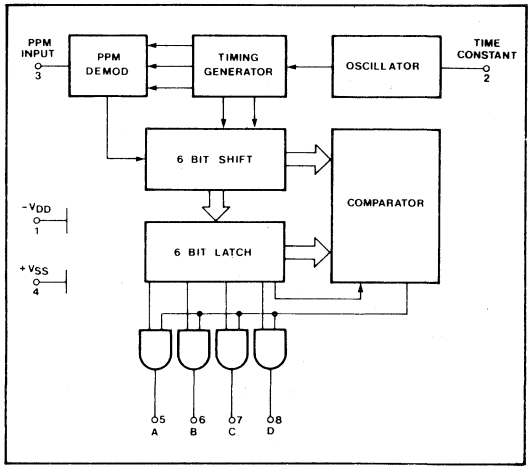


Fig 2 Block diagram

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates withint the same area).

Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

The ML926 responds only to codes 00001 to 01111 from the SL490 transmitter whereas the ML927 responds to codes 10001 to 11111.

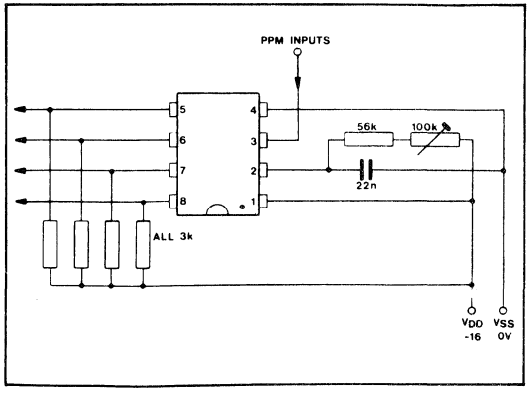


Fig. 3 Test circuit

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to −25V
Storage temperature	−55°C to +125°C
Operating temperature ambient	−10°C to +65°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$V_{DD} = -16V$, $V_{SS} = 0V$
$T_{amb} = 25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		12	14	18	V	
Current consumption	1	2	3	4	mA	
PPM input						
Input level high	3	−1		0	V	
Input level low	3	V_{DD}		−6	V	
Input pulse width	3	1		$22T_{OSC}$	μsec	$T = \frac{1}{f_{osc}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss 100kΩ to V_{DD}
Variation wrt V_{DD}			1		%/V	
Output voltage high	5-8	-1.5		0	V	R_L = 3.0K to VDD
Output device leakage (Output OFF)	5-8			1	μA	

Note 1. R_{osc} (Pin 2) is 56k-156kΩ, $f_{OSC} \simeq \frac{1}{0.15CR}$ ±20%

PIN FUNCTIONS

POSITIVE LOGIC '1' = Vss, '0' = V_{DD}

1. V_{DD}
−14V to −18V power supply

2. Oscillator time constant
An RC time constant of a capacitor and resistor at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal 'low' level with pulses to high level corresponding to the PPM pulses from the transmitter.

4. Vss
0V (ground)

5-8. A,B,C,D
Four open drain high power transistors give a binary coded output of the valid code being received.

	Momentary binary outputs	
Transmitter Code	ML926	ML927
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 0 1	0 0 0 1	↓ ↓ ↓ ↓
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1. 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	↓ ↓ ↓ ↓
1 0 0 0 0	0 0 0 0	0 0 0 0
1 0 0 0 1	↓ ↓ ↓ ↓	0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0		0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1	↓ ↓ ↓ ↓	1 1 1 1

Table 1 Response to SL490 codes

PLESSEY
Semiconductors

ML928/9

REMOTE CONTROL RECEIVERS
(WITH LATCHED OUTPUTS)

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML928 and ML929 are general purpose remote control receivers, each receiving and latching 16 of the 32 codes transmitted by the SL490 circuit in the PPM (Pulse Position Modulation) mode. The ML928 responds to codes 00000 to 01111 only, and the ML929 to codes 10000 to 11111. Both devices are packaged in 8-lead minidip to minimise board area. The on-chip oscillator may be adjusted from 15Hz to 150kHz, allowing different transmission rates. They have a high degree of immunity to incorrect codes; there must be two consecutive correct codes received before the outputs can change.

FEATURES

- Accepts 5 Bit PPM
- On-Chip Oscillator, 15Hz to 150kHz Range
- Easily Used With Ultrasonic, Infra-Red or Other Transmission Media
- Four High Drive Outputs
- 16 Latched States
- Minimum Sized Package

QUICK REFERENCE DATA

- Power Supply: 12V to 18V. Typical 4mA at 16V.
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 Bit with successive codeword comparison
- Outputs: Maximum 15mA sourced from open drain drive
- Logic convention: Logic 0 – output transistor ON, pulls output to V_{SS}
  Logic 1 – output transistor OFF

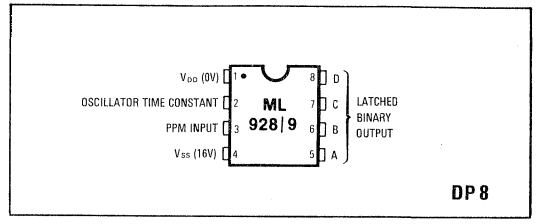


Fig.1 Pin connections - top view

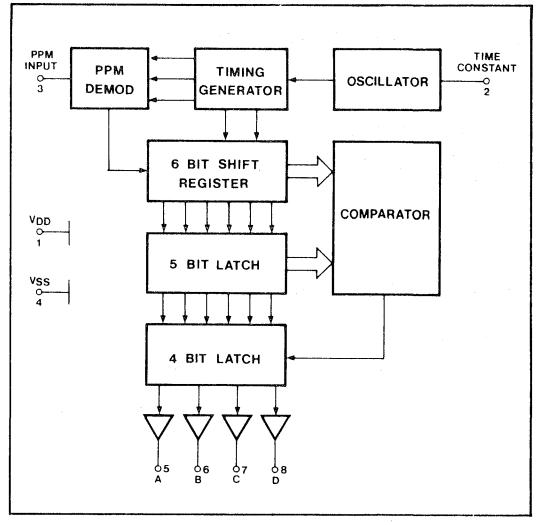


Fig. 2 ML928, ML929 remote control receivers block diagram

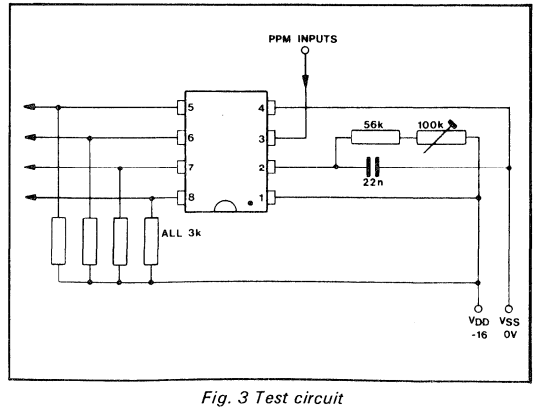


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{SS} = 0V
V_{DD} = −16V
T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current Consumption V_{DD}	1	3	4	5	mA	
Supply voltage	1	−12		−18	V	
PPM input	3					
Logic '0' level		−1		0	V	
Logic '1' level		V_{DD}		−6	V	
Input pulse width		1		$22T_{osc}$	μs	$T_{osc} = \frac{1}{f_{osc}}$
Oscillator Timing	2					
Frequency		15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss, 100kΩ to V_{DD}
Variation w.r.t. V_{DD}			1		%/V	
Latched binary output	5, 6, 7, 8	-1.5		0V	V	RL = 3.0k to VDD
Logic '0' output voltage						
Output leakage in logic '1' state				1	μA	

Note 1. $R_{osc.}$ (pin 2) is 56k-156k Ω. $f_{osc.} \simeq \frac{1}{0.15CR}$ ±20%

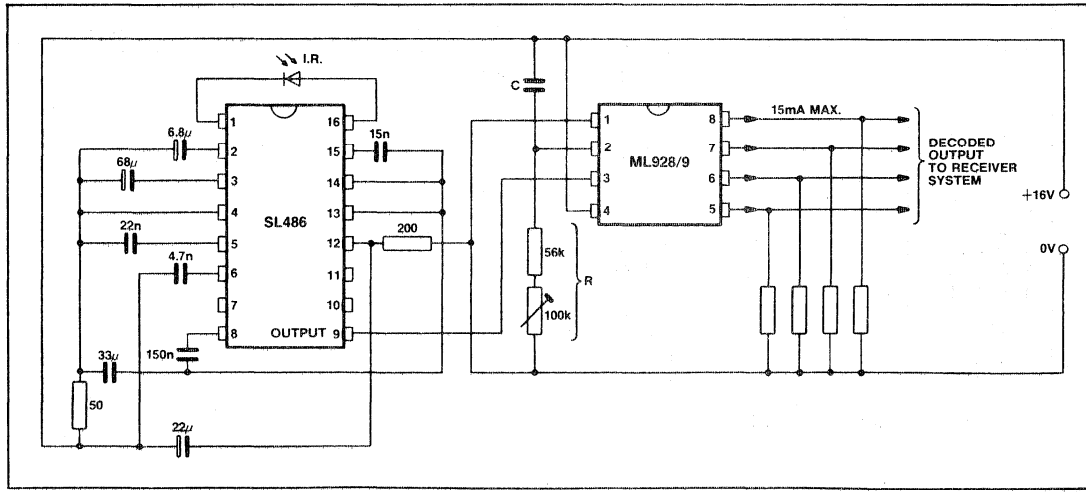


Fig.4 Typical application circuit, also shows general SL486 interface

PIN FUNCTIONS

Negative logic: '0' is 0V (V_{SS}), '1' is – 12V to –18V (V_{DD})

1. V_{DD}
–12V to –18V power supply

2. Oscillator time constant
An R-C time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz at 150Hz and should be set so that there are 40 periods in one 't_o' transmitter pulse interval.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal low level with pulses to high level corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A,B,C,D
Four open-drain high power transistors give a binary coded latched output of the last valid code received.

	Latched binary outputs	
Transmitter Code	ML928	ML929
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	No change
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0		0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0	No change	0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

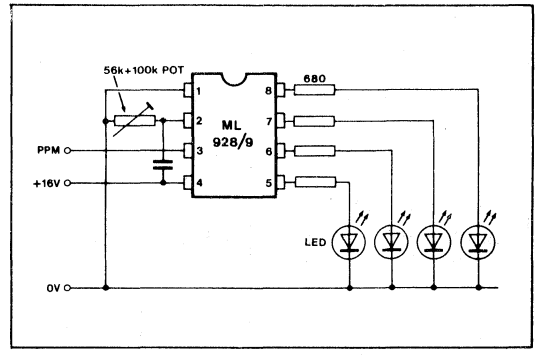


Fig. 5 Direct drive of LEDs

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to –25V
Storage temperature	–55°C to +125°C
Operating temperature ambient	–10°C to +65°C

PLESSEY
Semiconductors

MR9710

TELEVIEW DATA ACQUISITION CHIP

The MR9710 Data Acquisition (DA) chip is one of the set of LSI devices comprising the Plessey Semiconductor Televiewe (Teletext/Viewdata) system. It receives data from a TV signal or Telephone Line via an appropriate interface and processes the data accordingly. Under instruction from a control device it acquires the requested data and loads it into the correct location in the preselected page store. Control information extracted from the incoming data is provided to the Televiewe system.

The device is fabricated in Plessey Semiconductor N-channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability. It is supplied in a 40 lead dual-in-line package.

FEATURES

- Processes Teletext and Viewdata Input Data
- Direct Interface with Televiewe Highways
- Direct Interface with Standard UAR/T
- TTL Compatible Serial Teletext Data Input
- Full Checking of Teletext Data including Parity, Hamming and Data Frequency
- 'Don't Care' Digit Facility
- Non-used Viewdata Control Codes made available to Control Processor.
- Addresses Up To Eight Page Stores

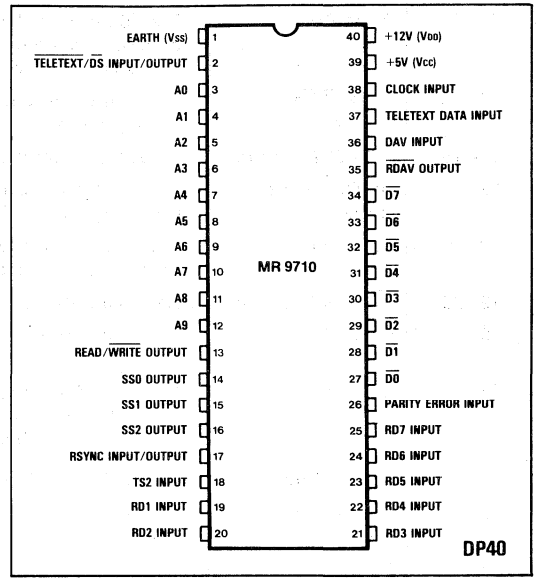


Fig.1 Pin connections - top view

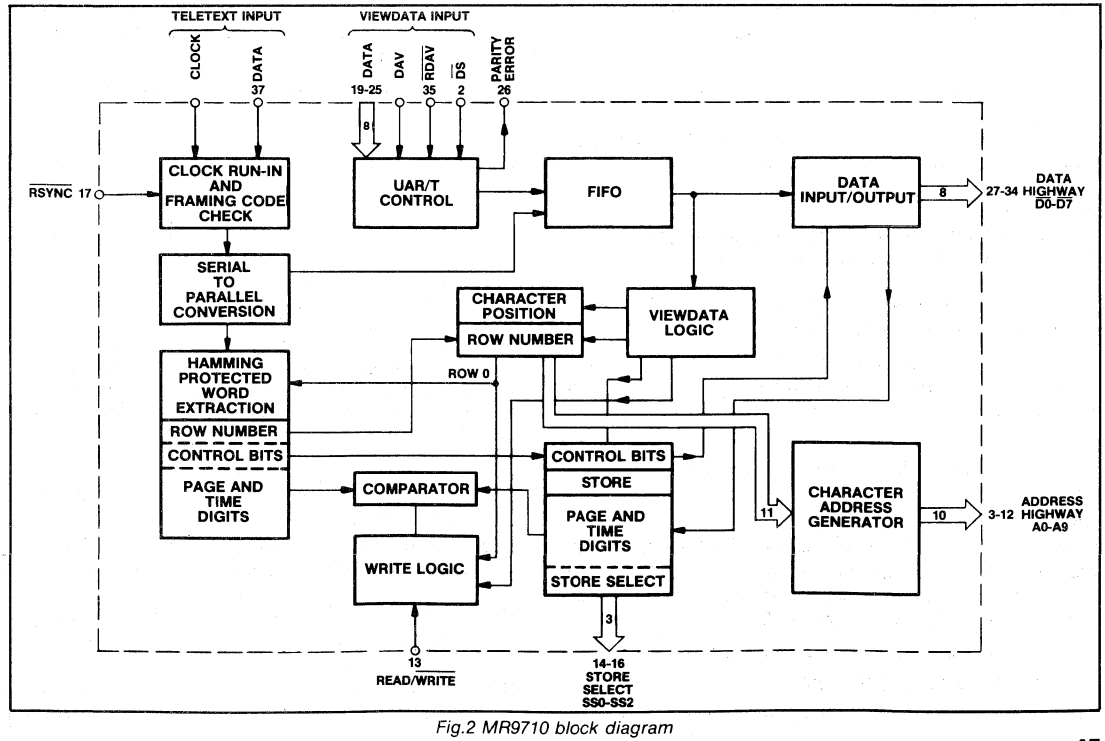


Fig.2 MR9710 block diagram

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the device and the reference for all signals and electrical parameters.
2	$\overline{\text{TELETEXT}}$/$\overline{\text{DS}}$ INPUT/OUTPUT	When strapped to earth (low level), the DA chip will process Teletext. In Viewdata it is the data strobe output to the UAR/T (active low).
3–12	A0 to A9	The 10 bits of address connected to the Address Bus of the Teleview system. As outputs they are tristate and active push-pull for high speed driving the store. They are also inputs to enable the device to be addressed.
13	Read/$\overline{\text{Write}}$ Output	The read/write control of the page Stores. The Stores will output data (read) when this signal is high.
14–16	SS0–SS2 Outputs	Three bits of Store Select code enabling one of the eight page Stores.
17	$\overline{\text{RSYNC}}$ Input/ Output	A low going pulse indicates to the DA the start of a Teletext line. The DA will output a low going pulse within a few microseconds to re-synchronise the Data Slicer.
18	TS2 Input	The second of the two time slot bits which, when true, indicates that the DA may use the Data and address highways.
19–25	$\overline{\text{RD1}}$–$\overline{\text{RD7}}$ Inputs	Received Data taken directly from the UAR/T.
26	Parity Error Input	The Parity error signal from the UAR/T.
27–34	$\overline{\text{D0}}$–$\overline{\text{D7}}$	Data I/O's for connection directly to the Teleview Data highway. As an output the active state is low and there is a passive pull-up on chip so that the signals on the highway may be 'wire-ored'.
35	$\overline{\text{RDAV}}$ Output	Low active signal to the UAR/T which will reset its data available output.
36	DAV Input	The Data Available signal from the UAR/T to indicate a character is available at the RD1–RD7 pins.
37	Teletext Data Input	Serial data input from a Data Slicer (e.g. SL9100). TTL compatible. If not used this input should be held low.
38	Clock Input	Normally the Teletext clock running at 6.9375 MHz and synchronised to the Teletext data by $\overline{\text{RSYNC}}$. In Viewdata only applications a 6MHz clock as used by the Video generator may be input here. TTL compatible.
39	Vcc	Connected to +5V. This has a low current requirement and is used mainly for the output drivers.
40	Vdd	Connected to +12V, the main positive supply for the device.

OPERATION

The Data Acquisition (DA) chip takes data from either the TV (Teletext) or telephone line (Viewdata) via the appropriate interface, processes it accordingly to type and user requests and loads the display data in the correct position in one of eight page Stores.

The processing of Teletext and Viewdata information is described in separate sections as is the interchange of data with the rest of Teleview system.

TELETEXT

If pin 2 is held low the DA may receive data via the serial Teletext data input.

While TS2 is true the DA will monitor $\overline{\text{RSYNC}}$ and the address highways. If a pulse appears on $\overline{\text{RSYNC}}$ it will process a Teletext data-line. At other times while TS2 is true it will respond to signals on the address highway and interchange data with a Control Device.

While TS2 is false the DA will do nothing.

TELETEXT DATA RECEPTION

Data is extracted from the TV video signal by an external circuit called the Data Slicer. This circuit provides a serial data signal and a clock to the DA's input.

A 0.5μsec negative pulse generated by the MR9735 Video Generator will appear on the $\overline{\text{RSYNC}}$ line just before the data on a possible Teletext line. This pulse stops the clock in the low state and primes the MR9710 to monitor the Teletext Data Input for clock run-in. The first negative transition restarts the clock which is used as a reference against which to compare the incoming signal. If the frequency is correct the MR9710 outputs a second $\overline{\text{RSYNC}}$ pulse which allows accurate resynchronisation of the clock for the rest of the Teletext line. If the frequency check fails the MR9710 goes back to its idle state waiting for a new $\overline{\text{RSYNC}}$ signal or the Data Interchange time.

After a valid clock run-in has been detected Teletext data is clocked into a serial to parallel converter and Framing Code detector. A time out will cause DA to go idle, while the detection of Framing Code will byte synchronise the S–P converter and start the DA receiving the Teletext data as shown in Fig.3.

The first two words following the Framing Code have data protected by Hamming Code and the appropriate

checks and corrections are performed. If the row address indicates that the data is a Page Header (Row 0) then the following 8 words are also processed by the Hamming Code circuit. If any Hamming Code fails such that it cannot be corrected, then that data line is rejected.

Requests for pages of Teletext data are input to the DA during the Data Interchange periods, described later. When a new page is selected the Page and Time store in the DA is loaded with all '1's indicating 'don't care' digits. As keys are pressed by the user of the Teleview system the values are loaded into the DA in the appropriate position.

A comparator in the DA compares Magazine, Page and Time digits one at a time as they are received in the data stream with the digits stored. The comparator will give a true output if the digit compares exactly or if the stored digit is all 1 (value 15). Where an incoming digit has a range less than 4 bits, e.g. time hours tens has the range 0-3 or 2 bits, the unused bits will be made to compare.

Every line of data received is checked for comparison on Magazine number. If this does not compare and the row address indicates that the row is not a Page Header then that row is rejected.

If the Magazine number does not compare and it is a Page Header then, with the exception of Rolling Headers, it is again rejected.

From the time that the DA is told that the P key has been pressed until the selected page has been captured for the first time all Page Headers that compare on Magazine number are loaded into the Store except those with the Interrupted Sequence bit (C9) set. This mode of display is referred to as Rolling Headers and provides an indication to the user that data is being received. During this mode the Magazine Serial bit (C11) will over-ride the Magazine comparison. A page of data may be captured when the page number has been fully enetered, i.e. the 3rd digit has been received or the T key has been pressed, and a Page Header is received whose Magazine, page and time digits compare with those stored in the DA. That header and all subsequent data lines with correct Magazine number will be stored up to and excluding the next Page Header of correct Magazine number. A 'Page being received' indication will be set at this time for transmission to the Control device.

When a Page Header is received that fully compares the Control bits accompanying that Header will be stored for subsequent transmission to the Control.

When the content of a data line is ready to be stored that data is loaded into the appropriate Store as defined by the signal from the Control device. Its position in the Store is defined by the Row Address of that data line, the location of the first character being 40 times the Row Address (with the exception of the Page Header which does not have the first 8 characters), with following characters being stored in the next 39 locations of Store.

Each character is checked for odd parity and if the check fails that character is not written. The write signal is removed to avoid overwriting a possible valid character already existing in Store.

The last eight characters of every Page Header contain the current clock time and are always written to Store.

VIEWDATA

With pin 2 connected to the Data Strobe input to a UAR/T and not held to earth the DA will process Viewdata.

While TS2 is true the DA is active as far as the Teleview highways are concerned and it will monitor $\overline{\text{RSYNC}}$ and the Address highway.

When an $\overline{\text{RSYNC}}$ pulse appears the DA will process any Viewdata character it has available. Whenever it is not processing characters it may receive characters asynchronously from the telephone line, via the exclusive connection to the UAR/T, and store them within the DA. Up to three characters may be received and stored before the next processing period when they may be loaded into the page store. Data Interchange with the Teleview system may occur when TS2 is high.

ASYNCHRONOUS DATA RECEPTION

The standard UAR/S (MR1015D) will convert the serial data received via the modem to parallel data for inputting to the DA and indicate a character is ready by the data available (DAV) line. At any time, except when actually processing previously received characters, the DA will read the data and acknowledge on $\overline{\text{RDAV}}$, a minimum of 3μsec after the DAV signal.

VIEWDATA CHARACTER PROCESSING

The eight bit input consists of seven bits of data plus a parity fail indication. The codes are shown in Fig.4.

Characters intended for storage are loaded into the Store in a location determined by the Character Address counter which is always arranged to point to the position in Store into which the next character will be written. The counter is manipulated by the Control Characters appearing in Cols. 0 and 1 in the character table.

0/8, Back Space, will cause the Character Address counter to be decremented by one.

0/9, Horizontal Tab, will cause the Character Address counter to be incremented by one.

0/10, Line Feed, will increment by 40.

0/11, Vertical Tab, will decrement by 40.

0/12, Form Feed, will reset to zero.

0/13, Carriage Return, will position the Character Address counter to the beginning of the current block of 40.

0/14, Cursor Home, will reset to zero.

A character in columns 2-7 will be written into the appropriate Store at the location indicated by the Character Address counter which will then be incremented by one.

The ESC character (1/11) will cause some modification of the following character as follows:-

If the character is in cols. 4 or 5 it will be written to Store with the most significant bit changed to Zero.

If the character is in col. 3 it will not be written to Store but made ready for transmitting to the Control device.

Any other characters, except NUL, will cancel the ESC sequence and be ignored.

The Form Feed character (0/12) will cause the F bit to be set in the appropriate DA to Control signalling word.

All other control characters in cols. 0 and 1, except NUL, will be sent to the Control at the appropriate time.

If any character has the parity fail indication set then the character 7/15 will be written to Store. At the start of a processing period (i.e. at $\overline{\text{RSYNC}}$) if a character is available for processing then the DA will erase the Cursor bit by reading the location pointed to by the Character.

Address counter and re-write it. Since the DA never writes the 8th bit in the Store the cursor will be removed.

DATA INTERCHANGE

During the DA's active period, indicated by TS2, when it is not performing any data processing then it will monitor the Address highway for the following codes:

1111XXXX0X indicates the DA should receive data from the data highway.

1111XXXXX0 indicates that the DA should send data to the data highway.

1111X0XXXX indicates that the DA should provide control to the UAR/T.

In the Receive mode the Control device may send data according to the codes in Table 1. The most significant bit of the data acts as a strobe which will cause the other 7 bits to be received and stored in the DA. Magazine, Page and Time digits will be stored in the appropriate location in the digit store, the Store Select number will be stored for use when accessing the Store and the indications of P and T keys being processed will also be latched for use in the processing period.

The receiving of data from the Control is completely asynchronous to the DA's internal clock and is controlled entirely by the Strobe bit.

The Send mode will cause the DA to apply the first code, shown in Table 2, to the data highway. When the code has been read by Control the signal will be acknowledged by Control forcing all 1's (low levels) which will step the DA onto the second word and so on. The Strobe bit is used in this case to indicate that the data is appearing for the first time and once read by Control, is cleared until new data is available. The exception is the first word which always has the Strobe set.

The UAR/T control is recognised by the DA since it has the UAR/T connections and in this mode a Strobe on the data highway will cause the DA to provide a data strobe $\overline{DS}$ to the UAR/T.

During the Data Interchange period the DA will monitor the Store Select lines and if they are all taken low it will output the current content of the Character Address counter to the address highway so that the Control may know where to insert the cursor.

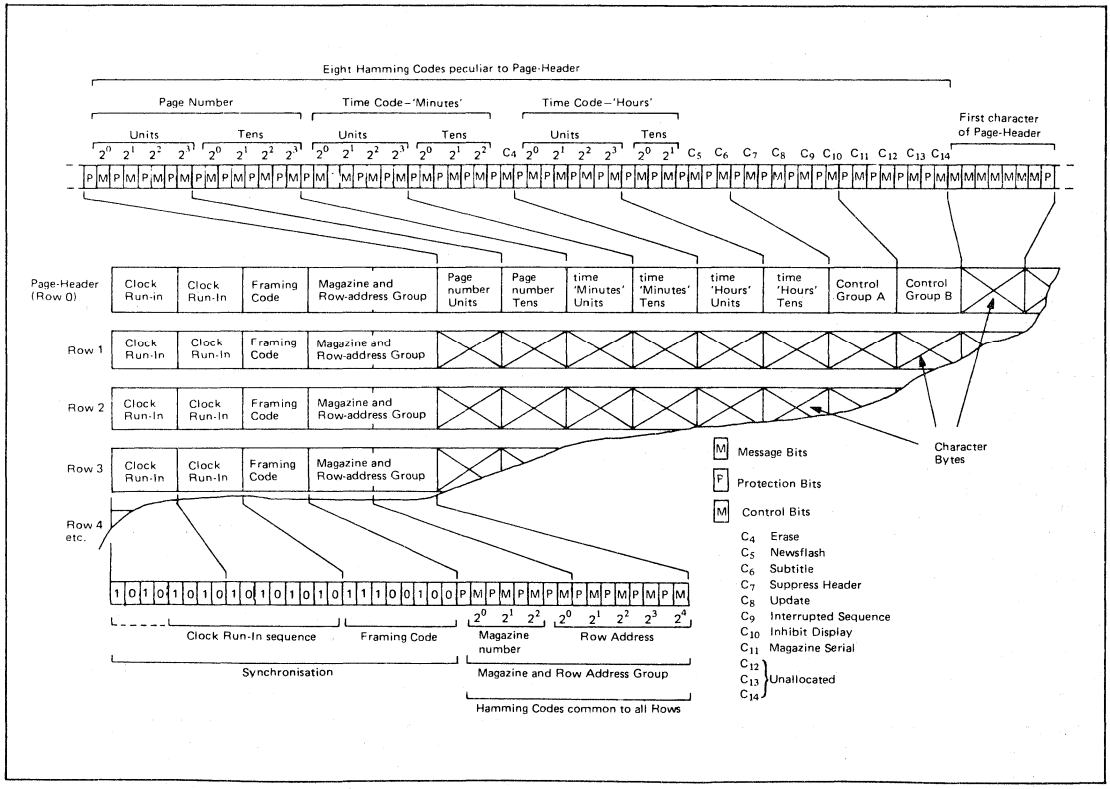


Fig.3 Synchronisation and Hamming codes at start of page-header and row transmission

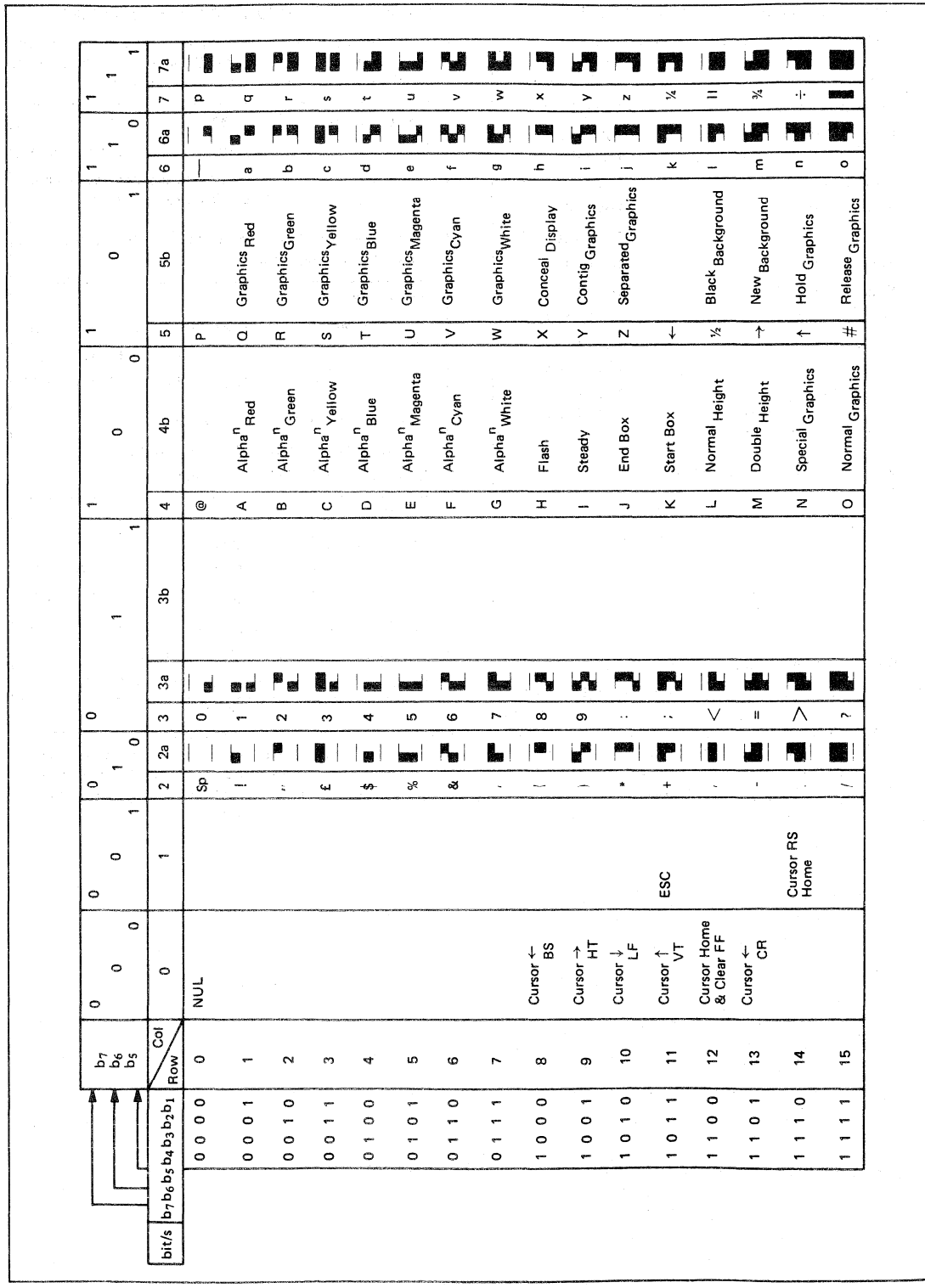


Fig.4 Viewdata transmission codes recognised by the MR9710

CONTROL TO DATA ACQUISITION SIGNALLING

Active low signalling, most significant bit is a strobe.

Highway Free		0000 0000
Magazine Number		1000 Dddd
Page Number,	tens	1001 Dddd
	units	1010 Dddd
Store Select		1011 0Sss
Key Pressed		1011 10Kk
Spare Code		1011 1100
Spare Code		1011 1101
Spare Code		1011 1110
Dummy Code		1011 1111
Time Hours,	tens	1100 Dddd
	units	1101 Dddd
Minutes,	tens	1110 Dddd
	Units	1111 Dddd

Where Kk is key identification:

P	00
T	01
Spare 1	10
Spare 2	11

Table 1

Sss is store select number, 000 to 111.

Dddd, Digit key value, initially values 0–9 and 15 used although any value may be sent. For Teletext the magazine range is 0–7, Time hours tens range 0–3, Time minutes tens range 0–7. In addition digit 15 is recognised by the DA as a 'don't care' digit causing automatic comparison.

DATA ACQUISITION TO CONTROL SIGNALLING

Active low signalling, most significant bit is a strobe. Signals acknowledged by the Control forcing all ones. Control word 1 is sent first and is always sent.

Control word 1		1000	T	S	s	s
Where T		is the Teletext bit, 1 = Teletext.				
S s s		is the Store Select number the DA is currently using.				
Control words 2–4 depend on whether Teletext or Viewdata is being processed.						
TELETEXT						
Control word	2	1001	PBR	C4	C6	C5
	3	1010	C10	C9	C8	C7
	4	1011	C14	C13	C12	C11
Sent* only when Valid Header received.						
PBR is set while a page is being received.						
C4 to C14 are the Teletext Control bits.						
VIEWDATA						
Control word	2	1001	X	F	0	0
	3	1010	b7	0	b6	b5
	4	1011	b4	b3	b2	b1
Sent* only when a Control character received by DA.						
F is set when Form Feed character processed.						
b1–b7 are the 7 bits comprising the Viewdata Character.						

Table 2

***NOTE:** that 'sent' means the Strobe bit is set. The other seven bits are actually put onto the highway at the request of the Control and may be used if appropriate (page being received, for example).

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Voltage on any pin with respect to Vss	−0.3V to +15V
Storage Temperature	−55°C to +150°C

Exceeding these ratings could cause permanent damage. Functional operation is not guaranteed under these conditions, the operating ranges are specified below.

Operating Conditions

Supply Voltages	VSS = 0V (substrate voltage) VCC = +5V ± 5% VDD = +12V ± 10%
Temperature Range	0°C to +70°C

Characteristic	Min	Typ	Max	Units	Conditions
OUTPUTS					
Address Outputs (tri-state)					
High level	+2.4		Vcc	V	Ioh = −320μA
Low level		+0.2	+0.45	V	Iol = 3.2mA
Capacitance			15	pF	V = 0V
T rise, T fall			200	ns	C load = 100pF
Leakage, high impedance state			5	μA	V out = 0V or +5V
Data Outputs (passive pull-up)					
High Level	+2.4		Vcc	V	Ioh = −1.5mA
Low Level		+0.2	+0.45	V	Iol = 3.2mA
Capacitance			15	pF	V out = 0V
R/$\overline{W}$ and Store Select Outputs					
High Level	+2.4		Vcc	V	Ioh = −320μA
Low Level		+0.2	+0.45	V	Iol = 3.2mA
Capacitance			15	pF	V out = 0V
Current sourced, 'off' state	1.2		2.6	mA	V out = 0V
$\overline{RDAV}$ and $\overline{DS}$ Outputs					
High Level	+2.4		Vcc	V	Ioh = −25μA
Low Level		+0.2	+0.45	V	Iol = 100μA
Capacitance			15	pF	V out = 0V
$\overline{RSYNC}$ Output (Open Drain)					
Low Level		+0.2	+0.45	V	Iol = 4mA
Leakage, output off			10	μA	V out = +12V
INPUTS (except Clock and Teletext Data)					
High Level	2.2		Vdd	V	
Low Level	Vss		+0.8	V	
Leakage (except I/O's)			10	μA	V = +12V
Input Capacitance			15	pF	V in = 0V
Clock and Teletext Data Inputs					
High Level	2.8		Vdd	V	
Low Level	Vss		0.4	V	
Capacitance			20	pF	V in = 0V
Leakage			10	μA	V in = +12V
Frequency	1.0		7.5	MHz	
POWER					
Vcc Supply Current			15	mA	Vcc = +5.0V
Vdd Supply Current			72	mA	Vdd = +12V (at 25°C)

PLESSEY
Semiconductors

MR9735

TELEVIEW 625 LINE VIDEO GENERATOR

The Video Generator Chip is one of a set of LSI chips used in the Plessey Semiconductor TELEVIEW Teletext/Viewdata system. It reads the contents of a Page Store and generates outputs suitable for driving a normal 625 line Colour Television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronising signals within the receiver and locks the total TELEVIEW system onto the incoming interlaced. signals. When no transmission is taking place the chip generates an interlaced or non--interlaced composite sync. signal which is used to synchronise the receiver.

A full set of colour display facilities as described in the Broadcast Teletext Specification (September 1976) is provided by the device.

The device is fabricated in Plessey Semiconductors N-Channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability.

FEATURES

- Interlaced 625 line or non-interlaced 313 line operation
- 24 Row x 40 Character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for the other TELE-VIEW chips to indicate the status of the display scan.
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronising signals for the receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities
- Can receive Teletext on lines 7-22

DISPLAY FACILITIES

1. Provides the following display facilities controlled by 'control' characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.

(a) Alpha-numerics/Graphics in seven colour set.

(b) Colour or black backgrounds.

(c) Selected characters can be concealed.

(d) Selected characters can be flashed.

(e) 'Boxed' characters can be inserted into the normal Television Picture. This can be done manually or automatically.

(f) Characters may be either single or double height.

(g) Graphics characters may be contiguous or separated.

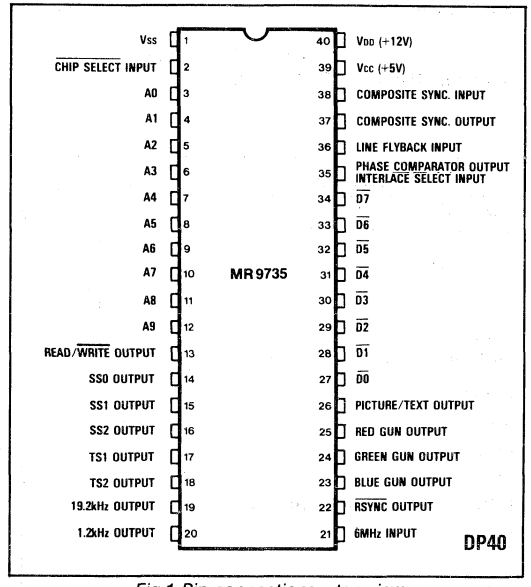


Fig.1 Pin connections - top view

(h) Graphics characters may be 'held' during other control characters.

(i) Special graphics for high resolution applications, a dynamically redefinable character set application also available.

2. Provides the following display facilities controlled from the users keyboard/keypad via the control chip (e.g. PIC1650-532).

(a) Switch between normal and data video.

(b) Teletext or Viewdata Operation.

(c) Clock time can be boxed into a normal picture (Teletext only).

(d) Display of one half of a page in double height.

(e) Black and white output of data in Mix Mode.

(f) Inhibiting of character rounding and flashing.

(g) Enabling of a cursor.

(h) Inhibit the display until updated.

(i) Reveal 'concealed' characters.

CHARACTER SETS

English	MR9735-002
German	MR9735-003
Swedish/Finnish	MR9735-004
Danish	MR9735-005
Italian	MR9735-006
Others	Contact Factory

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The chip can be put in its deselected state by connecting this input to Vcc. The input has an internal pull down to Vss. If connected to Vdd the test mode is selected.
3-12	A0-A9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required Page Store.
17,18	TS1,TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19,20	19.2kHz and 1.2kHz Outputs	These outputs provide 19.2kHz and 1.2kHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which is phase locked to the normal transmission for Teletext ON Hours operation. During OFF Hours working a free running crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	This output is an open-drain output and is used to indicate the presence of Teletext lines to the Teleview D.A. Chip MR9710 and Data Slicer SL9100. The timing of this signal is indicated in Fig.9.
23-25	Red, Green and Blue Outputs	These outputs are push-pull outputs which go high to turn on the relevant colour gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output may be used by the TV receiver to determine whether to display the normal TV Picture or the generated Text as provided at the Red, Green and Blue outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	$\overline{\text{D0}}$-$\overline{\text{D7}}$ Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output/Interlace Select Input	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In off-hours operation this open drain output goes high permanently, and thus can be used as an indication of on-hours/off-hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. In OFF Hours operation if the Phase Comparator output is held low a 313 line non-interlaced sync. is provided at the Composite Sync. output. If the Phase Comparator output is pulled high connected to Vcc via a 4.7k resistor interlaced sync. will be provided.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen. Line Flyback pulses are positive. If no Line Flyback is provided in OFF hours mode the display will be positioned so that the start of video is approximately 16μs after the negative edge of line sync.
37	Comp. Sync. Output	This output is an open drain output. In on-hours working or in Picture mode it outputs a regenerated composite sync. signal from the comp. sync. input. In off-hours working it outputs an internally generated composite sync.
38	Comp. Sync. Input	The Composite sync. input monitors the composite sync/video being received and extracts synchronising information and 'on-hours' 'off-hours' information for the Video Generator. This input must be predominantly high for 'off-hours' switching. Sync. pulses are negative.
39	Vcc	This pin is connected to the +5.0V supply.
40	Vdd	This pin is connected to the +10.0V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

The basic block diagram of the chip is shown in Fig.4 and major functional blocks are described below.

1. Comp Sync Generator and On Hours Detector

The prime function of this block is to detect negative going sync. signals from the incoming mixed sync. and to synchronise the TELEVIEW system with the transmitted signal. When the incoming transmission is turned off, (i.e. goes 'Off-hours'), this is recognised by the detector after at least 300ms of missing sync. pulses. An internally generated Composite Sync signal is then switched to the Composite Sync Out pin. Thus the receiver will continue in lock but synchronised to the Video Generator. Similarly if the normal transmission resumes, the fact that external sync pulses are being received is recognised by the Video Generator and the chip will re-synchronise itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync. at all times the chip can detect frame sync., line sync. and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Figs.7 and 8, but there are four periods i.e.

(i) Writing to RAM. TS10
This occurs during lines 7 to 22 under control of the D.A. chip.

(ii) Reading from RAM. TS00
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

(iii) Data Interchange Period. TS11
The Interchange of information between D.A., Control Processor and Video Generator occurs during this period (lines 23–47).

(iv) Spare TS01
During lines 289–296 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status the chip also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync. pulses are shown in Fig. 5.

2. Character Counter and Address Logic

The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If it is in the bottom half of the page, the address counter is initialized to 480.

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs at each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be described later. This facility is inhibited while displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for 40μs starting 3.5–6μs after LFB.

3. Input Latches and Character Read-Only Memory

The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organised as 96 characters each of 45 dots (5 x 9 array).

4. Data Control Latches (Colour Background Control)

Certain characters indicate to the video generator a change in display status. These characters are contained within columns 0 to 1 of the character set as shown in fig. 7 and may be used to change character colour, background colour, height, etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

5. Output Logic and Drivers

The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs are closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XX0XXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0
Control Word 1	1	0	0	0	T	S	s	s
Teletext								
Control Word 2	1	0	0	1	X	C_4	C_6	C_5
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}
Viewdata								
Control Word 2	1	0	0	1	X	F	0	0
Control Word 3	1	0	1	0	b_7	0	b_6	b_5
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1
Store Select for Display	1	1	0	0	SP	D	d	d
Key Data	1	1	0	1	*	P	*	*
Other Facilities	1	1	1	0	X	BH	M	BC

The Control bits are as follows:-

T	TELETEXT MODE i.e. NOT VIEWDATA
Sss	Identification of Store being written to
Ddd	Identification of Store being displayed from

(a) Teletext

C_4	Erases rows 1-23 of Store defined by Sss and resets Reveal if Sss = Ddd
C_5	Newsflash
C_6	Subtitle
C_7	Suppress Header
C_8	Update Indicator
C_9	No action
C_{10}	Inhibit display
C_{11}	No action
C_{12}-C_{14}	No action (may be programmed to enable and disable the chip)

(b) Viewdata

b_7-b_1	Cursor Control Bits
001 0001	Cursor ON } The two Control Words that make up these codes must be transmitted in numerical order in the same TS11 timeslot
001 0100	Cursor OFF }
F	Form feed or first appearance, Erases store defined by Sss, resets Reveal if Sss = Ddd
SP	Sets Picture/Text to picture (for initialization)
P	P Key presed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, Update.
M	Mix Mode
BC	Box Clock (Teletext only)
BH	Box Header (Teletext only)
	For M, BC and BH, the latches are set and reset by the appropriate bit
***	These are coded as follows:-
001	Picture/Text Key pressed
010	Reveal/Conceal Key pressed
011	½ Page Key pressed (Cycles Full, Top, Bottom, Full etc).
100	Update/Clear Key pressed
	For 001, 010, 011 and 100, the latches are toggled by the appropriate code
101	Rounding and Flashing OFF (Reset by P Key or new viewdata page)
111	Hold (not used by MR9735)

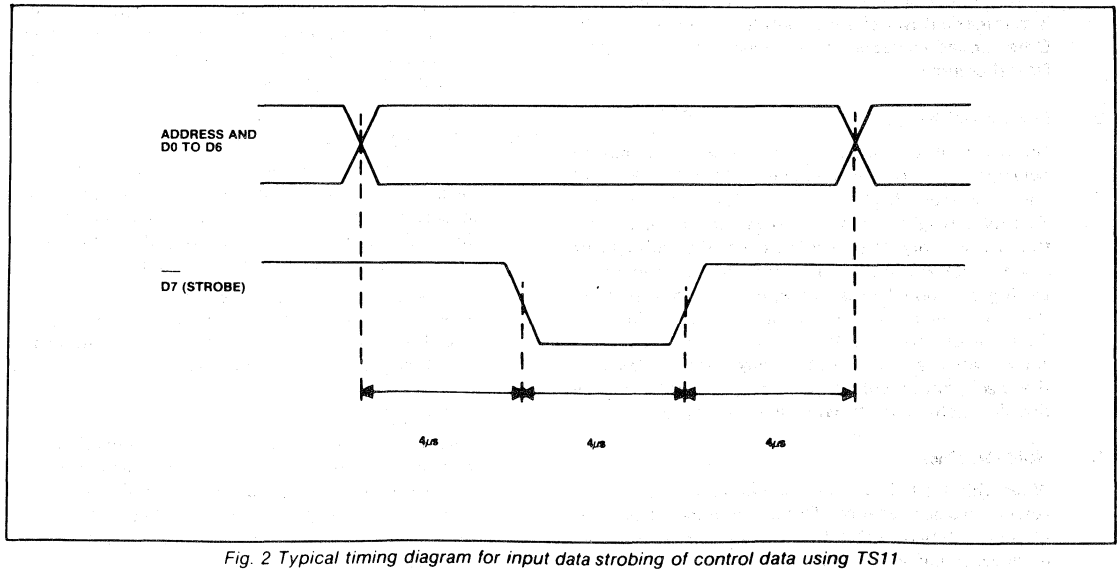


Fig. 2 Typical timing diagram for input data strobing of control data using TS11

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

1. **Character Set**

   The chip can display 96 Alphanumerics characters and 64 Graphics shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organised as:

   96 (characters) x 5 (dots) x 9 (lines) = 4320

   This can be programmed for different character fonts.

   The graphics shapes are determined directly from the bits of the character code (Fig.10).

2. **Display and Background Colour**

   The characters and the background can be displayed in one of seven colours. In addition the background may be black. This information is stored in two sets of three latches representing character and background colours.

3. **Conceal and Flash**

   Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

4. **Boxing**

   Text or graphics characters can be boxed into a normal video picture. While in Picture mode boxing is automatic if Newsflash or Sub-title (and Sss = Ddd). Other boxed characters may be manually revealed by Reveal command.

5. **Double Height**

   Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0–A9 so the same 40 addresses are read from another 10 times. Characters which are not double height are displayed as the background colour and the bottom(s) of the double height character(s) is (are) displayed.

6. **Hold Graphics**

   When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

7. **Special Graphics**

   While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 20 for each character in interlace mode (or 6 x 10 if not interlaced).

8. **Box Clock**

   When box clock is selected in picture mode and teletext the last eight characters of the page header are boxed in double height. To ensure that the "live" clock is displayed the store address is temporarily switched to that defined by Sss. This function is cleared in text mode.

9. **Box Header**

   When box header is selected in picture mode and teletext the page header is boxed in double height (not if bottom half of page selected).

10. **Half-page Operation**

    This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

11. **Monochrome Output/Mix Mode**

    In normal operation the Picture/$\overline{\text{Text}}$ Output is used to blank the normal picture information for boxing or displaying a page of text.

    In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Monochrome displays or printers. In this mode coloured backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

12. **Character Rounding**

    Characters are normally rounded by adding half dots to smooth diagonals. For normal height characters the extra TV lines made available by interlace are utilised for this and so if in non-interlace mode single height characters cannot be rounded.

    Character rounding can be inhibited totally by a signal from Control and in this mode, intended specifically for printers, flashing is also suppressed. Reset by P key or new Viewdata page.

13. **Cursor**

    The cursor is stored as the 8th bit of the appropriate character in the Data Store. When switched on it is displayed as a bar on the bottom line of the character rectangle flashing between foreground colour and black in anti-phase to normal flashing characters.

14. Non Interlaced Operation

When interlaced composite sync. is input to the chip it operates in normal Interlaced Mode and regenerates Interlaced composite sync.

If there is no incoming sync. the chip switches to the OFF hours mode.

If the Phase Comparator output is pulled high, e.g. 4k7 to Vcc, Interlaced Sync. is output. If the Phase Comparator output is held low Non Interlaced Sync. is output and character rounding for single height characters is inhibited.

SIGNAL DETECTION CRITERIA (For On Hours Operation)

The Video Generator detection circuitry for incoming sync. signals is designed to prevent mis-operation in the presence of noise. The criteria for detection is defined below.

1. Line Sync

The Comp. Video Input must be negative for greater than 3μs.

2. Frame Sync.

The Comp. Video Input must be negative for greater than 12μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

3. Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 12–39μs after Frame Sync Detection. This is used to lock the line counter.

4. On-Hours/Off-Hours Detection

The incoming line flyback and line sync pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/Frame occur for a period 350–1000ms the logic deems that a valid transmission is not being received and the chip switches 'OFF Hours''. If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Composite Sync is being received and the system goes 'ON Hours'.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Comp. Sync must be satisfied.

(a) Earliest back edge of LFB is 2μs after leading edge of line sync.

(b) Latest leading edge of LFB is 2μs after leading edge of line sync.

(c) Latest back edge of LFB is 12μs after leading edge of line sync.

The minimum length of the LFB pulse is 8μs.

5. 6MHz Display Oscillator

The 6MHz display oscillator must run fast in the OFF Hours mode but not so fast that the ON/OFF Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5kHz, the minimum offset is set by lock time criteria and would typically be +0.5kHz.

The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least −0.5kHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On chip D.C. restore is provided which allows simple interfacing to the television, either composite sync. signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system earth it is a.c. coupled to the chip.

A typical Interface Circuit is shown in Fig.3.

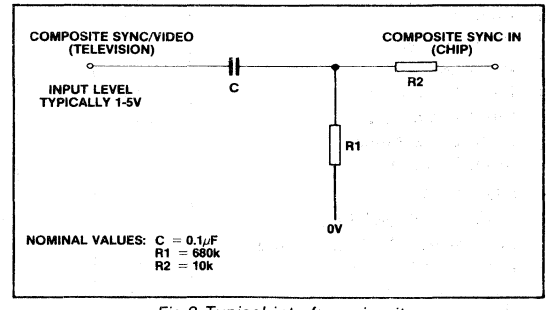


Fig.3 Typical interface circuit

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to Vss . . . . . –0.3 to +15V
Storage temperature range. . . . . –55°C to +150°C

*Exceeding these ratings could cause permanent damage
Functional operation is not guaranteed under these conditions
Operating ranges are specified below

Standard Conditions (unless otherwise indicated)

Vss = 0V (Substrate voltage)
Vcc = +5V ± 5%
Vdd = +10V ± 10%
Operating Temperature (Ta) = 0°C to +70°C
Clock Frequency 6.0MHz

Characteristic	Min	Typ**	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.4		Vcc	V	
Input Logic Low	Vss		0.8	V	
Input Current	10	25	100	μA	Vin = 5V
Comp. Sync.					
Input Logic High	1.0		Vcc	V	
Input Logic Low	–0.3		0.05	V	See Note 1
Input Capacitance			15	pF	Vin = 0V
Source Current		50		μA	Vin = 0V
6MHz					
Input Logic High	2.8		Vdd	V	
Input Logic Low	Vss		0.4	V	
Input Capacitance			25	pF	Vin = 0V
Mark to Space Ratio	40:60		60:40		
Frequency	1.0		6.5	MHz	
Input Leakage			10	μA	Vin = 10V
All Other Inputs					
Input Logic High	2.4		Vdd	V	
Input Logic Low	Vss		0.8	V	
Input Capacitance			15	pF	Vin = 0V
Input Leakage			10	μA	Vin = 10V
OUTPUTS					
Addresses, Read/$\overline{\text{Write}}$					
Store Select (Tri-State) (Note 2)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
Capacitance			15	pF	Vin = 0V
T rise T fall			200	ns	C load = 200pF
Leakage (Disabled)			10	μA	Vo = 0V, 5V
Time Slots (TS1, TS2)					
(Push-Pull)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
T rise T fall			200	ns	C load = 200pF
Comp. Sync (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 1.6mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			20	pF	V0 = 0V
Delay from Comp. Sync In.			1	μs	ON Hours only

Characteristic	Min	Typ**	Max	Units	Conditions
$\overline{\text{RSYNC}}$ (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0mA
Logic High Leakage			10	μA	Vo = 5V
Capacitance			15	pF	Vo = 0V
Phase Comparator (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0 mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			15	pF	Vo = 0V
R.G.B. Outputs Picture/Text Output (Tristate) (Note 2)					
Logic High Output	Vcc−1		Vcc	V	I source = 1mA
Logic Low Output	Vss		1	V	I sink. = 2mA
Capacitance			20	pF	Vin = 0V
T rise T fall (10%–90%)			30	ns	CL = 30pF
Differential T rise T fall			30	ns	CL = 30pF Note 3
19.2kHz, 1.2kHz Outputs					
Logic High Output	2.4		Vcc	V	Ioh = -30μA.
Logic Low Output	Vss	0.2	0.5	V	Iol = 300μA
T rise T fall			1	μs	C load = 100pF
POWER					
Vcc Supply		25	40	mA	Vcc = 5V
Vdd Supply		40	66	mA	Vdd = 10V

Note 1: Voltages below −0.3 volts should be current limited to 1mA.

Note 2: All tristated when $\overline{\text{Chip Select}}$ = Vcc. R.G.B. outputs also tristated when displaying picture and not mixed.

Note 3: Picture/$\overline{\text{Text}}$ matched in mix mode only.

** Typical values are at +25°C and nominal voltages.

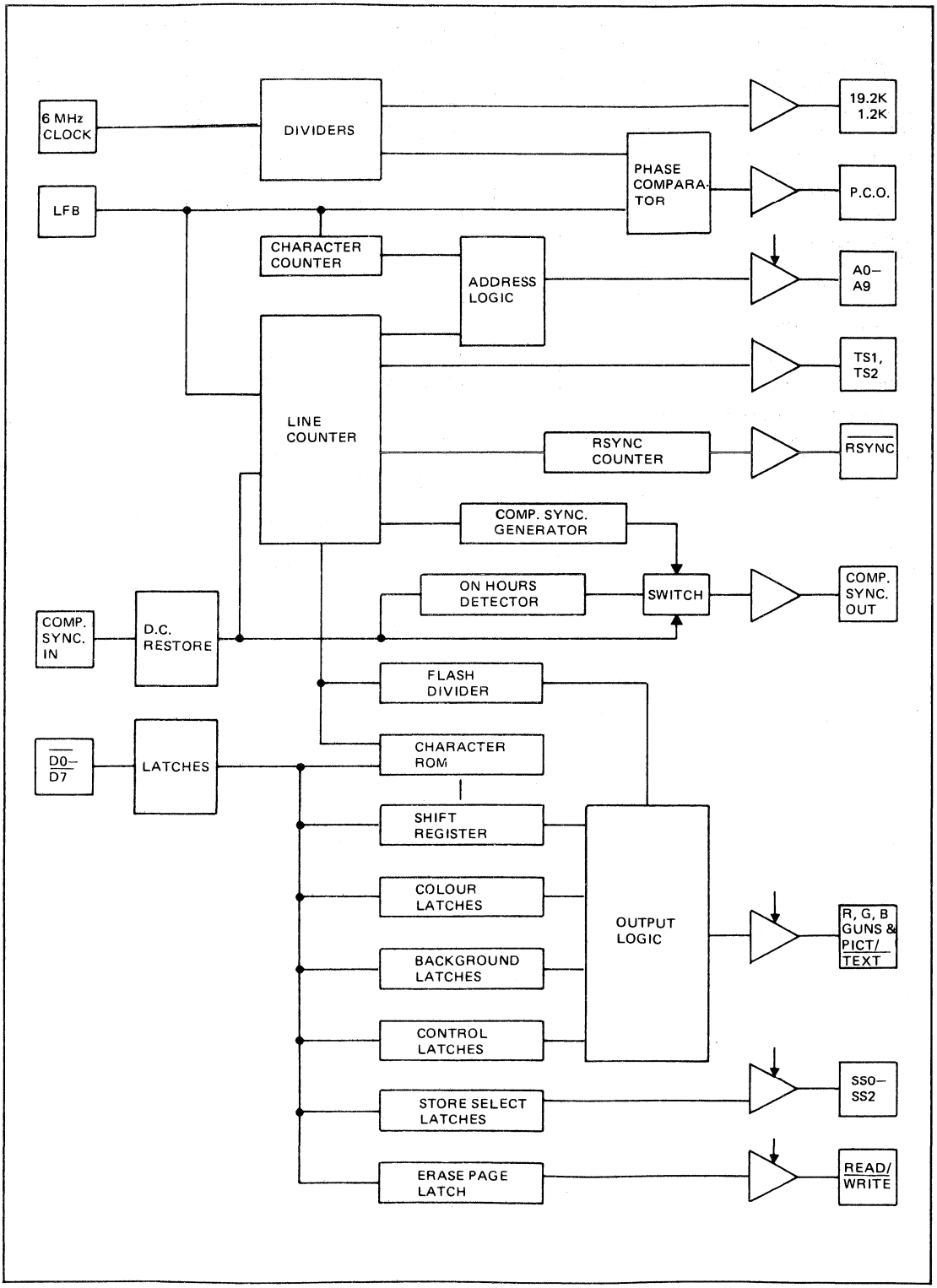


Fig.4 Block diagram

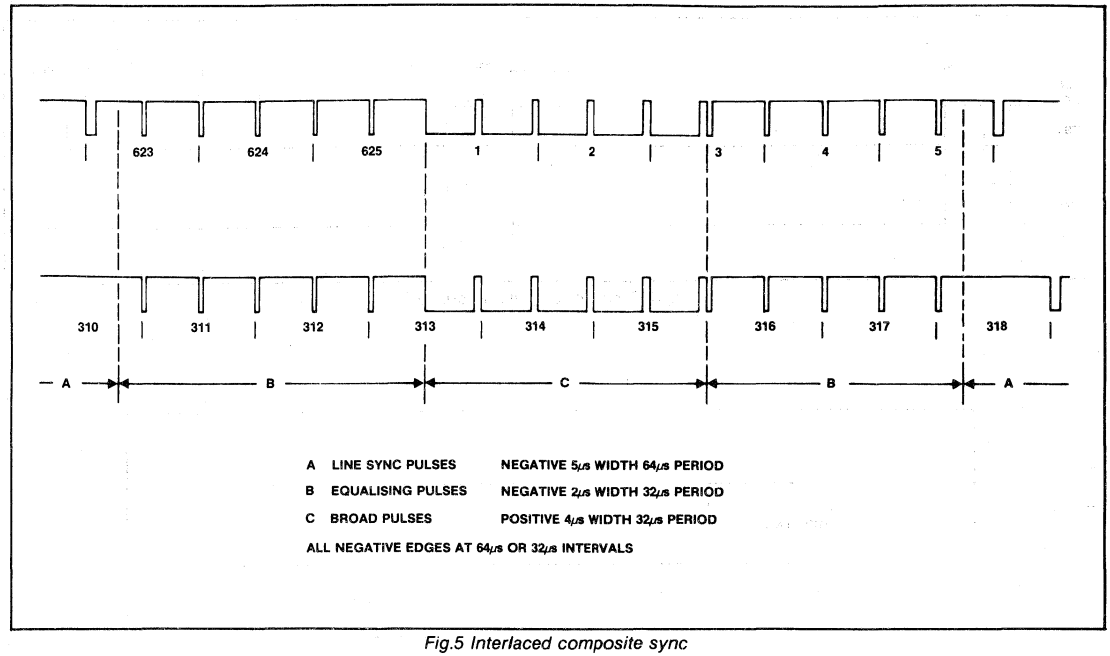


Fig.5 Interlaced composite sync

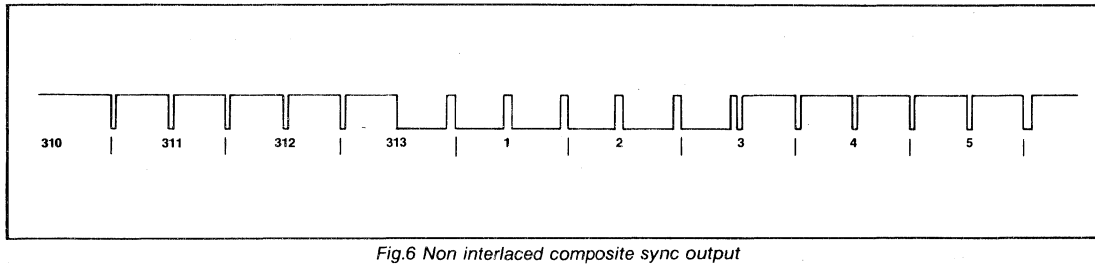


Fig.6 Non interlaced composite sync output

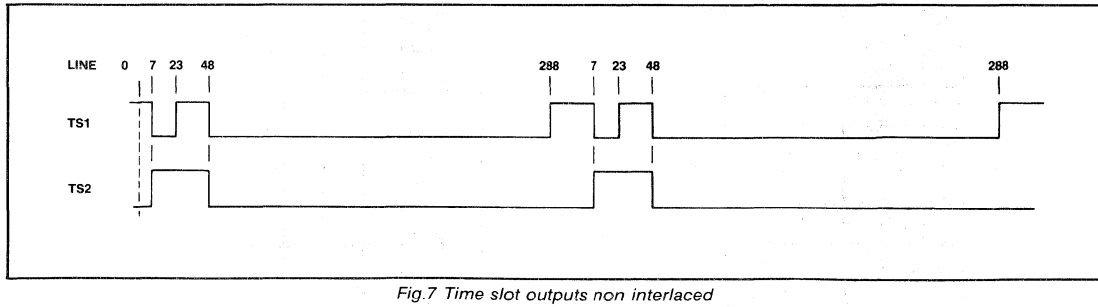


Fig.7 Time slot outputs non interlaced

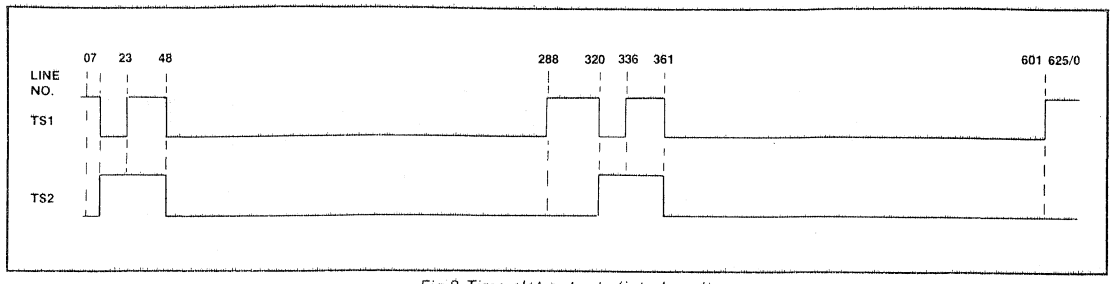


Fig.8 Time slot outputs (interlaced)

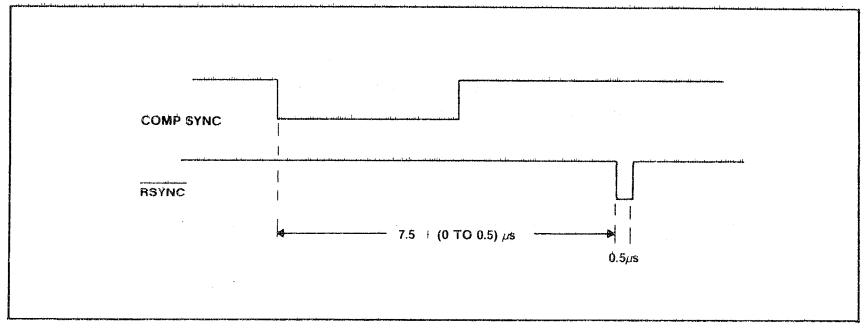


Fig.9 RSYNC timing

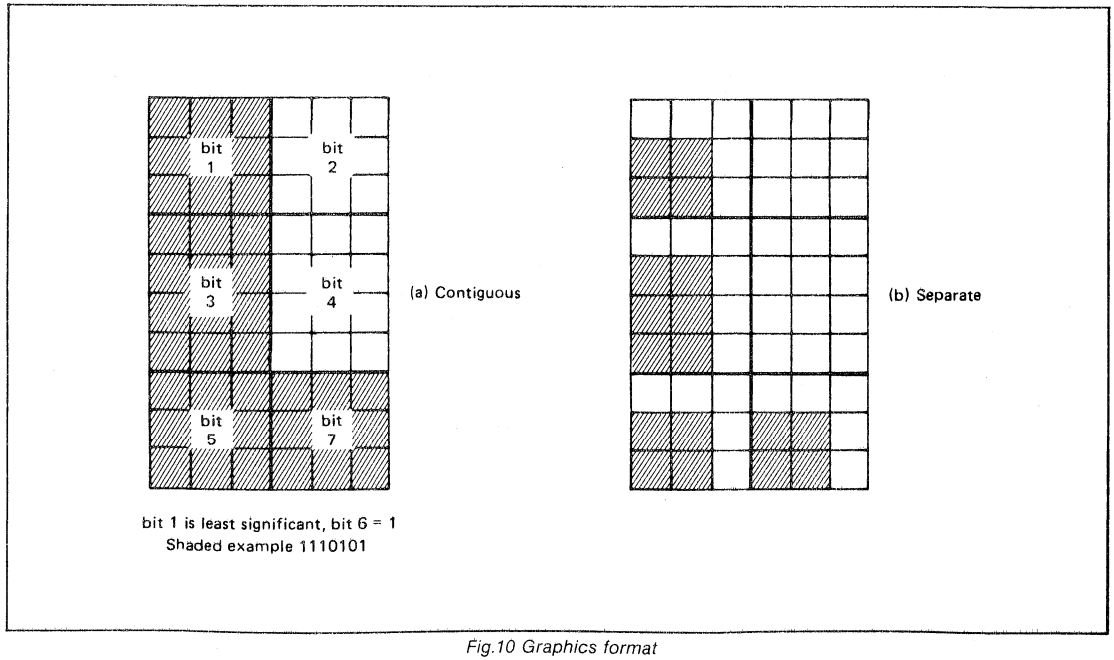


Fig.10 Graphics format

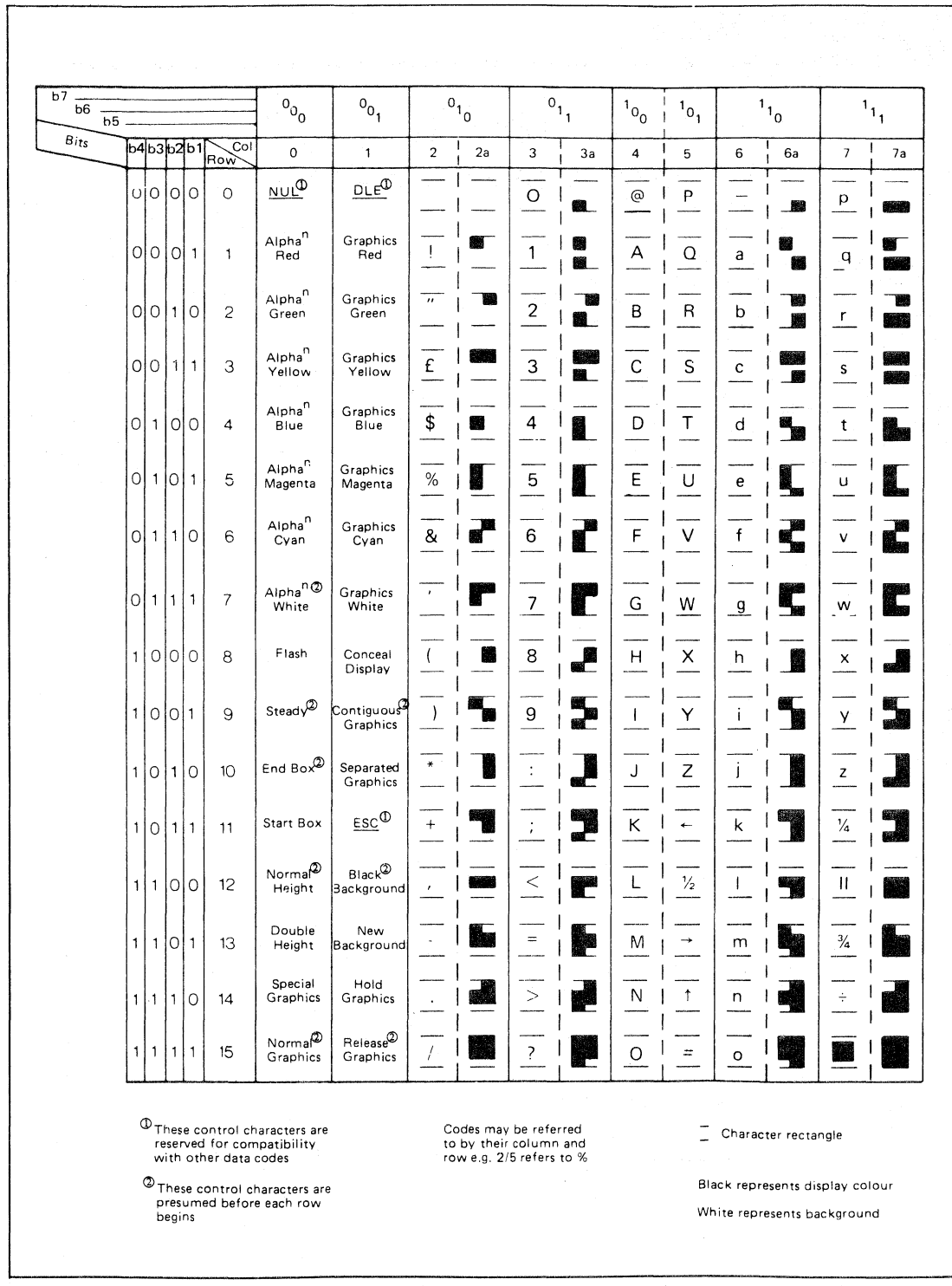


Fig.11 Teletext character codes (002 character set)

PLESSEY
Semiconductors

MV500

REMOTE CONTROL TRANSMITTER

The MV500 remote control transmitter has been introduced to complement the existing range of remote control devices. Together with a simple low cost keypad, an infra-red diode and a transistor, the MV500 forms a complete transmitter for remote control data. The device uses pulse position modulation (PPM) without a carrier and is therefore best suited to infra-red or direct wire link applications. CMOS technology is used which allows low power battery operation down to 3 volts. One of three output data rates may be selected, all timing being derived from a low cost ceramic resonator. The MV500 may be used with the MV601 remote control receiver or decoded directly by a microprocessor.

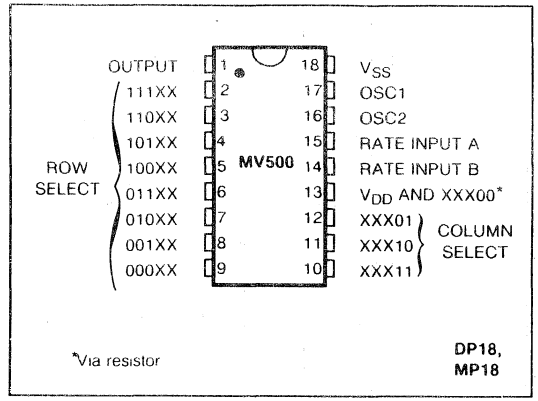


Fig.1 Pin Connections - Top View

FEATURES

- Very Low Power Requirements
- 3 to 9 Volt Operation
- Low Cost Ceramic Resonator
- Selectable Data Rates
- Single Pole Key Matrix
- Few External Components
- Code Synchronising Pulses

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5V to 11V
Input voltage (all pins)	-0.5V to VDD + 0.5V
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

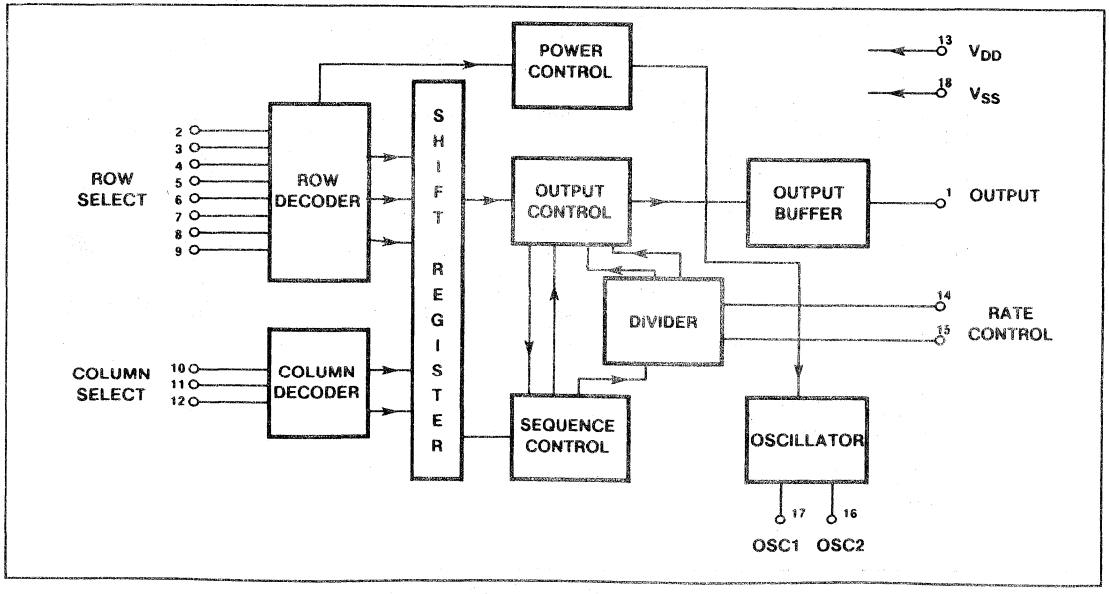


Fig 2 MV500 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +3V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Operating supply current	13		0.5	2	mA	Circuit fig.4
Standby supply current	13		0.3	2	µA	All inputs open circuit V_{DD} = 9V, T_{amb} = 25°C
Output source current	1	50	100	200	mA	V_{DD} = 6V, V_{OH} = 1V
		10	25	50	mA	V_{DD} = 3V, V_{OH} = 1V
Keyboard contact resistance	2-12					
Closed		0		20	kΩ	
Open		100		∞	kΩ	
Oscillator Frequency	16,17	400		1000	kHz	

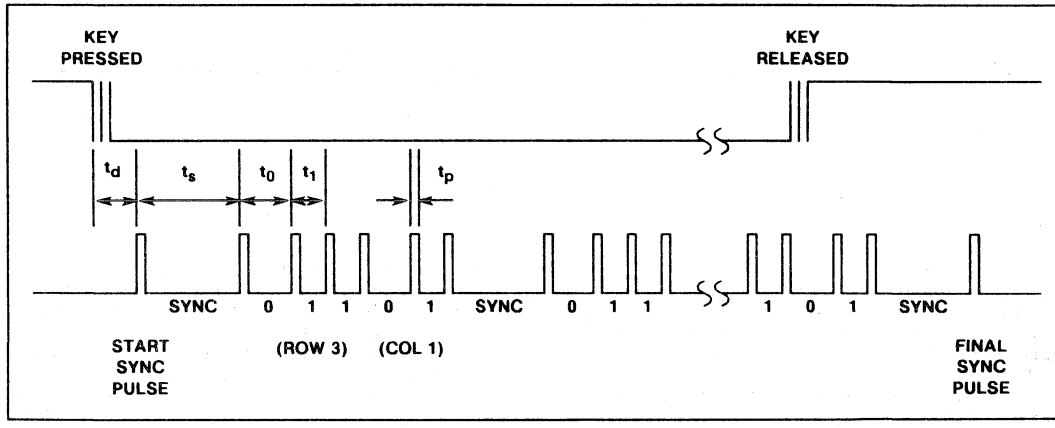


Fig 3 PPM Data Timing

TIMING

RATE INPUTS		RATE VALUE 'T' (CLOCK CYCLES)
B	A	
0	0	OUTPUT INHIBITED
0	1	2048
1	0	1024
1	1	512

Table 1 Rate Control

DELAY TIME, t_d = 1024 CLOCK CYCLES (min)

SYNC TIME, t_s = 6T (see Table 1)

LOGIC 0 TIME, t_0 = 3T

LOGIC 1 TIME, t_1 = 2T

PULSE WIDTH, t_p = 8 CLOCK CYCLES

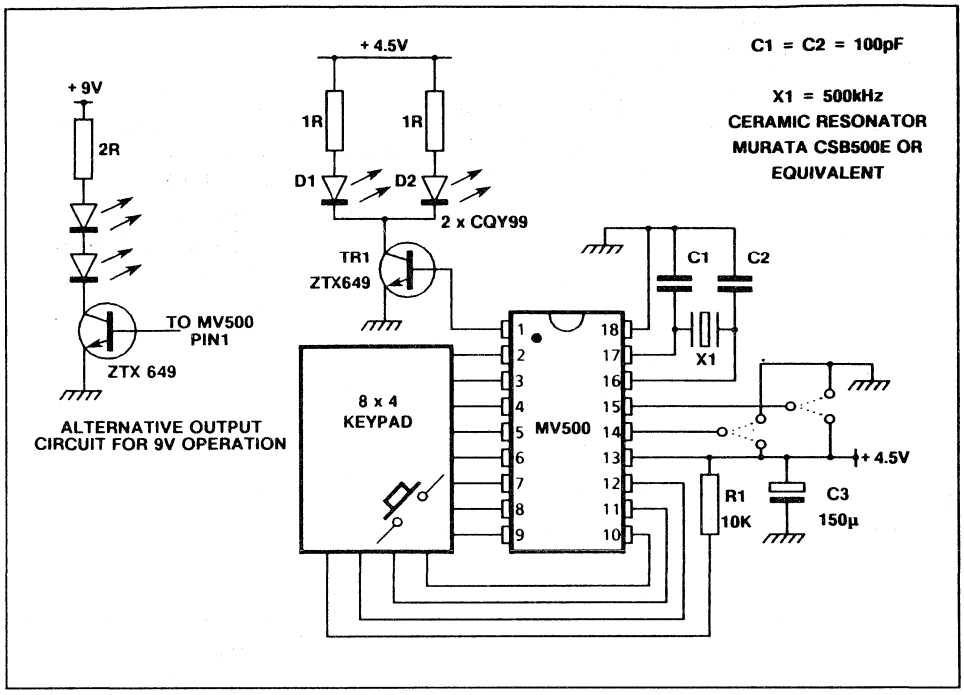


Fig 4 Infra-red Application Circuit

OPERATION

The circuit diagram of Fig.4 shows a typical infra-red transmitter operating from a 4.5V supply. When no key is pressed, the MV500 remains in its power down mode, isolating the oscillator and most of the logic from the supply, thus minimising the drain on the battery. The output is held low.

The device may be activated in one of two ways:-

a) one or both of the RATE inputs is held high, then a key switch is closed connecting any COLUMN to any ROW, or

b) any COLUMN and ROW are connected, then one or both of the RATE inputs is taken high.

Once activated, power is applied to the rest of the device, the oscillator started and a delay imposed before any change at the output occurs. After this time, an initial sync pulse is transmitted, followed by the code word, which is repeated for as long as the key remains pressed. When the key is released, the word being transmitted is completed before the device enters its standby mode again.

Taking both RATE inputs low will also force the device into its power down state at the end of the current word. A final sync pulse is always added at the end of the last word to be transmitted (Fig. 3).

When the transmitter is operated from a 9V battery, two infra-red LEDs may be used in series as shown inset in Fig. 4. At other voltages, consideration must be given to the arrangement of diodes used and a small resistance (1 or 2Ω) may be necessary in series with the diodes to limit the current. It should be noted that using two diodes in parallel increases the current drawn from the battery at each pulse. A significant increase in range may be obtained by using a plated plastic parabolic reflector in conjunction with one or two diodes, rather than simply increasing the number or power of the diodes used.

Transistor TR1 should be chosen to have high current gain and fast switching speeds at the current levels relevant to the diode arrangement used.

MV601

REMOTE CONTROL RECEIVER

The MV601 is a remote control receiver designed to operate in conjunction with the MV500 transmitter. A five bit tri-state binary output corresponding to the 32 codes available from the MV500 is provided together with data ready and output enable signals, allowing a simple interface to a microprocessor. A ceramic resonator and two rate inputs set the data rate to correspond to that produced by the MV500.

FEATURES

- High Noise Immunity
- 5V Operation
- Very Low Supply Current
- Momentary or Latched Operation
- Tri-State Outputs
- Ceramic Resonator and Data Rate Inputs to match MV500

APPLICATIONS

- Remote Control Interface to Microprocessor
- Industrial and Consumer Remote Control

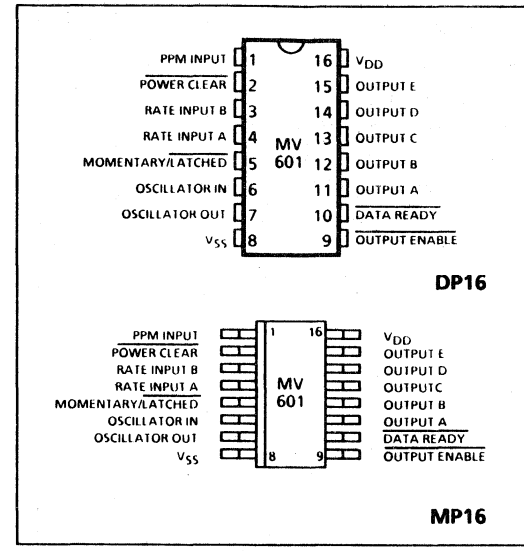


Fig 1 Pin Connections - top view

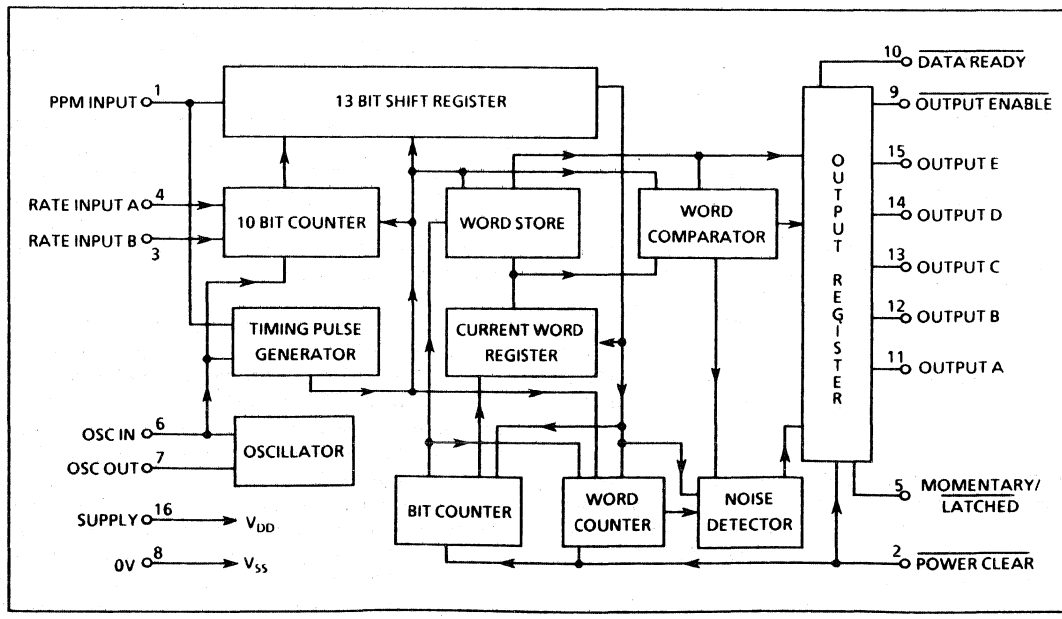


Fig.2 MV601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
INPUTS						
OSCIN, RATE A, RATE B, MOM / LAT, OEN	6, 4, 3, 5, 9					
Input low voltage (V_{IL})				V_{DD} / 3		
Input high voltage (V_{IH})		VDD ×2/3				
PPM, CLEAR	1, 2					
Input low voltage (V_{IL})				1.0	V	VDD = 5.0V
Input high voltage (V_{IH})		2.0			V	
Threshold voltage rising			1.85		V	
Threshold voltage falling			1.05		V	
CLEAR, RATE A , RATE B	2, 4, 3					
Input low current			-33	-100	µA	Nom. 150K pullup resistor
All other inputs except OSCIN Input current	1, 5, 9			±2.5	µA	V_{IN} = Vss -0.3V to V_{DD} +0.3V
OSCIN	6					
Input current				±10	µA	V_{IN} = Vss -0.3V to V_{DD} +0.3V
OUTPUTS						
A - E, DATA READY						
Output low current (sink)		13	26		mA	V_{OL} = 0.4V
Output high current (source)		-21	-45		mA	V_{OH} = 2.4V
Output leakage current (A-E)				±10	µA	VO V_{SS} -0.3 to V_{DD} + 0.3V pin 9 = V_{DD}
OSCOUT						
Output low voltage (sink)		1.0			mA	V_{IO} = 0.3V
Output high current (source)		-1.0			mA	V_{OH} = V_{DD} 0.3V

OPERATING NOTES

The MV601 is designed to operate in conjunction with the MV500 transmitter. When the rate inputs of MV500 and MV601 are programmed with the same binary input code and matched ceramic resonator frequencies are used (within 4%), the outputs of the MV601 will be set to the value of the PPM code transmitted. Two identical valid words must be received before an output response. A data ready signal, set after the output data has settled may be used to strobe data into an external register or generate an interrupt to a microprocessor.

When used in infra red systems, the PPM input will usually be derived from the output of an SL486 infra red amplifier, but direct connection to the transmitter is also possible. The PPM input is insensitive to pulse width.

The power clear input is generally connected to an external capacitor which holds the input momentarily low ensuring a reset of the outputs and internal logic at power on. The circuit can be reset at any time by taking the power clear input low.

The rate inputs have nominal 150K ohm pull up resistors and may therefore be left open circuit when a high input is required.

When more than 32 codes are required, the rate inputs on the MV500 transmitter can be switched and 2 or 3 MV601 circuits wired in parallel to the PPM signal. Only the MV601 with rate inputs identical to the transmitter will respond. An alternative method giving 64 possible codes from only one MV601 is shown in figure 7. The fastest and slowest rate settings from the transmitter should be used. In this circuit the three transistors produce a DC level dependent on the rate of the received PPM data. The DC level is used to provide the F output bit and to automatically switch the rate B input to the MV601 to correspond with the transmitter.

PIN FUNCTIONS

1. **PPM Input**
The serial PPM data is connected here. Pulse width is not critical but must remain high or low for at least one clock cycle.

2. **Power Clear**
A logic low resets the output register and internal logic ensuring full noise immunity from switch on. A capacitor to V_{SS} will normally be connected. A 150k (nom) resistor to V_{DD} is provided so that the input may be left open circuit if required.

3. **Rate Input B**
Thls input controls the received data rate according to table 1. Input state must match that on MV500. A 150k (nom) resistor pull up to V_{DD} is provided so that the input may be left open circuit if required.

4. **Rate Input A**
As pin 3.

5. **Momentary/Latched Input**
Controls the operational mode of the output register. When low, data will be retained at the output until updated by a newly validated code. When high, the data will only remain at the outputs whilst the valid code is present at the PPM input.

6. **Oscillator In**
The input to the oscillator circuit. A Pierce oscillator is formed by a ceramic resonator connected to pin 7 and capacitor connected to ground.

7. **Oscillator Out**
The output of the oscillator circuit. A capacitor connected to ground completes the Pierce oscillator circuit.

8. **V_{SS}**
The negative supply pin.

9. **Output Enable**
A logic low enables the A, B, C, D and E outputs. A logic high switches the output transistors off, providing a high impedance state.

10. **Data Ready**
Set low when valid data is present at the outputs.

11. **Output A**
Tri-state output set to the binary equivalent of the PPM input data.

12. **Output B**
As pin 11.

13. **Output C**
As pin 11.

14. **Output D**
As pin 11.

15. **Output E**
As pin 11.

16. **V_{DD}**
The positive supply pin.

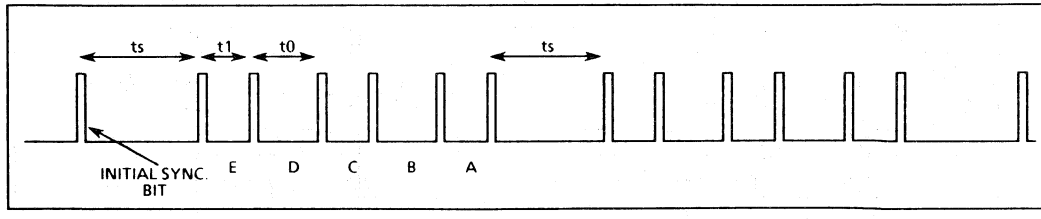


Fig.3 Typical Received PPM Data

RATE INPUTS		CLOCK CYCLES		
B	A	t1	t0	ts
0	0	NV	NV	NV
0	1	4096	6144	12288
1	0	2048	3072	6144
1	1	1024	1536	3072

Table 1 Rate control inputs

NV = NOT VALID

NOTE: RATE INPUTS SHOULD MATCH THOSE ON MV500

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	+ 7V
Input Voltage	V_{DD} + 0.3V to V_{SS}-0.3V
Operating Temperature	0°C to + 70°C
Storage Temperature	-55°C to + 125°C
Output Sink and Source Current	50mA
Humidity	85%

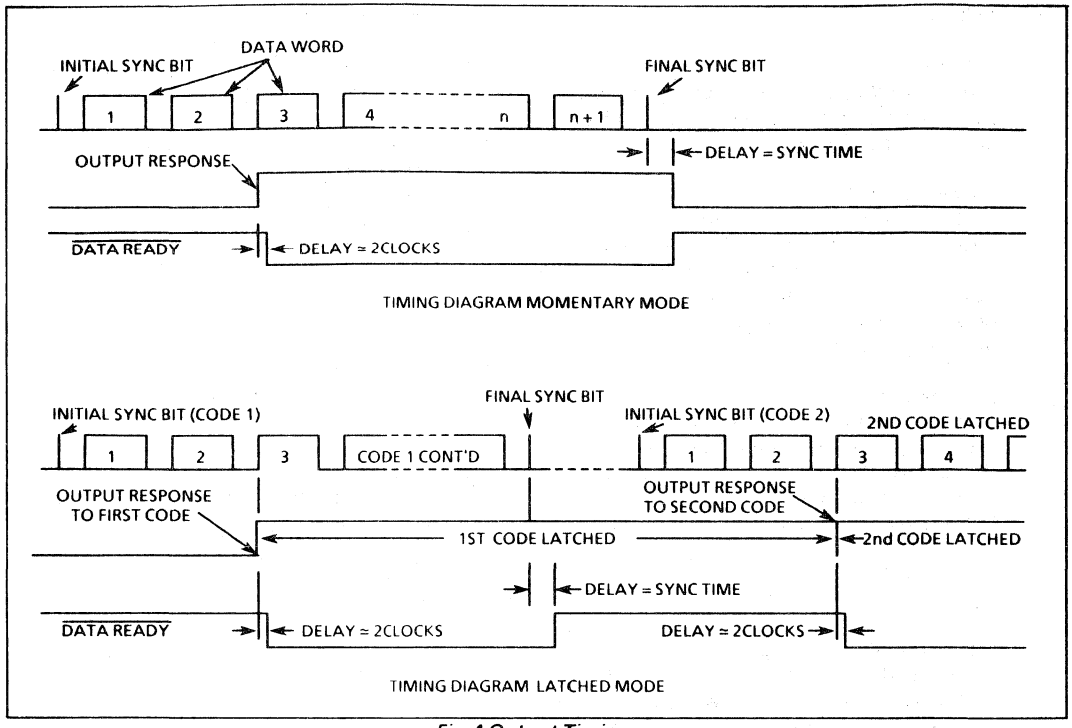


Fig.4 Output Timing

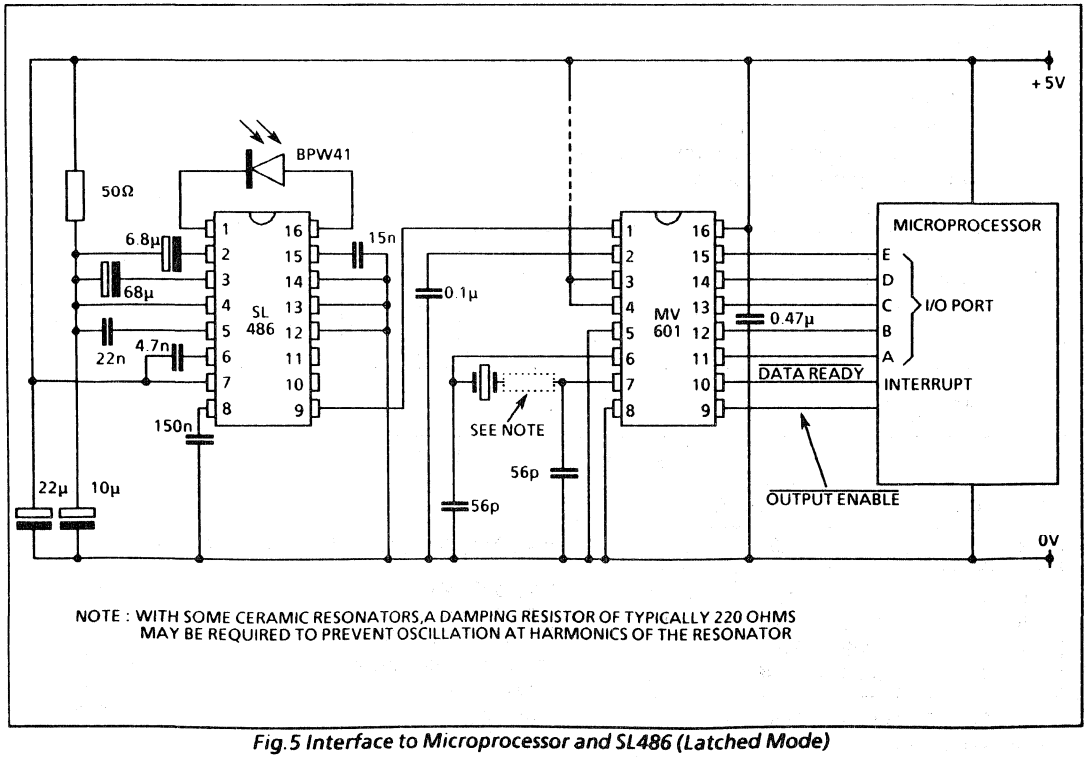


Fig.5 Interface to Microprocessor and SL486 (Latched Mode)

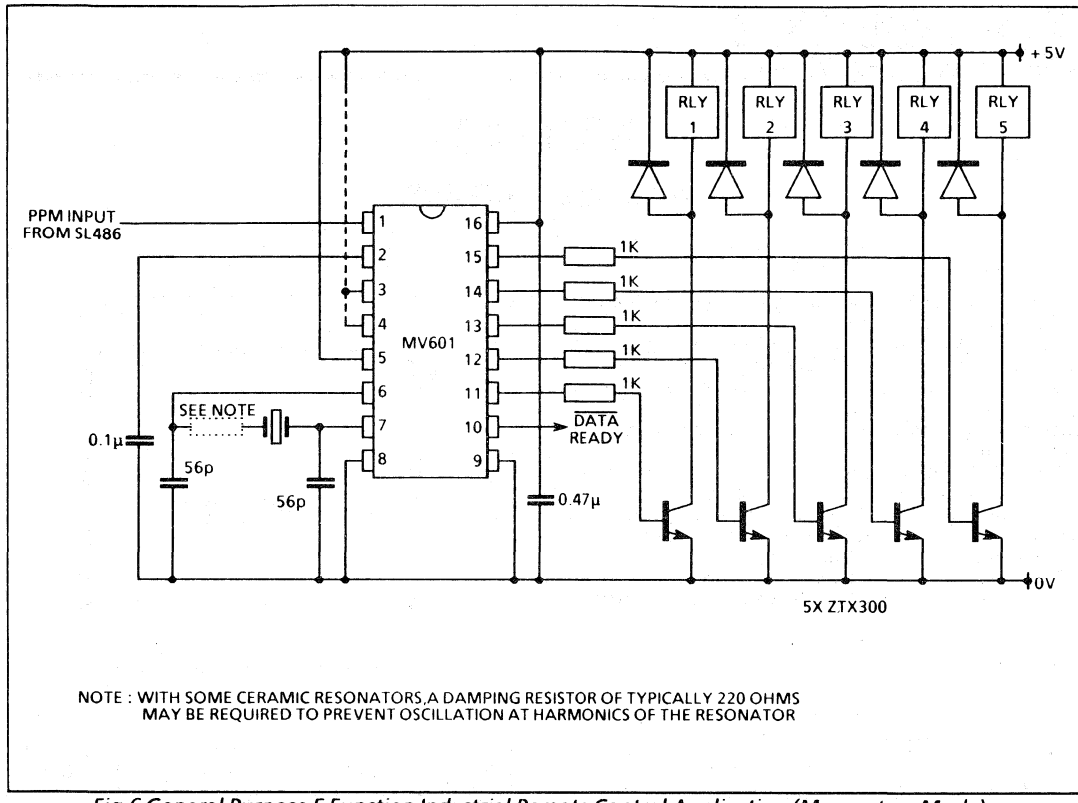


Fig.6 General Purpose 5 Function Industrial Remote Control Application (Momentary Mode)

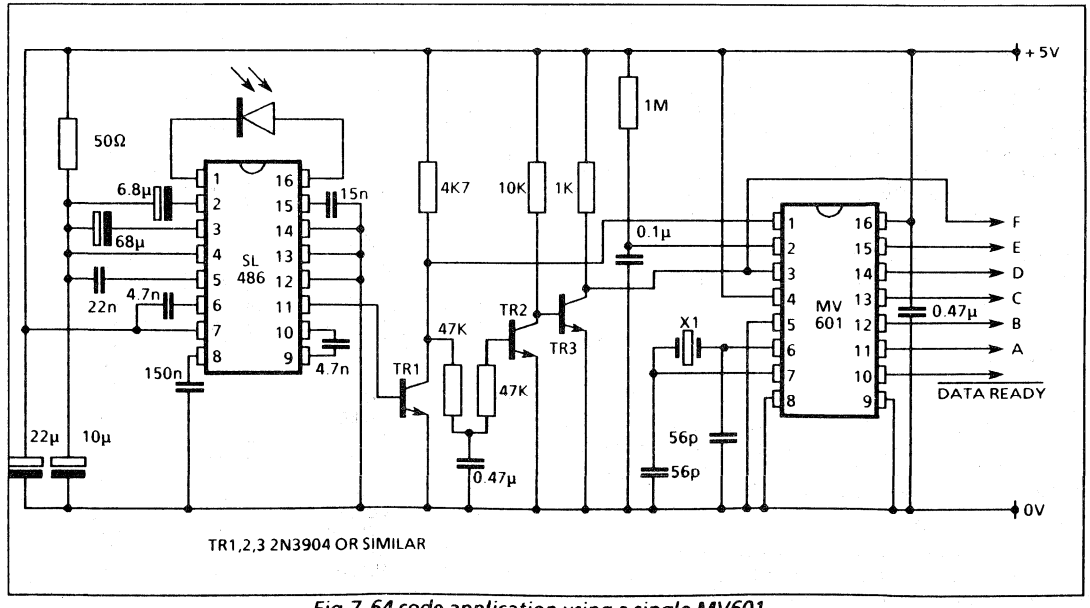


Fig.7 64 code application using a single MV601

PLESSEY
Semiconductors

MV1710

MAC VIDEO CIRCUIT

The 1710 is the video circuit for the Nordic VLSI C/D/D2 MAC packet receiver chipset.

The MV1710 video circuit receives the digital MAC vision signal from an 8 bit, 20.25MHz, A/D convertor. The vision signal is decompressed and descrambled according to the EBU - standard, [ref.1]. Frame and line synchronising signals are received from the MV1720 Control Chip.

The MV1710 is programmable through the configuration chain, which is set up by the microcomputer. The programmable features are scrambling method, descrambling control word, pan-constant, output rate, relative output delay and blanking level.

The video output consists of 8 bit digital luminance and UV colour difference signals at frequencies of 13.5MHz and 6.75MHz respectively.

FEATURES

- Double or Single Cut Line Rotation Descrambling
- 4:3 or 16:9 Aspect Ratio
- Separate Sync and Blanking Signals
- Programmable Through the Configuration Chain

DESCRIPTION OF THE SIMPLIFIED BLOCK DIAGRAM

Descrambler

The descrambler controls the video ram write address calculation. The calculation can be done in three different ways, depending on the content of the Vconf-field in the configuration chain. The cases are: no scrambling, double cut scrambling and single cut scrambling. In the scrambling case, the control word is read from the configuraton register into a PRBS generator and the cut points calculated. Together with a sample counter, this is sufficient to set the ram write enable for luminance and chrominance at the correct time interval in each line.

Write controller

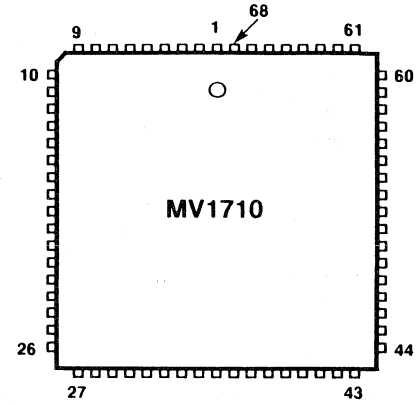
The write controller administrates which ram to write to in each line.

Read controller

The read controller administrates which ram to read from in each line. Each ram is read from address 0 to end within a line. If the pan option is set, reading is started at a variable address, and only 3/4 of the line is read out.

Luminance rams

Two rams are included, each capable of storing one line of luminance (697 bytes). During a line, input video is written to one ram, and output Y is read from the other ram. In the next line, the first ram is read and the second ram is written. This procedure is repeated for each two lines.



Pin	Function	Pin	Function
1	U7	35	VBLANK
2	V_{SS}	36	V_{SS}
3	U3	37	BLACKSTRB
4	U2	38	CDATAIN
5	V_{DD}	39	V_{DD}
6	V0	40	CSTRB
7	V1	41	EFCNT
8	V_{SS}	42	F
9	V4	43	V_{SS}
10	V5	44	L
11	V6	45	F3
12	V7	46	CUTBIT
13	V_{SS}	47	CLK2
14	V3	48	V_{SS}
15	V2	49	CKL13
16	V_{DD}	50	CDATAOUT
17	VIDEO0	51	V_{DD}
18	VIDEO1	52	Y0
19	V_{SS}	53	Y1
20	VIDEO2	54	V_{SS}
21	VIDEO3	55	Y7
22	VIDEO4	56	Y6
23	VIDEO5	57	Y5
24	V_{SS}	58	Y4
25	VIDEO6	59	V_{SS}
26	VIDEO7	60	Y3
27	V_{DD}	61	Y2
28	CLK1	62	V_{DD}
29	V_{SS}	63	U0
30	COMPSYNC	64	U1
31	LUMEN	65	V_{SS}
32	COLEN	66	U4
33	V_{DD}	67	U5
34	HBLANK	68	U6

Fig.1 Pin connections - top view

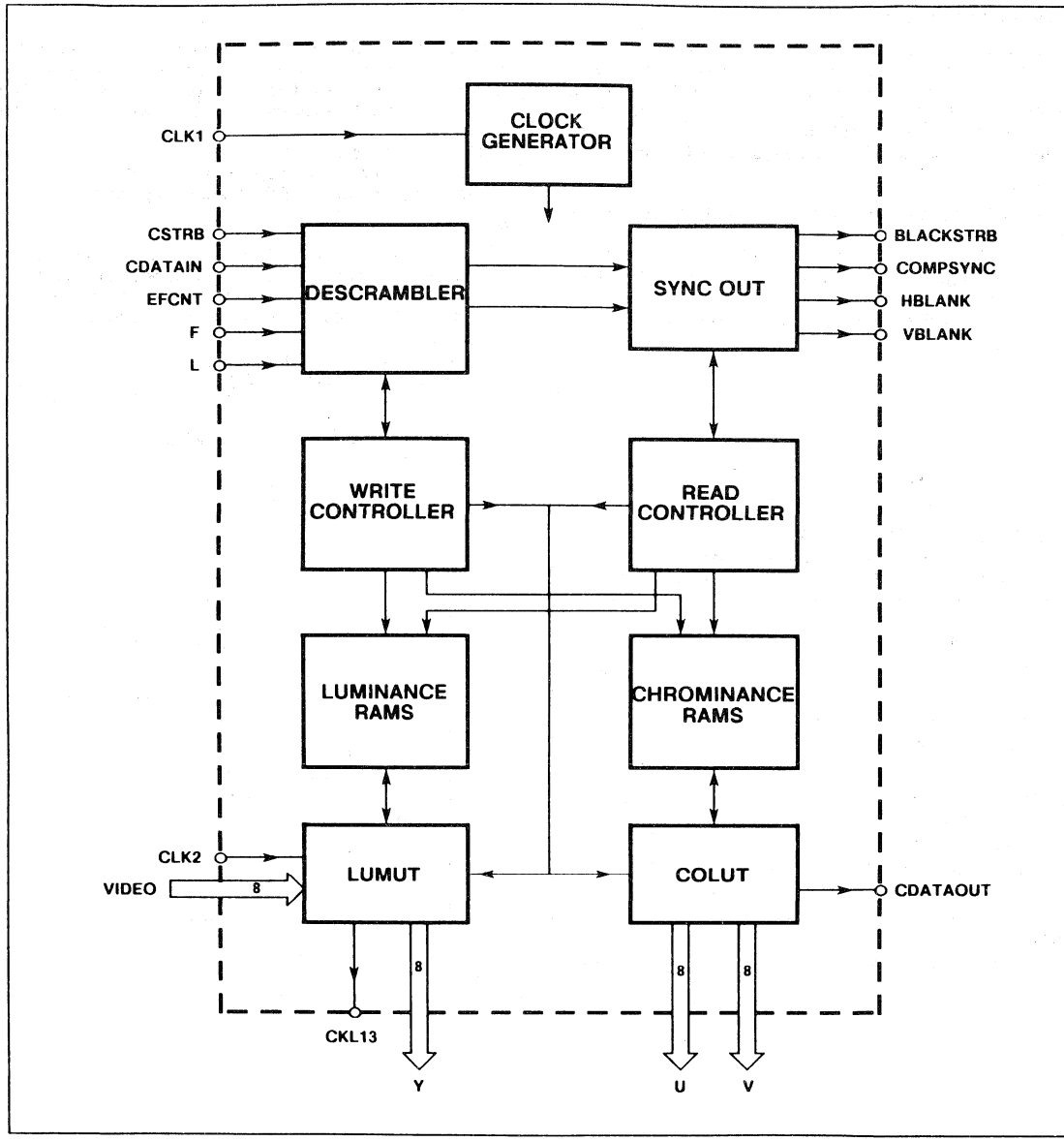


Fig.2 Simplified block diagram for MV1710 MAC video chip

ABSOLUTE MAXIMUM RATINGS
(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

Chrominance rams

Four chrominance rams are included, each capable of storing one line of chrominance(349 bytes). During a line, input video is written to one ram and output U and V is read from the other three rams, one colour component directly, and the other component averaged from the two other rams. This procedure is repeated for each four lines.

Lumut

Lumut controls the Y luminance output. Two options exist:

Y at 13.5 MHz, 4:3 aspect ratio picture. The 13.5MHz may be generated internally or provided by the CLK2 input pin.

Y at 10.125MHz, 16:9 aspect ratio picture.

Colut

Colut controls the U and V colour output. U and V are transmitted on every second line, and the missing line is reconstructed by calculating the average between the line before and after. U is received on odd lines and V on even lines.

The two options are:

U, V at 6.75MHz, 4:3 aspect ratio picture.

U, V at 5.625 MHz, 16:9 aspect ratio picture.

Syncout

Syncout generates the following synchronising signals:

Blackstrb, a strobe signal for the black level reference.

Composite sync, a negative line pulse for each line, and 5 field pulses and equalising pulses for change of field.

H blank, horizontal blanking signal.

V blank, vertical blanking signal.

(ref . 1) MAC packet family specifications
EBU No. Tech 3258-E

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	
Clock 2 frequency		42	MHz	
Setup time (all inputs) See note 1	0		nS	

NOTE

1. This figure is valid for all data inputs relative to the positive edge of CLK1.

PLESSEY
Semiconductors

MV1720

MAC CONTROL CIRCUIT

The main functions of the MV1720 Controller for the Nordic VLSI C/D/D2/MAC/packet receiver are to decode the bit-stream from the demodulator, and to serve as an interface between the receiver microcomputer and the chip set.

The MV1720 synchronises on the frame structure by recognising line and frame sync, and generates timing signals which control the operation of other modules. Data is spectrum descrambled, and data in the selected bursts is de-interleaved and formed into full packets. Packet headers and optionally the data part are corrected and routed to a common output for sound and data.

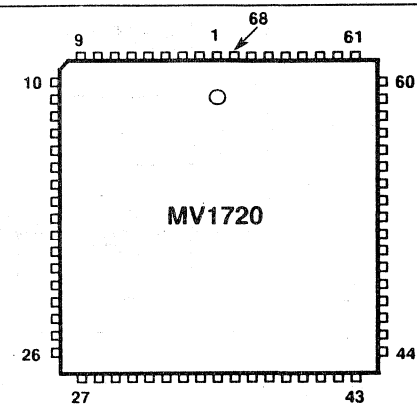
SI-packets (addr 0), SMM, CMM or AUX packets can also be routed to a separate packet buffer which can be read from the receiver microcomputer. CMM address recognition is supported. Golay encoded packets are decoded, corrected and optionally compressed before they are stored in the packet buffer.

The MV1720 has a general purpose microprocessor interface that is compatible with most microprocessors or microcomputers. The data rate is controlled by the microcomputer and can be up to 2 Mbyte/sec.

Line 625 is decoded and majority voted for repeated and static data fields. The resultant data is output as a special 'packet' with separate strobe signals. This packet can also be read via the packet buffer.

FEATURES

- Programmable Sync Acquisition and Generation
- De-interleaving of Two Independent Subframes
- Hardware Golay Decoding and Correction for CMM, SMM and SI-Packets (Programmable)
- Programmable Packet Address Selection
- Programmable SMM Packet Selection
- Programmable CMM Packets Selection with Unique Customer Address and Shared Address (according to the EBU Spec) (ref.1)
- Programmable CMM Packet Selection with Collective Address and Entire Audience (Proposed EBU Spec Extension)
- High-Speed Microprocessor Interface supporting most Microprocessors or Microcomputers



Pin	Function	Pin	Function
1	V_{SS}	35	CE
2	V_{DD}	36	V_{SS}
3	FS2	37	MCD4
4	FS1	38	MCD5
5	RESET	39	V_{DD}
6	DATAIN	40	MCD6
7	CLK1	41	MCD7
8	V_{SS}	42	NC
9	CDATAOUT	43	NC
10	NC	44	NC
11	TEST	45	TEST
12	CSTRB	46	RS
13	V_{DD}	47	MCLK
14	CLKPLL	48	IRQ
15	CLAMP	49	VAL
16	CDATAIN	50	PDATA
17	L	51	V_{SS}
18	F	52	SPINF
19	TEST 1	53	SFRQ
20	LSYNC	54	V_{DD}
21	V_{SS}	55	PACKST
22	CLKD 2	56	PACKDT
23	RD	57	V_{SS}
24	WR	58	SIV
25	TEST	59	TEST
26	NC	60	NC
27	NC	61	NC
28	TEST	62	SB2
29	V_{SS}	63	SB1
30	MCD0	64	TTV
31	MCD1	65	DISD
32	MCD2	66	DATAOUT
33	V_{DD}	67	ML625
34	MCD3	68	EFCNT

Fig.1 Pin connections - top view

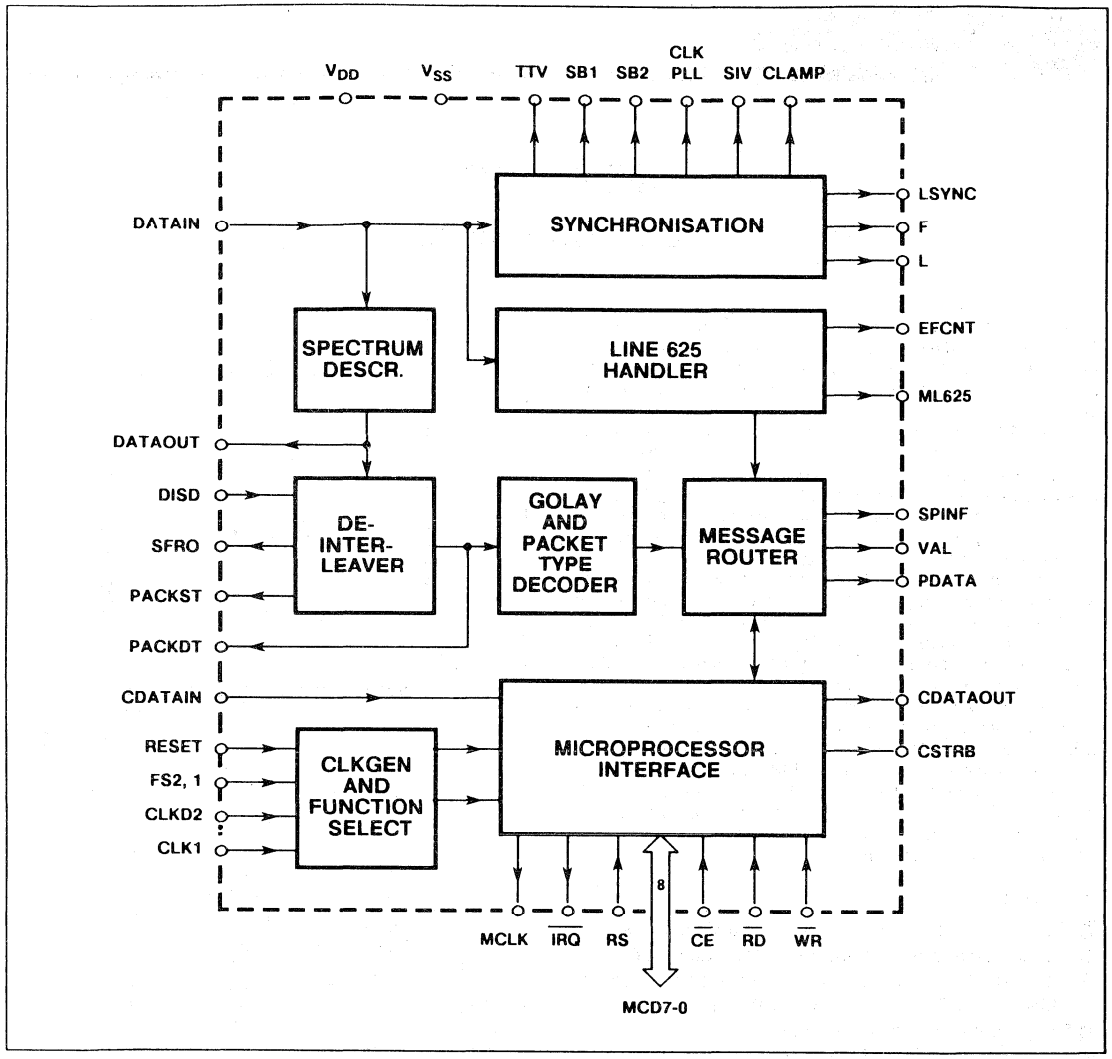


Fig.2 Simplified block diagram for MV1720 MAC/packet control chip

DESCRIPTION OF THE SIMPLIFIED BLOCK DIAGRAM

Synchronisation

This module monitors the input data from the receiver, looking for the line sync words (LSW) appearing in the beginning of each line. There are two such alternating words named W1 and W2. The module first looks for 3 consecutive alternating LSWs, and enters 'local sync' when this occurs. Afterwards it expects to find the boundary between an even- and odd-numbered frame within 1250 lines, i.e. two frame periods.

When searching for the LSW, it will accept 1 bit error before local sync is obtained, after which it switches to accepting 2 bit errors. After entering local sync it may loose 15 consecutive LSWs before sync is assumed to be lost.

When detecting the frame boundary the F and L output signals both change from low to high, and continue to toggle according to the specification. The position where these signals change can be programmed via the microcomputer interface.

This module also generates the signals SB1 and SB2 (flagging two selectable data bursts (subframes) on DATAOUT), SIV (service identification in line 625 on DATAOUT), CLAMP (clamp period for video), TTV (lines containing Teletext), and LSYNC (active after each LSW detected).

Spectrum Descrambler

The descrambler contains a 15-bit pseudo-random generator. It starts after LSW is detected in line 1 and runs continuously until line 625 when it is initialised (set to ones).

The DATAIN signal is XOR'ed with the output from the generator. The output from the descrambler is available on the DATAOUT pin of the MV1720.

De-Interleaver

This module consists of four 751 bit buffers and a sequencer handling input and output. Each buffer is a 751 x 1 bit static RAM. Incoming data arrives in bursts (99 x 2 bits/line for the standard sub frames); outgoing data is transmitted as complete packets.

Four buffers enable the MV1720 to de-interleave a continuous stream of data from two independent subframes. It is possible to de interleave data that only occurs in certain lines, i.e. field blanking by using the DISD input. Output from the de-interleaver is available as PACKDT (packet data), PACKST (packet strobe) and SFRO (subframe origin).

Golay and Packet Type Decoder

This module uses a Meggitt decoder for error correcting the Golay encoded packet header and optionally the data part for selected packets.

To achieve real time operation, a pipelined syndrome register is included. The correctable error patterns are permanently stored in an on-chip ROM.

The module removes the 11-bit checksum in the packet header and inserts a bit indicating which of the two selected sub-frames is the origin of the packet. The module corrects the Hamming (8,2) PT byte as well.

The resulting error corrected packets are immediately passed on to the Message router.

Messager Router

The Message Router handles all incoming packets, and compares packet addresses and address fields in CMM packets. The microcomputer can select which packets should be transmitted to a buffer in the processor interface.

The selection is done by storing the different addresses in a table in the Message Router and comparing them to appropriate packet fields. This table is updated via the configuration chain. The table contains:

Packet 0 address (permanently stored)
CMM packet address (10 bits)
CMM packet Unique Customer address (36 bits)
CMM packet Shared address (24 bits)
CMM packet Collective address (12 bits)
SMM packet address (10 bits)
AUX packet address (10 bits)
Line 625 data packet (permanently stored)

The processor interface can control the priority between the different packets. All packets will be transmitted to the PDATA pin at 20.25 M bits. Data in line 625 is converted to a packet with the decimal address 1023 (inserted by the Line 625 Handler).

A strobe signal for the packet-headers is provided on a separate pin of the MV1720. This signal (VAL) is high during the first 13 bits (PA, CI, SFRI) of every packet.

The line 625 message is not strobed by the VAL signal. A strobe signal (SPINF) is enabled during output of this message. SPINF is also enabled during output of packets with packet address 0, CMM and SMM messages.

Line 625 Handler

This module handles parts of the special data burst in line 625 of each frame; i.e.

UDT - Unified Date Time
SDF - Static Data Frame
RDF - Repeated Data Frame

The first bit of UDT (sequence bit) is checked and any sequence error is flagged in the special line 625 packet. The next four bits of UDT are not processed in any way, just included in the line 625 packet.

In every fifth line 625 packet, a majority vote of the five last SDFs is included. In the other four packets, the SDF part is not valid. A flag (SDFV) indicates whether SDF is valid or not. The majority voted SDF's are also BCH error checked but not corrected. If the BCH check fails then SDFV is not set.

The five TDMCTLs in line 625 are also majority voted and BCH checked. The result (RDF) is included in the line 625 packet together with an error flag for the BCH check.

The module also contains a flywheel counter for FCNT. This counter is incremented every line 625. The most significant bit of FCNT is available externally as EFCNT. If a valid RDF is received, the received FCNT is loaded into the counter. Loading FCNT will not change EFCNT before next line 625.

Clock Generator and Function Select

CLK1 is used to generate all internal timing and must always be available. CLKD2 is only for D2/MAC reception.

RESET is used to reset MV1720 to a known state after power up.

FS1 and FS2 are function select inputs used during test and should always be tied to V_{SS}.

Processor Interface

The processor interface is for an external microcomputer. This microcomputer initialises and configures the complete MAC/packet chipset, and receives selected information from the packet multiplex together with status information.

This interface is designed to be compatible with a large number of different microprocessors or single chip microcomputers. The interface is shown in Fig.3.

ABSOLUTE MAXIMUM RATINGS (Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

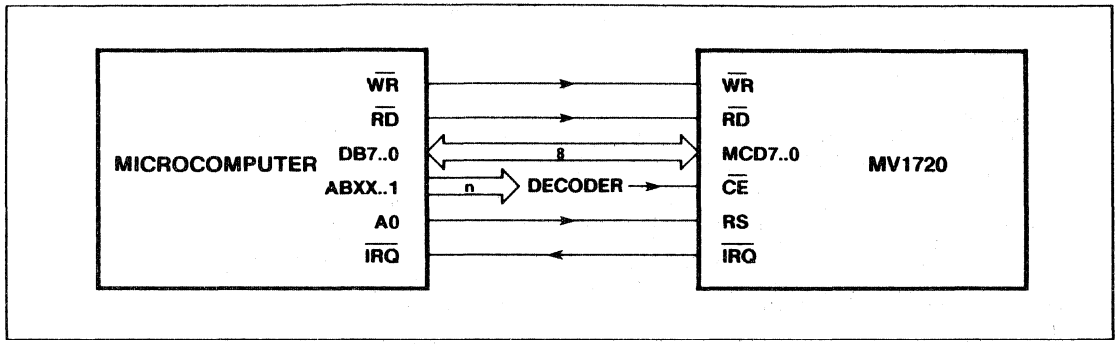


Fig.3 Interface between the MV1720 and a microcomputer

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	
Setup time (all inputs) See note 1		0	ns	

NOTE

1. This figure is valid for all data inputs relative to the positive edge of CLK1.

(ref.1) MAC packet family specifications EBU No. TECH 3258-E.

PLESSEY
Semiconductors

MV1730

MAC SOUND CIRCUIT

The MV1730 is the sound circuit for the Nordic VLSI C/D/D2 Mac Packet receiver chipset.

The MV1730 receives packets of data from the MV1720 control chip. Packets for the desired sound service and BI packets are recognised and processed. The configuration of the sound is automatically controlled by information in the BI packet. Descrambling of sound and scale factor extraction is done before the packet is stored in an external RAM. The RAM is a buffer which helps to adjust the varying packet arrivals to a regular output sample frequency. The samples are read from the RAM into the MV1730 for further processing. Errors are detected and corrected before they are forwarded to external chips for error concealment, digital filtering and D/A conversion. A microcomputer supplies the MV1730 with the control word for descrambling, packet address etc.

FEATURES

- Simultaneous Processing of Two Independent Sound Services, for instance Stereo Sound and Commentaries
- Linear and Companded Sound Decoding
- First or Second Level Error Correction
- Stereo, Mono, High Quality and Medium Quality Sound
- Configuration Data in BI Packets automatically set the right configuration of the chip
- Several MV1730s can be used in Parallel
- Conditional or Free Access Sound
- Digital Mixing of Main Sound and Commentary
- Scrambled or Non-Scrambled Data Output

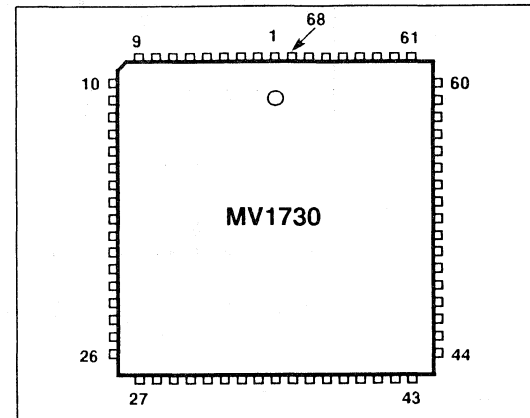
DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM

Packet Control

The packet control module, provides for packet reception at 20.25 M bits and timing for further packet processing. Each incoming packet has a header with a 10-bit address, one bit indicating in which subframe it is located, and two bits used as a continuity index. The packet header of each packet is compared with the contents of the configuration chain, and packets which match address and subframe are extracted. The continuity index is checked and packet loss is flagged.

BCBI

The BCBI module processes the packet type byte (PT), and determines whether it is a BI, BC1 or BC2 packet. This module also stores changes from BC1 to BC2 and vice versa, and indicates new sound configuration when three packets are received after the change has occurred. The two sound services are handled independently.



LC68

Pin	Function	Pin	Function
1	CLAB2	35	RDATA0
2	WSAB2	36	V_{SS}
3	40CLK1	37	$\overline{RD}$ATA3
4	EFAB1	38	$\overline{CAS}$
5	V_{DD}	39	V_{DD}
6	DAAB1	40	RDATA2
7	CLAB1	41	ADDR0
8	WSAB1	42	ADDR1
9	PURST	43	ADDR2
10	EFCNT	44	ADDR3
11	V_{DD}	45	ADDR7
12	CLK1	46	PA2
13	V_{SS}	47	PA1
14	CDATAIN	48	V_{SS}
15	CSTRB	49	BCDATA
16	V_{DD}	50	DSDATA
17	SIV	51	V_{DD}
18	SIC	52	FWD720
19	NC	53	CDATAOUT
20	V_{SS}	54	V_{SS}
21	NC	55	NFI2
22	V_{DD}	56	NFI1
23	NC	57	ENBC
24	V_{SS}	58	XC2
25	VAL	59	X22
26	PDATA	60	X12
27	ADDR4	61	V_{DD}
28	ADDR5	62	XC1
29	V_{SS}	63	X21
30	$\overline{ADD}$R6	64	X11
31	$\overline{RAS}$	65	40CLK2
32	$\overline{W}$	66	V_{SS}
33	V_{DD}	67	EFAB2
34	RDATA1	68	DAAB2

Fig.1 Pin connections - top view

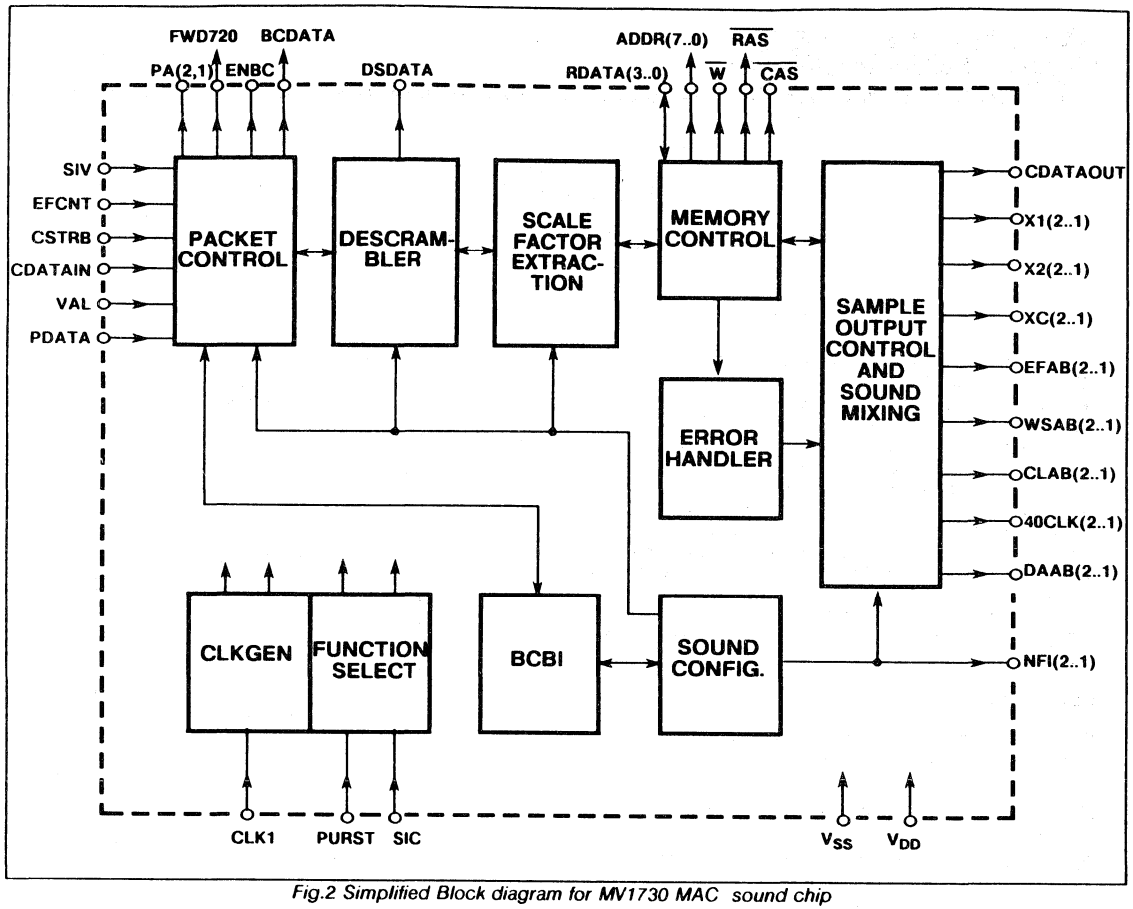


Fig.2 Simplified Block diagram for MV1730 MAC sound chip

Sound Configuration

The sound configuration block handles BI packets. The structuring bytes are error checked (Hamming protection), and if correct, the Bytes 1 and 2 are majority voted over the 5 repetitions. The current sound configuration is updated each time a BI packet is accepted. A new sound configuration is updated when three BC packets are received after a change BC1 to BC2, or BC2 to BC1.

Descrambler

The descrambler handles the two different sound services independently, and synchronisation can be achieved at the start of new frames.

It supports the three different levels of access-control described in the MAC standard. (ref .1)

Free access, unscrambled:
The sound data is unchanged.

Free access, scrambled:
The sound data is descrambled with a local control word stored in the receiver.

Conditional access, scrambled:
The sound data is descrambled with a control word from the conditional access system.

The signal EFCNT is the most significant bit in a frame counter, and it is used to resynchronise the descrambler. The other bits may be supplied by the configuration chain, to assure fast recovery after change of channel or power up.

The signal SIV starts an update of the descrambling system for each frame.

The control word for descrambling is provided by the configuration chain.

Scale Factor Extraction

The scale factor is extracted by majority decision logic. Nine samples are evaluated for each bit in the scale factor as described in the EBU specification (ref. 1). The control information intended for high speed switching is also extracted.

Memory Control

This block is the interface to a standard 4 x 16k DRAM. It generates the address $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ signals. Writing is done in page mode. There are a minimum of 256 refresh cycles per 4ms.

The number of packets in the RAM varies the sample output frequency slightly to maintain the buffer between 14 and 20 packets. A maximum of 32 packets can be stored per sound service.

Errors such as packet loss, full buffer and empty buffer are handled to minimise sound distortion. The parity bit is restored according to the scale factor and CIB bits, before the sound samples are sent to the error handler.

Error Handler

The Error Handler receives data from Memory Control and checks for errors. Four types of checks are done according to the data format:

Range checking (and if possible correction) according to scale factor and coding method (linear/companded).
Parity check (first level protection) for linear and companded data.
Hamming code check with single bit error correction for linear and companded data (second level protection).
Final range checking according to scale factor and coding method.

If any non-correctable errors are detected, the sample is flagged for concealment.

In addition the Error Handler does Range Limiting (for linear coding) and Range Expansion (for companded coding) before data is presented to the Sample Output Control Module.

Sample Output Control

The block contains an oscillator and output buffer for each of the two sound services, and a sound mixing unit. The sound mixing unit makes it possible to mix main sound and commentary sound. The main sound is output on sound service 1 pins. The mixing of both channels is controlled by the commentary channel. Both fade in time for the commentary channel and fade out time for the main sound, are controlled by bits FI2, FI1, and FI0 of the configuration chain. The range of fading time is 0.1 to 0.8sec. Both fade out time for the commentary channel, and fade in time for the main sound is controlled by bits FD2, FD1 and FD0 of the configuration chain. The range of fading time is 0.6 to 2.0sec. The bit MIX in the configuration chain selects if mixing is required or not.

The frequency of the oscillator controls the sample output rate. In order to maintain the sample storage in the RAM between 14 and 20 packets, the oscillator frequency is shifted slightly ($\pm$ 150ppm).

A frequency determining network, consisting of an 8.192MHz crystal and three capacitors is connected to X1, X2 and XC. Frequency control is exercised by internal switching of the capacitor connected to XC. Tolerance for the crystal is $\pm$ 30ppm.

The output pins DAAB, EFAB, CLAB, and WSAB are designed to match the Philips SAA7220 chip. This chip performs error concealment and filtering.

The error flag indicates unreliable sample data. In the case of erroneous samples, the output buffer will contain the last valid sample until a new valid sample is received.

Each sample is expanded from 14 to 16-bit by inserting zeroes in the two LSBs. The sample output frequency is always 32kHz. With medium quality sound at 16kHz sample frequency, each sample is copied and every second sample is error flagged and concealed.

The Configuration Chain

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the microcomputer.

Several function blocks of the MV1730 are controlled by the configuration chain. The packet control block needs the packet addresses and indication of which subframe (or both) to select packets from. In addition one bit per sound service is used for muting until a stable state is reached after change of sound service, or after power up.

The configuration chain also provides control words for descrambling. The two services can be descrambled independently.

In addition, the seven least significant bits of the frame count (FCNT), and one bit indicating update of the descrambling control word after a change of service or power-up, are placed in the configuration chain.

The configuration chain may be updated from the microprocessor at any time except in line 625 and line 1.

The configuration data is clocked into the chain when CSTRB is high, otherwise the contents of each register stage is stored.

ref.1
MAC packet family specifications
EBU No. TECH 3258-E

ABSOLUTE MAXIMUM RATINGS
(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS
Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	

MV1740

MAC TELETEXT DECODER

The MV1740 is the Teletext chip for the Nordic VLSI C/D/D2 MAC Packet receiver chipset.

The MV1740 is a single chip Teletext decoder capable of decoding VBI and MAC packet Teletext as well as normal terrestrial Teletext for 625 line systems. With dual page acquisition circuits, and direct memory addressing, the current selected page can always be kept live while the second acquisition circuit stores linked or other pages. The control of the MV1740 is via the I²C Bus with the configuration chain being used to select data configurations and codes.

FEATURES

- Non-display packets stored for linked page operation, video programming, and other advanced uses.
- Low external component count.
- Can decode MAC packets, D2MAC VBI and terrestrial World System Teletext.
- Multi-language capability for European languages .
- Up to 254 display pages stored, using two low cost 200ns DRAMs.
- High resolution characters 16 by 10 dot matrix.
- On chip Descrambler.
- Displays microcomputer generated pages.

DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM

PACKET RECEPTION AND TIMING

The packet header control, provides for packet reception and timing for packet processing. Each incoming packet has a header with a 10 bit address, one bit indicating in which subframe it is located, and a two bit continuity index. The packet header of each packet is compared with the contents of the configuration chain, and packets which match address and subframe are sorted out. The packet type byte is used to indicate whether the text packets are scrambled.

DESCRAMBLER

Descrambler synchronisation can be achieved at the start of new frames. All three different levels of access-control described in the MAC standard [1] are supported;

Free access, unscrambled:

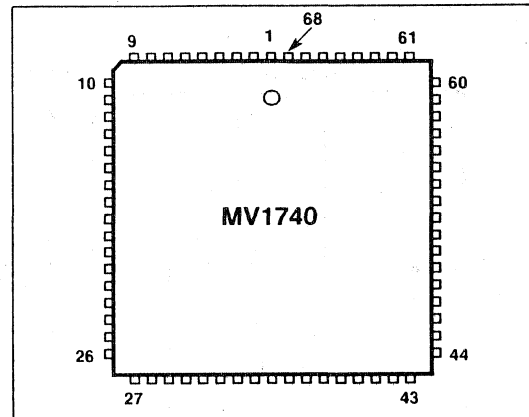
The Teletext data is delivered unchanged.

Free access, scrambled:

The Teletext data is descrambled with a local control word stored in the receiver.

Conditional access, scrambled:

The Teletext data is descrambled with a regenerated control word from the encryption system.



Pin	Function	Pin	Function
1	VDD	35	VSS
2	VSS	36	VDD
3	NC	37	TCR
4	SIC	38	BLANK
5	NC	39	RED
6	TTV	40	GREEN
7	VAL	41	BLUE
8	SIV	42	YOP
9	CSTRB	43	CSO
10	CDATAIN	44	A9
11	EFCNT	45	D1
12	NC	46	VSS
13	CLK1	47	A8
14	PDATA	48	$\overline{CAS}$
15	NC	49	D0
16	VSS	50	$\overline{WR}$
17	VDD	51	A6
18	NC	52	$\overline{RAS}$
19	ODATA	53	VDD
20	STRB42	54	A3
21	STRB90	55	A0
22	GSTRB	56	A4
23	CDATAOUT	57	A2
24	VSS	58	A5
25	XTO	59	A1
26	XTI	60	A7
27	XCK	61	VDD
28	$\overline{RESET}$	62	I2C SCL
29	SYNCI/O	63	I2C SDA
30	DATAI/O	64	EVENT
31	EXT	65	SE
32	BLC	66	TEST
33	WLC	67	VBIDAT
34	VIDEO	68	CLKD2

Fig.1 Pin connections - top view

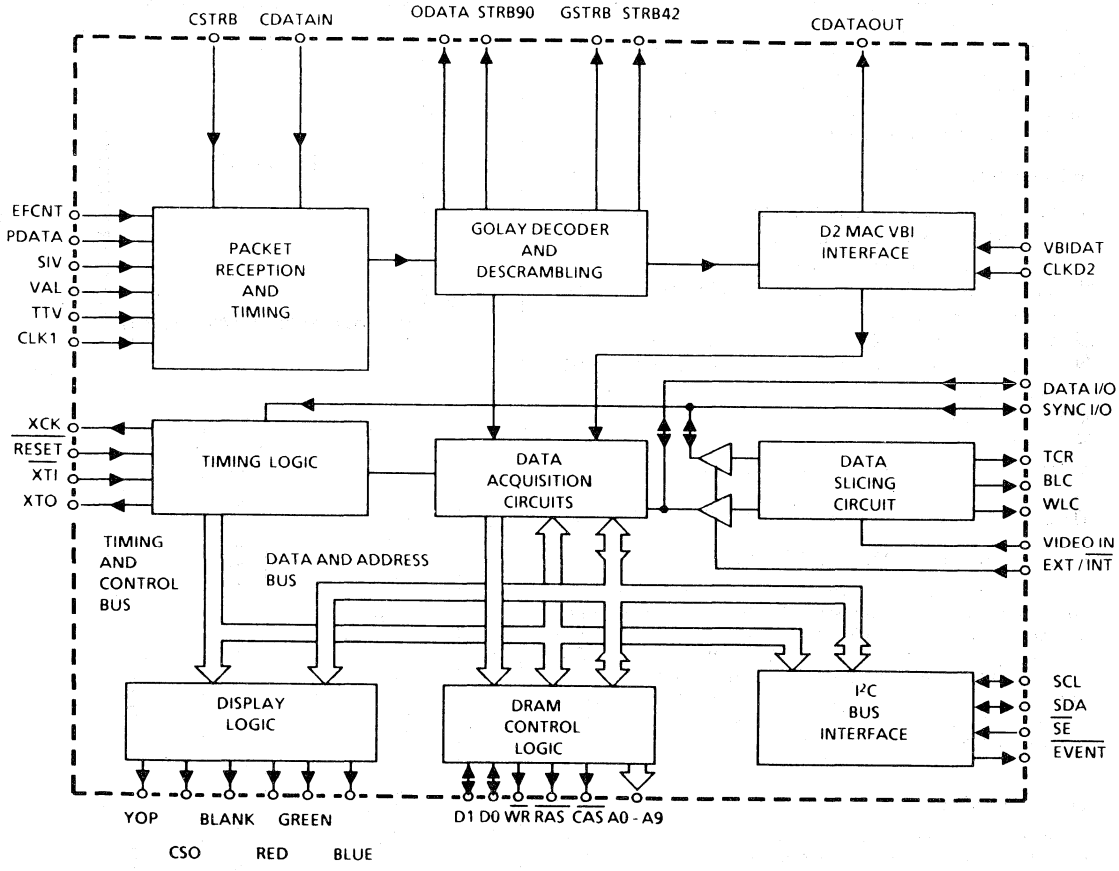


Figure 2. MV1740 Block Diagram

The signal EFCNT is the most significant bit in a frame counter, and it is used to resynchronise the descrambler. The other bits of the frame counter may be supplied by the configuration chain, to assure fast recovery after change of channel or power-up. The signal SIV starts an update of the descrambling system for each frame. The control word for the descrambling is provided by the configuration chain.

GOLAY DECODER

The Golay decoder receives MAC packets (all except header and PT byte) from the descrambler and corrects up to three errors in 12 information bits of each Golay word (24,12).

DATA ACQUISITION CIRCUIT

The MV1740 has dual acquisition circuits to ensure that the viewed page can always be kept live while the second acquisition circuit stores linked or other pages. The data acquisition circuits can accept data from one of three sources:

1: Parallel data from the internal Golay decoder.
2: D2MAC VBI serial data.
3: Video signal, data extracted using internal data slicer.

After Hamming Code checking and correction, the data is latched into the appropriate registers and compared with the internal programmable registers, as set up by the controlling microprocessor, to check for the desired magazine and page. The Teletext data is stored in two external DRAMS controlled completely by the MV1740.

I²C BUS INTERFACE

The MV1740 can be addressed on the I²C bus as either a slave transmitter or a slave reciever

The MV1740 has twelve read registers and nineteen write registers controlled via the I²C Bus. These registers control data acquisition and display. They are also used to inform the microprocessor of details of the received Teletext data. The register structure of the MV1740 allows the microprocessor to quickly read the Event and Page Receive registers, which hold the information on the page being currrently received.

TIMING LOGIC

The internal timing of the MV1740 is based on a single 27.75MHz crystal. To enable the MV1740 to be used with microprocessor generated text, a composite synchronisation pulse is generated on-chip if an external one is not available .

DRAM CONTROL LOGIC

The display memory uses two low cost DRAMs which are controlled by the MV1740, including all the necessary refresh cycles. Refresh occurs during the line flyback period on all ten address lines. The two DRAMs may be either: 64K x 1, 256K x 1, or 1M x 1 giving 14, 62, or 254 displayable pages in memory, (a display page consists of packets 0 to 25). In addition there are two pages of store for non-display packets. These two pages will store two versions of packets 29 and 30 and any mix of packets 26, 27, or 28 up to a total maximum of 23 packets per acquisition circuit. It is also possible for the MV1740 to use two 4Mbyte DRAMs if the extra address lines are externally controlled.

DISPLAY LOGIC

The MV1740 display is controlled via four write registers. Any of the stored pages in DRAM may be displayed. The features controlled include :

Which acquisition circuit is displayed;
Language displayed;
Control of display of the header;
Display of TEXT, PICTURE, or MIX;
Display of boxes of either text or picture;
Reveal of text hidden by "conceal" control codes;
Cursor control;
The display of rows 25 and 26;
Double height display of,
  Top half of text,
  Middle half of text,
  Bottom half of text.

Rows 25 & 26 can be displayed under software control. The contents of these rows will be optionally written by packets X/24 and X/25 dependent on the status of a register bit. A row zero write inhibit bit in a register will prevent the transmitted data in the header packet writing to memory, so that the microprocessor may process packet 8/30 data and write its own header line at the top of the screen.

THE CONFIGURATION CHAIN

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the microprocessor. Several functions of the MV1740 are controlled by the configuration chain. The packet control block needs the MAC packet addresses and indication of which subframe (or both) to select MAC packets from. The configuration chain also provides control words for descrambling.

The seven least significant bits of the frame count (FCNT) and one bit indicating the update of the descrambling after a change of service or power up are placed in the configuration chain.

ABSOLUTE MAXIMUM RATINGS
(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS
Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	

(ref.1) MAC packet family specifications EBU No. TECH 3258-E

MV1812

TELETEXT DATA ACQUISITION

The MV1812 is a high speed CMOS circuit capable of decoding any World System 625 line teletext transmissions.

The circuit operates on serial teletext data provided by the Plessey SL9100 Data Slicer and provides parallel words of data if the transmitted data matches the selection criteria set in the internal registers.

The circuit will be of particular use in teletext systems where the transmitted data is not intended for immediate display, where its high data throughput rate will allow large volumes of data to be received at the highest transmission rates possible. The design of the MV1812 will allow data in paged format or other formats to be equally well received.

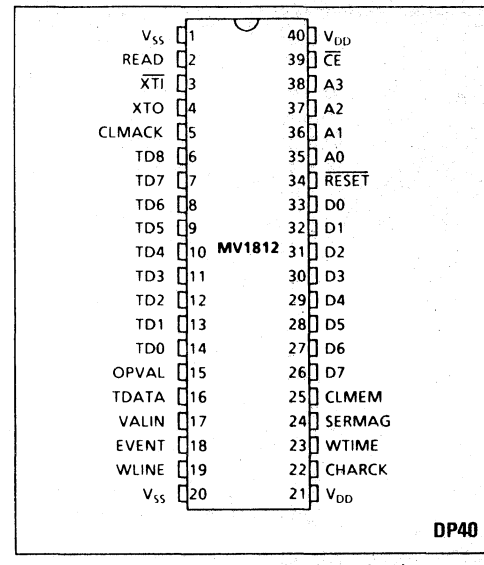


Fig 1 Pin Connections (top view)

FEATURES

- Interfaces with standard 8-bit data bus
- Nine internal registers giving complete acquisition control
- Data checking ensures minimal reception of errors
- Data purity counter for optimal electronic tuning
- Programmable Framing Code
- All teletext packets received
- 16,777,216 unique teletext pages may be specified

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.3V to 7V
Input voltage (all pins)	-0.3V to V_{DD} + 0.3V
Operating temperature range	0°C to + 70°C
Storage temperature range	-40°C to + 125°C
Relative Humidity	85%

APPLICATIONS

- Datacast and other 'Subscription User Group' service receivers
- Teletext/Telesoftware receivers for personal computers
- World System Level 1 to 5 teletext receivers
- Aerial and TV tuning equipment
- Advanced multi-media teletext service transceivers
- Hand held low power teletext receivers
- Video programming of VCRs (VPX)
- Specialist teletext receivers for cable TV systems

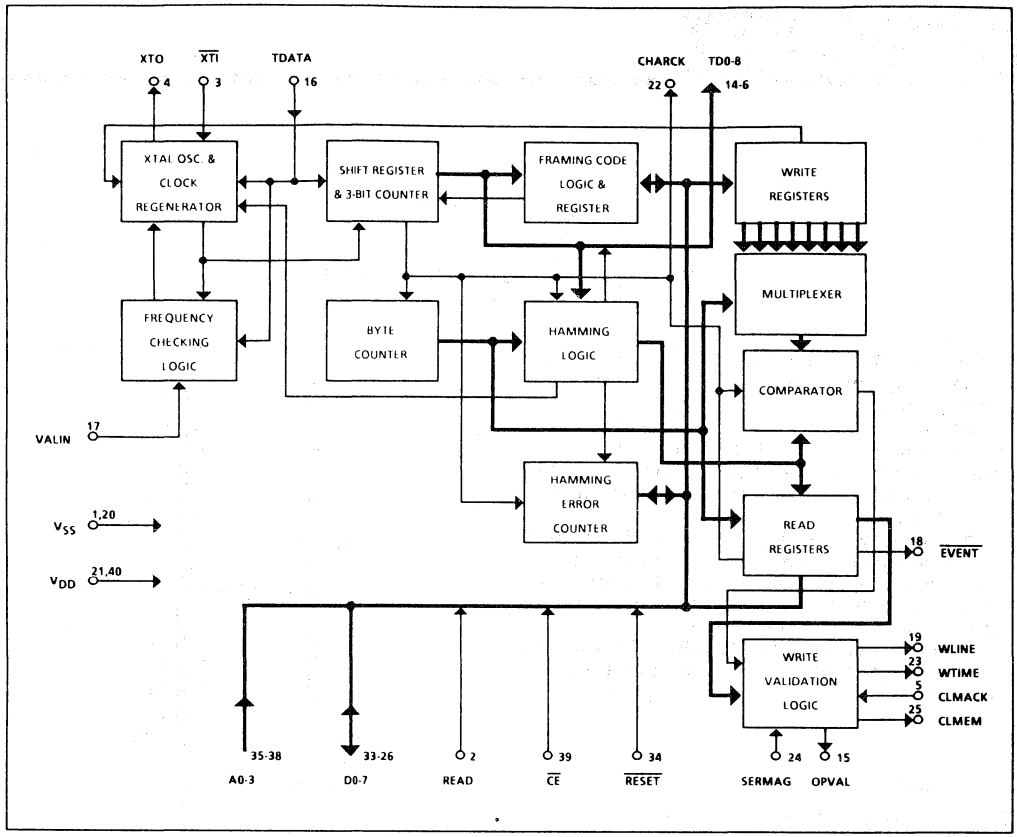


Fig 2 MV1812 Block Diagram

DEVICE DESCRIPTION

The MV1812 is a single chip teletext data acquisition circuit capable of receiving all current and proposed future teletext services. A block diagram of the device is shown in fig.2.

The device is controlled via a standard 8-bit data bus allowing a simple interface to most microprocessors. Complete control of the acquisition of data is provided via nine internal registers. A data purity counter is included to show the error rate of incoming data, which allows systems with electronic tuning to tune for optimum teletext reception and also has potential for aerial tuning. Page selection is achieved by specifying the magazine number, page number and page sub-code of the desired teletext page. The digits of each of these page selection codes may individually be specified as "don't care" or, alternatively, data acquisition may be disabled completely. The framing code is also programmable such that any 8-bit code may be specified for byte synchronisation at the start of each line. The default framing code for World System teletext transmissions is 27_{16}.

The MV1812 receives a teletext data stream from a data slicer such as the SL9100. An on chip oscillator provides a clock against which the frequency of the incoming data is compared. A data clock is recovered and used to shift the teletext data into an 8-bit shift register. The data is checked for the framing code which is used to byte synchronise the data and to initialise a character clock. A byte counter counts the character clock for subsequent enabling of data latches in the read registers. After any Hamming Code checking and correction, the data is latched into the appropriate registers and compared with the internal programmable registers, as set up by the controlling microprocessor, to check for the desired magazine page. Parallel 8-bit page data is output from the device together with a parity check bit for enabling or disabling writing of the data to memory.

PIN DESCRIPTIONS

V_{DD} & V_{SS} (pins 21 & 40, and 1 & 20 respectively).
The 5 volt ±0.5v supply is applied on any convenient pair of these pins. However, if large bus loads are to be driven from either of the data output buses, it is recommended that all four supply pins are used.

TDATA (Teletext Data, pin 16).
Sliced teletext data from the SL9100 circuit is input to the chip on this pin. (see fig. 3)

XTI & XTO (XTAL in & XTAL out, pins 3 & 4).
This pair of pins is designed to drive a 27.75000 MHz fundamental or third overtone quartz crystal. If a third overtone type is used, two external components are required to ensure operation at the correct frequency. Typical external components are, a 33nF capacitor and a 1µH inductor in series and in parallel with the crystal (see fig.4). A nominal 1 MΩ resistor is included on chip between XTI and XTO to bias the input to its correct operating region. The crystal should be within ± 100 p.p.m. of the nominal frequency over the operating temperature range.

VALIN (Valid Line, pin 17).
This input must be high during any TV line that may contain teletext data. It must return low (for at least the minimum period) prior to the next TV line in order to reset the acquisition circuits ready for the next clock run-in. The Sync Output from the SL9100 may be used, though for maximum data security, it should be gated off during the picture transmission lines if full field teletext transmissions are not being received.

RESET (pin 34).
The active low reset input. This input has a nominal 150KΩ resistor coupled to V_{DD}, and a Schmitt input buffer, allowing a simple external circuit consisting of a 1µF capacitor to ground, to perform a power-on reset pulse of sufficient duration to allow the crystal oscillator to stabilize. When held low, this input resets all registers to default settings, and initialises counters.

CE (Chip Enable, pin 39).
The active low chip enable input. When low, this input enables a read or write operation of the registers via the D0-D7 tri-state I/O's and A0-A3 address inputs.

READ (pin 2).
When READ is high with CE low, this input forces the D0-D7 pins to an active state, outputting the contents of the register addressed by the An inputs. If READ is low when CE is low, the addressed register is written with the data input on the Dn pins.

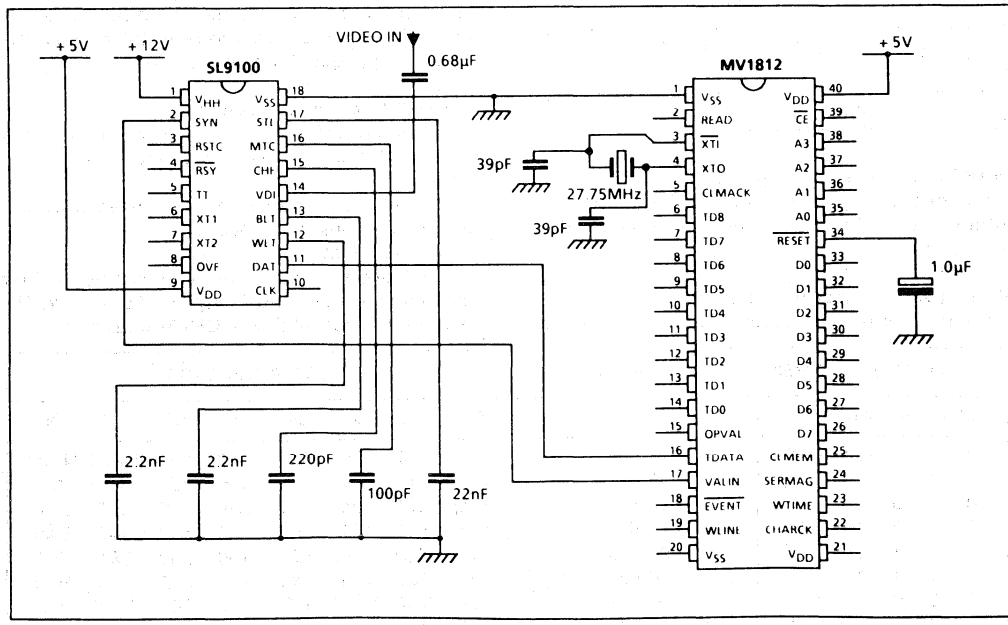


Fig 3 Interface to SL9100

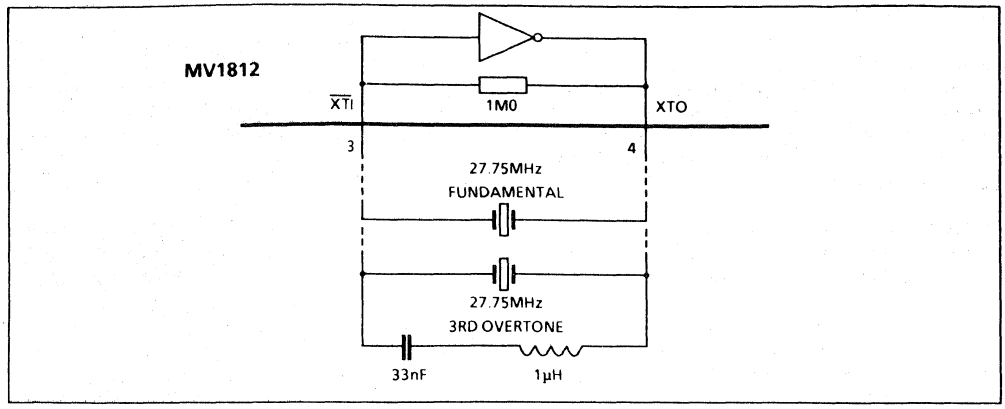


Fig 4 Crystal Oscillator Options

A0 - A3 (Address Inputs, pins 35 - 38).

The register address inputs. There are nine 8-bit registers to control the circuit as shown in Table 1. All other register addresses are absent. If written to, no action is taken, if read, FF_{16} is output. Details of the register contents and actions are described later.

TD8 - TD0 (Teletext Data Outputs, pins 6 - 14).

These nine outputs transmit the checked teletext data. Bits 7 to 0 are the data, bit 8 is a "write enable" bit for the word. It is controlled by the setting of the 'PAR' (Parity check inhibit) bit in the RECON register as shown below.

PAR	TD8
0	1 = PARITY CHECK CORRECT 0 = PARITY CHECK FAILED
1	ALWAYS 1

CHARCK (Character Clock, pin 22).

This output signal is used to 'clock' the TDn outputs. The TDn outputs are stable when this output is high.

D7 - D0 (Data Inputs/Outputs, pins 26 - 33).

The register data inputs/outputs. These pins are high impedance inputs at all times except when CE is low and READ is high, when they become outputs.

EVENT. (pin 18).

An active low open drain output intended for interrupting a microprocessor when an important event has occurred. The 'EVENT' register bits uniquely describe which type of event has occurred.

WLINE (Write this Line, pin 19).

This output is set near the beginning of every line to indicate to the external system whether the data appearing on TD0-TD8 is to be used or not. The time at which it is set in any particular line may vary depending on the packet number being received, but it is unconditionally stable when the OPVAL output goes high on each line.

WTIME (Write Time only, pin 23).

This output will only be set high during a line if the packet being received is a header (pkt. #0) and:-

i) the magazine number compares with that set in register bits MG2,1 & 0, or,

ii) the SERMAG input is high.

The data contained on such lines can be used for updating a real time clock display. As with WLINE, this output is not valid until OPVAL goes high.

ADDRESS				HEX	REGISTER NAME	REGISTER CONTENTS							
A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	EVENT	NPR	C10	C8	C4	VHR	NDP2	NDP1	NDP0
0	0	0	1	1	CBITS	C14	C13	C12	C11	C9	C7	C6	C5
0	1	0	0	4	SELCON	ACQ	MC	PBC	PAC	SDC	SCC	SBC	SAC
0	1	0	1	5	PGREQ1	SC3	SC2	SC1	SC0	SA3	SA2	SA1	SA0
0	1	1	0	6	PGREQ2	MG2	MG1	MG0	SD1	SD0	SB2	SB1	SB0
0	1	1	1	7	PGREQ3	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
1	0	0	0	8	RECON	CA	WI0	WI24	WI25	PAR	MV	MPX	RLH
1	0	1	1	B	HAMMC	H7	H6	H5	H4	H3	H2	H1	H0
1	1	1	1	F	FCODE	F7	F6	F5	F4	F3	F2	F1	F0

Table 1 Register Contents

SERMAG (Serial Magazine Reception, pin 24).

An input that controls the writing of header packets in conjunction with the above two outputs. The C11 control bit, as read from the CBITS register, defines whether or not serial magazine transmission is being used. The table below shows which headers are flagged by the WTIME and WLINE outputs for all combinations of the SERMAG input and the RLH (roll headers) bit in the RECON register. Note that the RLH bit enables WTIME and WLINE to only flag headers in which the C9 bit is not set.

INPUTS		OUTPUTS	
SERMAG	RLH.$\overline{C9}$	WTIME	WLINE
0	0	MH	PH
0	1	MH	MH
1	0	AH	PH
1	1	AH	AH

KEY:

PH - Headers for the requested page only
MH - Headers for requested magazine only
AH - All headers

OPVAL (Output Valid, pin 15).

WLINE & WTIME outputs are always valid when this output goes high. At the start of every line this output is reset low by the VALIN input and will go high as the fifteenth byte of data is being received by the circuit, unless a byte with an uncorrectable Hamming error is received, in which case it will stay low to the end of the line.

CLMEM (Clear Memory, pin 25).

Clear memory output. This output goes high if the first header received for a requested page has the C4 bit set. Subsequent headers for the same page do not affect this output.

CLMACK (Clear Memory Acknowledge, pin 5).

Clear memory acknowledge input. To reset the CLMEM output to the normally low state, this input must go high momentarily. A full chip reset will also clear CLMEM.

REGISTER DESCRIPTIONS

EVENT Register (Address 0)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
NPR	C10	C8	C4	VHR	NDP2	NDP1	NDP0
CONDITION ON RESET							
0	ud	ud	ud	0	0	0	0

ud = undefined

This register is read only, if written to, no action is taken. The register can be read at any time by the controlling microprocessor, but if an interrupt condition has been set, the condition will be cleared by the reading of this register and the EVENT output will return to a high impedance state.

There are eight possible events which set the EVENT output low. They are:-

i) a valid header (pkt. #0) has been received for the requested page,

ii) the complete requested page has been received, or

iii) one of six different non-display packets has been received.

The VHR bit, read via D3, indicates the "Valid Header Received" condition and the NPR bit, read via D7, indicates the "New Page Received" condition. These two bits are cleared by reading this register, as are NDP0-2, but bits C4, C8 & C10 remain as set by the last event to change them.

The three NDP bits in D2, D1 & D0, indicate which of the six "Non-Display Packets" has most recently been received. These bits are the three least significant bits of the packet number (or row address) as received in bytes four and five. They uniquely describe the packet number as in the table below:-

Received Packet No.	NDP Bits		
	2	1	0
26	0	1	0
27	0	1	1
28	1	0	0
29	1	0	1
30	1	1	0
31	1	1	1

The other three bits in positions D4, D5 & D6 are the control bits C4, C8 & C10 respectively from the most recently received header (pkt. #0). Their respective functions are Erase Page, Update Page and Inhibit Display. These three bits cannot set the EVENT output.

Header packets passing through the MV1812 for the purpose of updating displays etc.(eg WTIME), have no effect on the bits in this register.

CBITS (Control Bits) Register (Address 1)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
C14	C13	C12	C11	C9	C7	C6	C5
CONDITION ON RESET							
ud	ud	ud	ud	ud	ud	ud	ud

ud = undefined

This register is also read only. Its contents are as shown in the table above. They are the remaining control bits from the most recently received header (pkt. #0) which matched the acquisition requirements in the PGREQ registers.

The bit functions are:-
C5 - Newsflash
C6 - Subtitle
C7 - Suppress header
C9 - Out of sequence page
C11 - Serial magazines
C12, C13 & C14 - Language control bits

SELCON (Select Acquisition Control) Register (Address 4)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
ACQ	MC	PBC	PAC	SDC	SCC	SBC	SAC
CONDITION ON RESET							
1	1	1	1	0	0	0	0

The SELCON register has full read and write capability. Its control bits govern which digits of the incoming headers (pkts. #0) are compared with the register contents for page acceptance. The read data is normally identical to that most recently written to this register (see note under PGREQ registers). The individual bits have the following functions:-

ACQ -Acquisition on. When set high, Teletext acquisition is enabled. When low, acquisition is disabled. It is recommended that acquisition is disabled when changing channel, to minimise the possibility of data errors and to reset the internal "Page Being Received" flag to avoid a lock-up situation, where a page has started being received, then no suitable terminating header is received, due to a channel change.

MC -Magazine Compare. When set, this bit allows comparison of the received magazine bits with the register bits. Not set implies don't care.

PBC, PAC -Page Number Digits Compare. When set, these bits allow comparison of the respective received page number bits with the register bits (PA = least significant digit).

SDC, SCC, SBC, SAC -Page Sub-code Digits Compare. When set, these bits allow comparison of the respective received sub-code bits with the register bits (SA = least significant digit).

PGREQ1, 2 & 3 (Page Request) Registers (Addresses 5, 6 & 7) (see Table 2)

These registers define the magazine, page number and sub-code (formerly time-code) which the MV1812 compares with the incoming headers (pkts. #0) to establish if the following page related packets (pkt. nos. 1-28) are to be received or not. The default setting after reset is magazine 1, page 00, sub-code 0000, though the sub-code digits are ignored by the default state of the SELCON register.

The bit functions are:
MGn -Magazine select bits
PBn, PAn -Page no. select bits
SDn, SCn, SBn, SAn -Sub-code select bits

The read sections of these registers are completely separate to the write sections. Initially they are undefined, but after reception of the first valid header, they contain the magazine no., page no. and sub-code of the page being received, irrespective of any "don't care" settings in the SELCON register. This feature allows the microprocessor to read the page number as soon as the "Valid Header Received" interrupt has occurred, so that it may decide in advance of receiving the data, where the data is to be stored. This is particularly useful in the case of rolling pages (multi-page sequences with the same page no.), as each received page can (if sub-coded) be stored in separate areas of memory and updated as required.

NOTE: The PGREQ registers are double buffered by the internal "Page Being Received" signal. This prevents data from different pages being accepted erroneously as the original page. If a new page number is written to the PGREQ registers during reception of a page, the new data is held internally until the current page has been completed (defined by the reception of another header which does not compare with the current SELCON/PGREQ settings). The new page number is then transferred to the comparison registers.

The SELCON register is also double buffered, but by the VALIN signal, such that any data written to the SELCON register while VALIN is high, is not transferred to the active part of the register until VALIN returns low. If the SELCON register is set such that all digits except the magazine number are "don't care", all headers for the specified magazine will compare and the "Page Being Received" signal may be permanently on. In this case, writing a new value to PGREQ2 to select a different magazine will not take effect unless the ACQ bit in SELCON is set low temporarily, to reset the "Page Being Received" signal.

ADDR	REGISTER NAME	REGISTER CONTENTS							
		D7	D6	D5	D4	D3	D2	D1	D0
5	PGREQ1	SC3	SC2	SC1	SC0	SA3	SA2	SA1	SA0
6	PGREQ2	MG2	MG1	MG0	SD1	SD0	SB2	SB1	SB0
7	PGREQ3	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
		CONDITION ON RESET							
5	PGREQ1	0	0	0	0	0	0	0	0
6	PGREQ2	0	0	1	0	0	0	0	0
7	PGREQ3	0	0	0	0	0	0	0	0

Table 2 Page Request Register Contents

RECON (Receive Control) Register (Address 8)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
CA	WI0	WI24	WI25	PAR	MV	MPX	RLH
CONDITION ON RESET							
0	0	0	0	0	0	0	0

This register controls various aspects of the reception of teletext information within the MV1812. With the exception of the MPX bit (read via D1), the written and read information are identical. The bit functions are:-

CA -This bit is for future requirements.

WI0 -Write Inhibit packet #0. Setting this bit inhibits the appearance of WLINE and WTIME if they would otherwise have been set high by a received header (packet #0). It does not inhibit writing of any internal registers by such headers or reception of data related to any such headers.

WI24 & WI25 -Write Inhibit of packets #24 and #25. These bits inhibit the setting of WLINE during reception of either packets #24 or #25 during reception of page related data

PAR -Parity check disable when set. See also the description of TD8 (pin 6) output.

MV -Majority Voting enable bit. When set high, this bit enables any seven of the eight bits of the framing code word to be matched for word synchronization, otherwise all eight have to match exactly. Synchronization will always be correct with seven bit matching of the default framing code (27_{16}), since during the clock run in, the best match will be of five bits. Majority voting therefore allows synchronization in the presence of errors that might otherwise cause the line to be rejected.

MPX -Non-multiplexed data bit. This bit has no effect when written to. When read, this is the first message bit (L.S.B.) of byte six of the most recently received packet 8/30, or Broadcast Service Data packet. This indicates whether the teletext transmissions are full field (MPX = 1) or field-blanking interval only (MPX = 0).

RLH -Roll Headers bit. When set, this bit allows all sequentially numbered headers to be written to store in conjunction with the WLINE output. Normally, only headers (packets #0) pertaining to the requested page would be signalled by WLINE, but when RLH is high and SERMAG (pin 24) is low, all headers of the selected magazine (MG2,1 & 0) are signalled. When SERMAG is also high, all magazines headers are signalled. Any header though, with the C9 (out of sequence) bit set, will not be signalled with WLINE. The register contents will not be affected by such headers, and interrupts will not be generated by them.

HAMMC (Hamming Error Counter) Register (Address B_{16})

This register shows the number of errors in the

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0
CONDITION ON RESET							
0	0	0	0	0	0	0	0

Hamming encoded words checked by the MV1812. Any recognisable Hamming error*, correctable or not, causes the count to be incremented by one. The counter overflows at 255 (FF_{16}) and restarts. The Hamming encoded words checked (and internally corrected) by the MV1812 are:-

Packet no.	Byte nos. checked
0	4 - 13 inc.
1 - 25	4 & 5
26 - 31	4,5 & 6

The counter is reset to zero by a hardware reset (pin 34) or by writing zero to it. Writing any other number has no effect.

This counter is primarily intended to allow an electronic system to tune for optimum teletext reception. It should be noted that intervals between broadcasts of particular teletext page numbers may be erratic, giving erratic short term count rates for a given average level of errors. This can be overcome either by enabling reception of all pages by setting all SELCON register bits (except ACQ) low to receive all pages, or to disable page based data reception, as described in the SELCON register description. The former technique is probably preferable as it will give a far higher count rate for any given level of errors, allowing more rapid tuning. The latter would only give the error rates of packets such as 8/30 which may not be broadcast by all authorities.

* 3,5,7 & 8 bit errors in Hamming encoded words are not recognisable.

FCODE (Framing Code) Register (Address F_{16})

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
F7	F6	F5	F4	F3	F2	F1	F0
CONDITION ON RESET							
0	0	1	0	0	1	1	1

This register establishes the byte used for comparison with the incoming data for the purpose of establishing byte synchronization. For normal World System Teletext this will be 27_{16}, so this is the default. However any other byte may be used. The read data is identical to that written.

APPLICATION NOTES

The following notes assume that the MV1812 is to operate in a system which conforms to the principles of teletext transmissions as described in the "World System Teletext Specification".

DATA INPUT

Prior to any data being presented to the MV1812, the RESET and VALIN inputs must be held low for at least the minimum period, and preferably for about 250ms from power up, if a crystal is used as the clock source, to avoid erroneous clocking as the crystal starts oscillating.

After VALIN is released (goes high), the clock regeneration section (see fig 2) searches for the first negative going edge of the incoming data stream on TDATA and synchronises to this. The frequency of the clock run-in is compared with the bit clock derived from the 27.75MHz clock. If the clock run-in is not within + 16/-10% of the correct frequency, the acquisition circuits are locked to prevent any further action until VALIN returns low.

If the frequency check is good, the fifth negative going edge of the clock run-in is used to resynchronise the bit clock, which is then used to clock the incoming data into the main shift register. The contents of this shift register are compared after each shift with the programmed framing code. If an exact match of all eight bits occurs (or seven bits, see RECON register description), a three bit (divide-by-eight) counter is started, to generate a byte synchronised clock. If no match is found in the first 24 received bits, the acquisition circuits are locked until VALIN returns low.

As the subsequent bytes (nos. 4, 5, etc.) are received, they are latched and presented on outputs TD0 to TD7 (with parity check output on TD8) with the byte synchronised clock, CHARCK. On all received teletext lines, bytes four and five are checked for correct Hamming protection. If possible and necessary, the four message bits are corrected internally, prior to being latched into the appropriate registers. Bytes four and five contain the magazine number (3 bits) and the packet number (5 bits). If the packet number is in the range 26-31, byte six is also checked for good Hamming protection. If the packet number is zero, a page header, bytes six to thirteen are checked by the Hamming circuits. If any of the Hamming checked bytes fails and cannot be corrected, the acquisition circuits are locked until VALIN returns low. The data output on pins TD0 to TD7 is as received, without any Hamming correction, therefore the user must also do the Hamming correction on these and any subsequent bytes so protected, prior to using the data.

DATA OUTPUT

In the event of an uncorrectable Hamming failure, it is likely that some data may already have been latched into external circuits by CHARCK. To avoid the possibility of this data being used erroneously, it is suggested that the output data is buffered before being transferred to system memory. One method of achieving this is to use the MV1830 as shown in fig.5. The MV1830 is a high speed CMOS teletext data buffer organised as 64 by 9 bit words. The first device stores data from one TV line until OPVAL goes high. If WLINE is high, data is gated into the next data buffer in sequence until VALIN goes low at the end of the line. If WLINE is not high when OPVAL goes high, or if OPVAL does not go high, any data in the first MV1830 will be reset by VALIN at the end of that line. Once the teletext data has been transferred to the second data buffer, the host processor may read the data during the remainder of the current line and part of the subsequent line, bearing in mind that a further 42 bytes of data may be transferred when OPVAL goes high during the

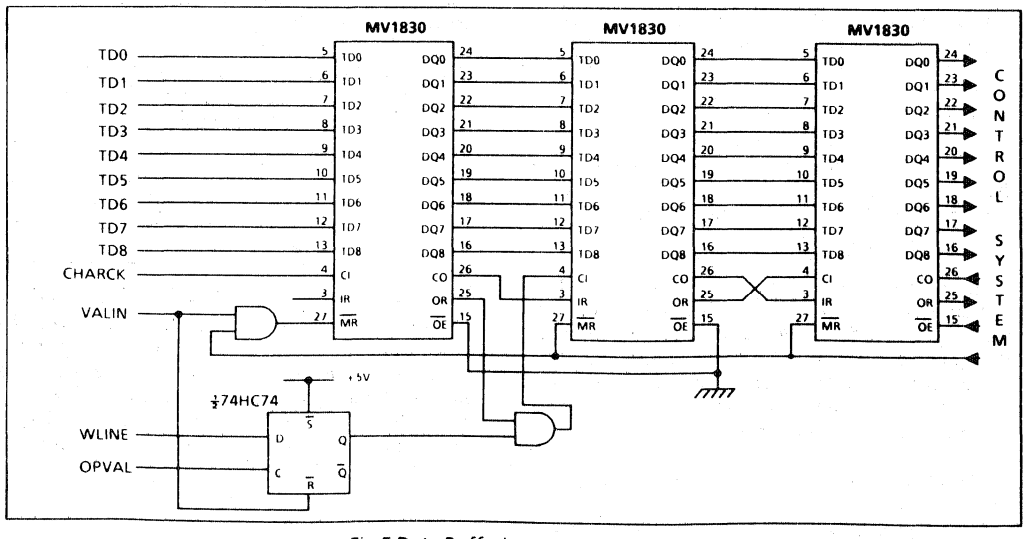


Fig 5 Data Buffering Using MV1830

Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Magazine	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet	30	30	30	30	30	30	30	30	31	31	31	31	31	31	31	31
Received?	Y	N	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y

Table 3 Independent Data Service Packets

NOTE:
Received? indicates whether or not reception of packets belonging to a particular channel is indicated by WLINE. Channels marked 'N' are received and passed through the MV1812, but do not set WLINE or generate an EVENT. At the present time, only channels 0, 8, 9, 10 & 11 have defined purposes within the World System Teletext Specification.

next TV line. If a total of four MV1830s are added in cascade after the first device, the data from up to six TV lines may be stored during the vertical blanking interval, allowing a slow system to read the data during the rest of the TV frame period.

An alternative arrangement is to use DMA to transfer the data directly from the MV1830 into system memory. One possible DMA interface is shown in Fig. 6. Teletext data is stored in the MV1830 until the end of the current line. If WLINE and OPVAL are not both high when VALIN goes low, the data buffer is reset. If WLINE and OPVAL are both high, however, a DMA request is generated. The DMA controller should be programmed to transfer 42 bytes of data only, after which the DMA request must be reset before VALIN goes low again after the next TV line.

ACQUISITION CONTROL

Teletext packets related to a particular page are those that follow a given page header (pkt. #0) if they are of the same magazine, and if their packet numbers are in the range 1-28 inclusive. Such packets are signalled by the MV1812 using WLINE, assuming that the selection criteria within registers SELCON and PGREQ1, 2 & 3 have been fulfilled for the page header in question.

Packet numbers 29, 30 & 31 have no relation to any particular page and may be transmitted at any time. The MV1812 will signal with WLINE the reception of X/29, 0/30 and X/31, where 'X' is the magazine number defined in PGREQ2 and SELCON.

Packets X/29 are defined as 'magazine related', containing information relating to all pages within that magazine.

Packets #30 and #31 are referred to as an 'Independent Data Service' facility within the teletext transmission service. Instead of referring to packets and magazines, bytes four and five are re-labelled as:-

Byte 4 -parallel data channel number

Byte 5 -all data bits = 1 indicating Independent Data Service packet

The four bits of byte four thus define one of 16 parallel data channels, which correspond to magazines/packets as shown in Table 3.

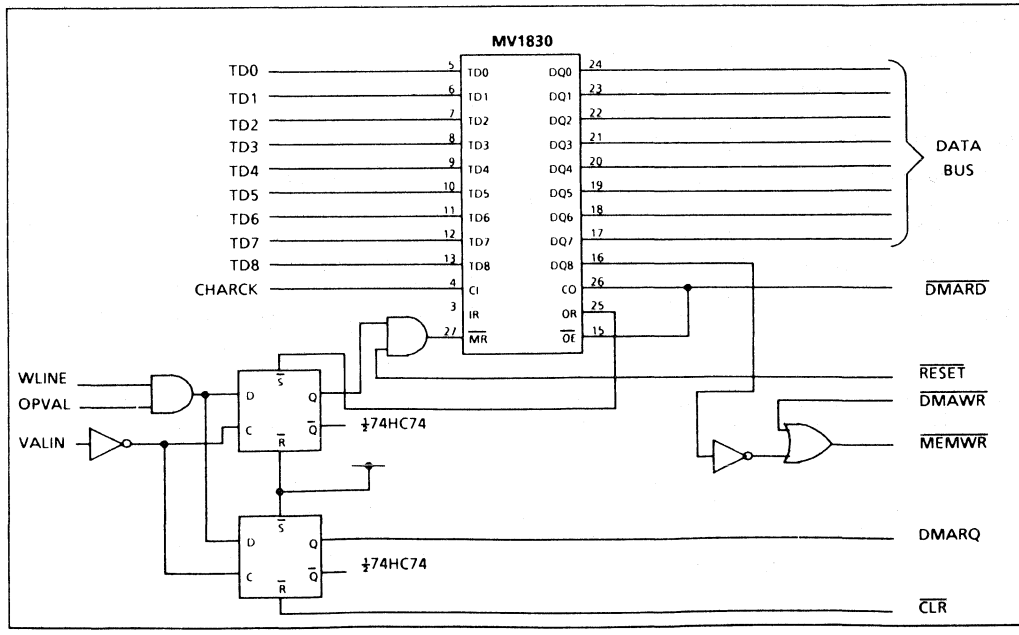


Fig 6 Data Buffering for DMA Interface

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
All Inputs (except XTI)						
Input low current (source)		-10	-33	-100	µA	All inputs have 150KΩ pull-
Input high current (sink)				±1	µA	up resistor to V_{DD}
XTI input	3					
Input low current (source)				-10	µA	
Input high current (sink)				+10	µA	
All Inputs (except RESET, VALIN & TDATA)						
Input low voltage		-0.3		1.5	V	
Input high voltage		3.5		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
VALIN & TDATA	17,16					
Input low voltage		-0.3		0.8	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
RESET input (Schmitt input)	34					
Input low voltage		-0.3		1.0	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
Threshold voltage (rising)			1.85		V	$V_{DD} = 5V$
(falling)			1.05		V	$V_{DD} = 5V$
All outputs (except CHARCK, XTO & EVENT)						
Output low (sink)		13.8	26		mA	$V_{OL} = 0.4V$
Output high (source)		-21.7	-46		mA	$V_{OH} = 2.4V$
CHARCK, XTO & EVENT	4,18,22					
Output low (sink)		6.9	13		mA	$V_{OL} = 0.4V$
CHARCK,& XTO	4,22					
Output high (source)		-10.8	-23		mA	$V_{OH} = 2.4V$
Supply Current	21,40			10	µA	F_{IN} (XTI) = 0Hz
			10		mA	F_{IN} (XTI) = 27.75MHz
Max Input Frequency, $F_{IN_{MAX}}$	3	27.75			MHz	

DYNAMIC CHARACTERISTICS (see Fig 7)

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Sym	Value			Units	Conditions
		Min	Typ	Max		
Reset low time	T_{RL}	75			nS	
Address to data valid	T_{ADV}			70	nS	
Read enable to data valid	T_{EDV}			80	nS	Note 1
Read disable to data bus free	T_{DF}			30	nS	Note 1
Data setup before address change or write disable	T_{DAS}			30	nS	Note 2
Data hold after address change or write disable	T_{DAH}			30	nS	Note 2
VALIN low time	T_{VL}	75			nS	
VALIN high to first negative TDATA clock edge	T_{VC}	50			nS	
Clock run in	$T_{CR_{MIN}}$	10			bits	Note 3
	$T_{CR_{MAX}}$			16	bits	Note 3
Data setup before CHARCK	T_{DS}	100			nS	
Data hold after CHARCK	T_{DH}	400			nS	
CHARCK high time	T_{CH}	4	4	4	bits	Note 3
CHARCK low time	T_{CL}	4	4	4	bits	Note 3
Write outputs setup time before OPVAL high	T_{WS}	1.08			µS	Outputs WLINE & WTIME
OPVAL low after VALIN low	T_{OPL}			80	nS	
OPVAL high after first CHARCK positive edge	T_{OPH}	87	87	87	bits	Note 3
EVENT low after VALIN low	T_{EN}			40	nS	Note 4
EVENT low after first CHARCK positive edge	T_{EP}	80	80	80	bits	Note 5

Note 1 -Read enable/disable is from the leading/trailing edge of the logical AND of READ high and CE low
Note 2 -Write enable/disable is from the leading/trailing edge of the logical AND of READ low and CE low
Note 3 -One bit period = 4 x XTI period
Note 4 -All events other than NPR or VHR
Note 5 -Events due to NPR or VHR bits being set

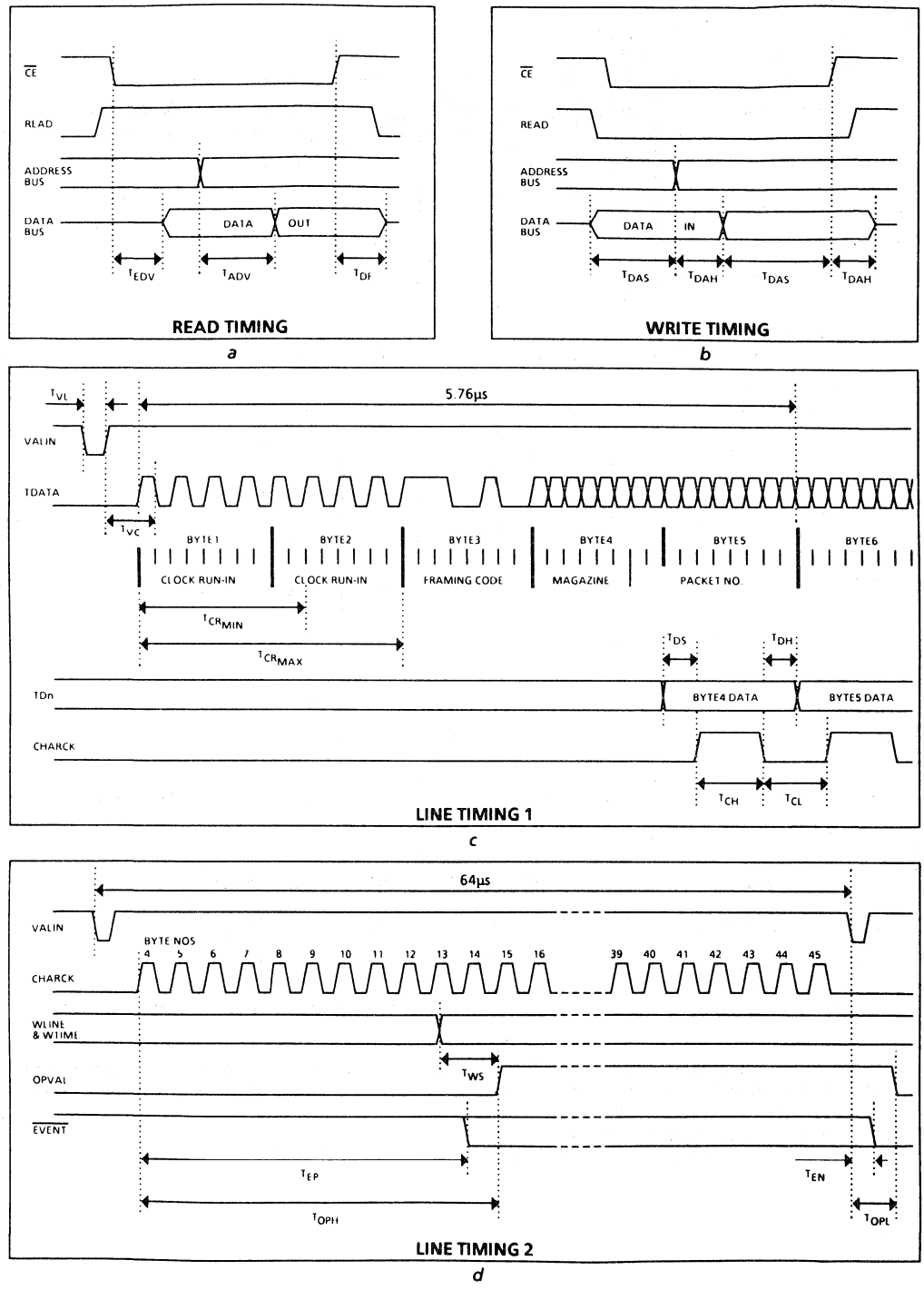


Fig 7 MV1812 Timing Diagrams

PLESSEY
Semiconductors

MV1815

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World Standard Teletext Systems. The MV1815 has an on board data slicer circuit, dual page acquisition circuits, and direct memory addressing, which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

- On-Chip data slicing.
- Up to 254 display pages, using two low cost 200ns DRAMs.
- Low external component count.
- I²C Bus for low cost interfacing .
- Multi-language capability for fourteen European languages .
- Pinout to suit single sided PCB layout.
- Non-display packets stored for linked page operation, video programming, and other advanced uses.
- High resolution characters 16 by 10 dot matrix
- Advanced CMOS technology gives low power dissipation and high reliability.

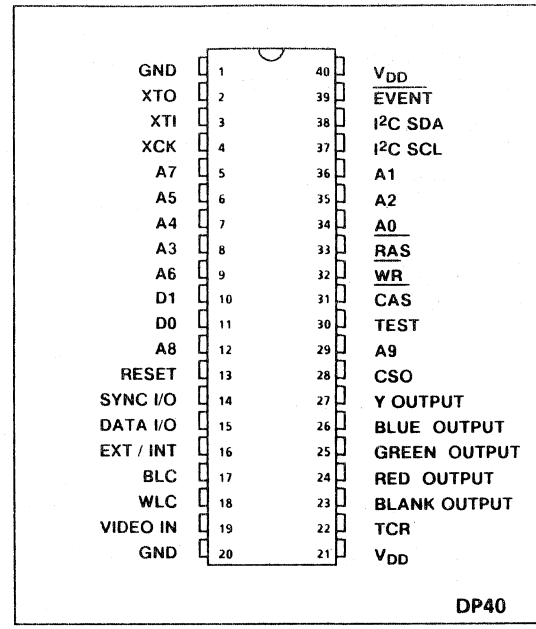


Figure 1. Pin Connections (top view)

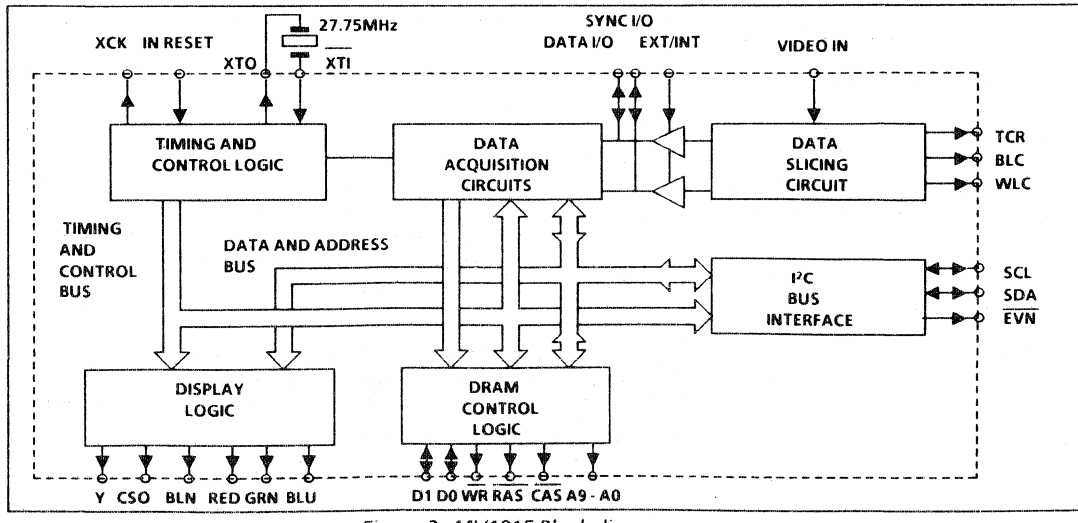


Figure 2. MV1815 Block diagram

Section	Specification
Data Acquisition Logic	
Teletext data rate	625 Lines 50 Fields / second. 6.9375 Mbits / sec ± 25ppm.
Data line content	360 bits as 45 bytes of 8 bits each.
TV lines used VBI	Lines 6 to 22 and 319 to335.
TV lines used full field	Lines 6 to310 and 319 to 622. (display is interrupted during data acquistion).
Packets accepted	X/0 to X/25, X/26, X/27,X/28, X/29, 8/30 (formats 1 & 2), X/31.
Page numbers	00 to FF
Pages subcodes	0000 to 3F7F
Display Logic	
Characters per row	40, occupying 46.126µs of the 52µs display time
Teletext rows displayed	1 to 24 and 25 and 26 software switchable
TV lines used	Rows Start Finish 24 48 288 26 38 298
Character definition	16 x 10 dot matrix
Character Sets	English, German, Swedish, Italian,Belgian,Spanish, Czechoslovakian, Polish, Rumanian, Hungarian, Serbo Croat, Danish and American
Spacing control characters	Standard Level One Range
Data boxing into picture	Page Number - Row 1 characters 1 to 8 Page Header - Row 1 characters 9 to 32 Clock Time - Row 1 characters 33 to 40 Rows 25 and 26
Displayable page stores	14 to 254 each of 1K bytes, depending on the size of the DRAM being used
Display options	Picture, Text Mix of text foreground and picture background Three part magnify - display rows 1 to 12 rows 7 to 18 rows 13 to 24 Boxing of Newsflash and Subtitles into picture Boxing of picture into text.
Dynamic RAM Control Logic	
Device Type	2 off 1M x 1 or, 2 off 256K x 1 or, 2 of 64K x 1 with page or nibble mode operation.
Maximum access time (t_{RAC})	200ns.
Refresh period for complete memory	2.048ms. Refresh occurs during the line flyback period. Contents of any memory location may be accessed by the microprocessor via the I²C Bus interface.
I²C Bus Interface	Standard implementation of a slave transmitter / receiver. Control of the MV1815 is via 31 on - chip registers.

Table 1 MV1815 System Specification

Device Description

The MV1815 is a single chip teletext decoder using an on chip data slicing circuit capable of receiving Teletext services broadcast to the WST Level 1+ standard, for display on 625 line TV receivers.

The device is controlled using a low cost I²C interface allowing easy interface to microprocessors. The register structure of the MV1815 allows the microprocessor to quickly read the Event and Page Receive registers, which hold information on the page being currently received. The chip requires only a single 27.75MHz crystal for all system clocks, this clock is internally divided by two to generate an external clock capable of driving the host microprocessor at 13.875MHz.

The MV1815 has dual acquisition circuits to ensure that the viewed page can always be kept live while the second acquisition circuit stores linked or other pages. It is possible for many linked page numbers to be transmitted in extra packet 27's. As the MV1815 has the capacity to store up to 254 different pages, it can store a complete magazine of linked pages.

The display memory uses two very low cost DRAMs. The DRAMs are controlled by the MV1815, including all the necessary refresh cycles. Refresh occurs during the flyback period on all ten address lines. The two DRAMs may be either: 64K x 1, 256K x 1, or 1M x 1 giving 14, 62, or 254 displayable pages in memory, plus two pages of store for non-display packets. These two pages will store two versions of packet 30 and two versions of packet 29 leaving the rest of the two pages to store any mix of packets 26, 27, or 28 up to a total maximum of 23 per acquistion circuit. It will be possible for the MV1815 to use two 4Mbyte DRAMs if the extra address lines are externally controlled.

Rows 25 & 26 can be displayed under software control. The contents of these lines will be optionally written by packets X/24 and X/25 dependent on the status of a register bit. A row zero write inhibit bit in a register will prevent the transmitted data in the header packet writing to memory, so that the microprocessor may process packet 8/30 data and write its own header line at the top of the screen. The displayed page can be enlarged into three overlapping half pages for ease of reading.

The on board character ROM holds 192 different characters with a resolution of 16 x 10 dots . This allows selective interlacing with high resolution characters, and a seven language capability.

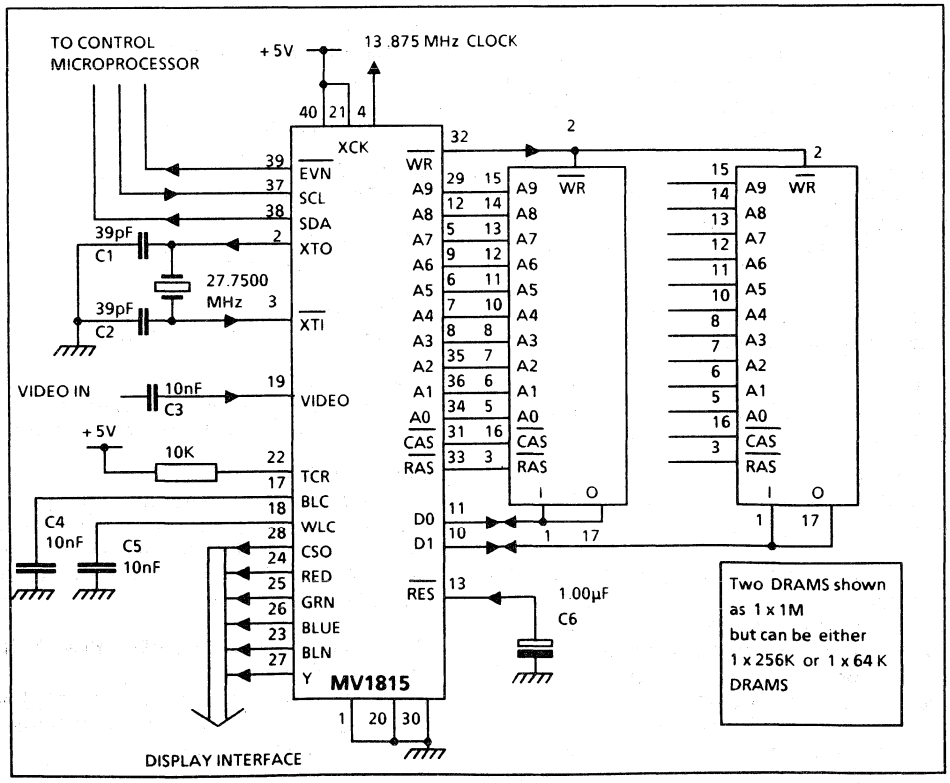


Figure 3. MV1815 applications circuit

APPLICATION NOTES

The following notes assume that the MV1815 is to operate in a system which conforms to the principles of the teletext transmissions as described in the "World System Teletext Specifications".

The design of the MV1815 enables it to be incorporated in a system, using a minimum of external components, figure 3 shows a typical application circuit. It can be seen from this circuit that to produce a complete multi-page teletext system requires only three ICs and eight discrete components.

The video signal required is typically 1V (peak to peak) coupled by a 10nF capacitor in series.

The pin-out on the MV1815 has been specially designed to allow the circuit to be constructed easily on a single sided PCB when using either 64K x 1 or 256K x 1 DRAMs. It is required that two DRAMS are always included in the circuit rather than a single large DRAM, as the MV1815 expects to access a two deep memory field.

The reset input must be held low for about 250ms from power up to avoid erroneous clocking. A 1µF capacitor is all that is required.

If the on-chip data slicer is not required, by holding EXT/INT high, an external data stream and sync pulses may be input to the MV1815 on pins SYNC and DATA.

Pin Descriptions

Vdd and **Vss** (pins 21 & 40 and 1 & 20 respectively).

The 5 ± 0.5 volt supply is applied to any convenient pair of these pins. It is however recommended that all four supply pins are used.

Video input (pin 19).

The video input is connected to this pin coupled via a 10nF capacitor. A video signal between 0.5V and 2.5V peak to peak is required.

BLC (pin 17).

Black level capacitor. A 10nF capacitor connected to ground is required.

WLC (pin 18).

White level capacitor. A 10nF capacitor connected to ground is required.

TCR(pin22)

Time constant resistor. A 10K resistor is required to V_{DD}.

DATA I/O and **SYNC I/O** (pins 15 and 14 respectively).

The two outputs from the internal data slicer are fed via two tri-state buffers to the inputs of the data acquisition logic circuits. These two pins can be used to inject an external data and sync pulse train into the data acquisition circuits or to use the output of the internal data-slicer, depending on the state of EXT/INT.

EXT/$\overline{\text{INT}}$ (pin 16).

When this pin is held low the data acquisition circuits use the data and sync pulse trains from the internal data slicer. When high it permits external data and sync signals to be fed directly into the data acquisition circuits.

$\overline{\text{XTI}}$ & XTO (pins 3 and 4).

This pair of pins are designed to drive a 27.75000 MHz fundamental or third overtone quartz crystal. If a third overtone type is used, two external components are required to ensure operation at the correct frequency. Typical external components are, a 33nF capacitor and a 1µH. inductor in series and in parallel with the crystal. A 1MΩ resistor is included on chip between XTI and XTO to bias the input to its correct operating region. The crystal should be within ± 100 p.p.m. of the nominal frequency over the operating temperature range.

XCK (pin 4).

This pin is a clock output running at 13.875 MHz. It can be used as a stable clock for other components.

A0-A9(pins 34, 36, 35, 8, 7, 6, 9, 5, 12, 29 respectively).

DRAM address lines.

D0 (pin 11).

DRAM data line to bank 0

D1 (pin 10).

DRAM data line to bank 1

$\overline{\text{CAS}}$ (pin31).

DRAM column address strobe

$\overline{\text{RAS}}$ (pin 33).

DRAM row address strobe

$\overline{\text{WR}}$ (pin 32).

DRAM read/not write signal

TEST(pin 30).

This pin is used for internal testing and should be held low for the normal operation of the chip.

$\overline{\text{EVENT}}$ (pin 39).

An active low open drain output intended to interrupt a microprocessor when an important event occurs on either data acquisition circuit. The EVENT/A /B register bits uniquely describe which type of event has occured.

CSO OUT, BLUE, GREEN RED, BLANK (pins 28, 26,25,24,23).

These pins are high power RGB outputs allowing direct connection to display circuits without further buffering.

Y (pin 27).
This pin is a logical OR of the R.G.B. ouputs

SCL & SDA (pins 37 & 38 respectively)
Standard connection to I²C bus. The MV1815 can work at frequencies to a maximum of 1 MHz.

$\overline{\text{RESET}}$ (pin 13).
The active low reset input. This input has a nominal 150 KΩ resistor coupled to V_{DD} and a schmitt input buffer, allowing a simple external circuit consisting of a 1µF capacitor to ground to perform a power - on reset pulse of sufficient duration to allow the crystal oscillator to stabilize. When held low this input resets all registers to default setting and initalises counters.

MV1815 REGISTER ACCESSING VIA I²C

The MV1815 has twelve read registers and nineteen write registers. The I²C - bus slave address is "001001W/R".

When the MV1815 is addressed on the I²C bus as a slave transmitter, i.e. the eighth data bit is high, it will acknowledge the address byte, then transmit the contents of register address #0 to #10 in numerical order, if the master receiver continues to issue clock and acknowledge pulses. After transmitting register 10 contents, the register address will be set to #17, the RAM data register. The contents of RAM will be transmitted from the starting address set in the memory address registers. Each further transmitted byte increments the memory address by one, rather than the register address.

When addressed as a slave receiver, i.e. the eighth data bit is low, the MV1815 will acknowledge the address byte. The first data byte received by the MV1815 sets the register address counter. This defines the address of the register that will be written to by the following byte. Subsequent transmitted bytes will increment the register address by one each time, and the data will thus be written to all numerically higher registers, until the address reaches #17, the RAM data register. All subsequent received bytes will increment the memory address by one and be written to RAM. Whenever a stop condition occurs while the MV1815 is addressed as either a receiver or transmitter, the register address counter will be reset to zero.

READ REGISTERS

EVENT A/B - Event Registers (register numbers 0 & 1).

These are interrupt registers, designed to quickly notify the controlling microprocessor about the major acquisition events, so that the microprocessor is relieved of the task of polling memory for information regarding the reception of data. The EVENT output is set low when any one of six major events occurs in either of the acquisition circuits. Multiple events will set multiple bits in the registers, which will be cleared when the appropriate registers have been read, as will the EVENT output.

The events that are notified using this register are:- New page received, Valid header received, receipt of non-display packets and control bits C8 and C10, though these bits do not set the EVENT output.

CBITS A/B - Control Bit Registers (register numbers 2 & 6).

These registers display the remaining eight control bits, C5, C6, C7, C9, C11, C12, C13 and C14 received in the last valid header for each acquisition circuit.

PGR 1/2/3 A/B - Page Received Registers. (register numbers 3,4,5,7,8 & 9).

These registers show the exact page number and sub code of the received page.

HAMMC - Hamming Correction Counter. (register number 10).

To aid correct tuning of the receiver, each Hamming protected character received with other than exactly correct Hamming protection, will increment this counter. Thus by regularly reading this count, and monitoring its rate of increase, a good indication is given of the signal quality.

RDATA - RAM Contents Register. (register number 17).

RD7 to RD0 - The video RAM data at the address set by HADD and LADD registers, can be read from this register.

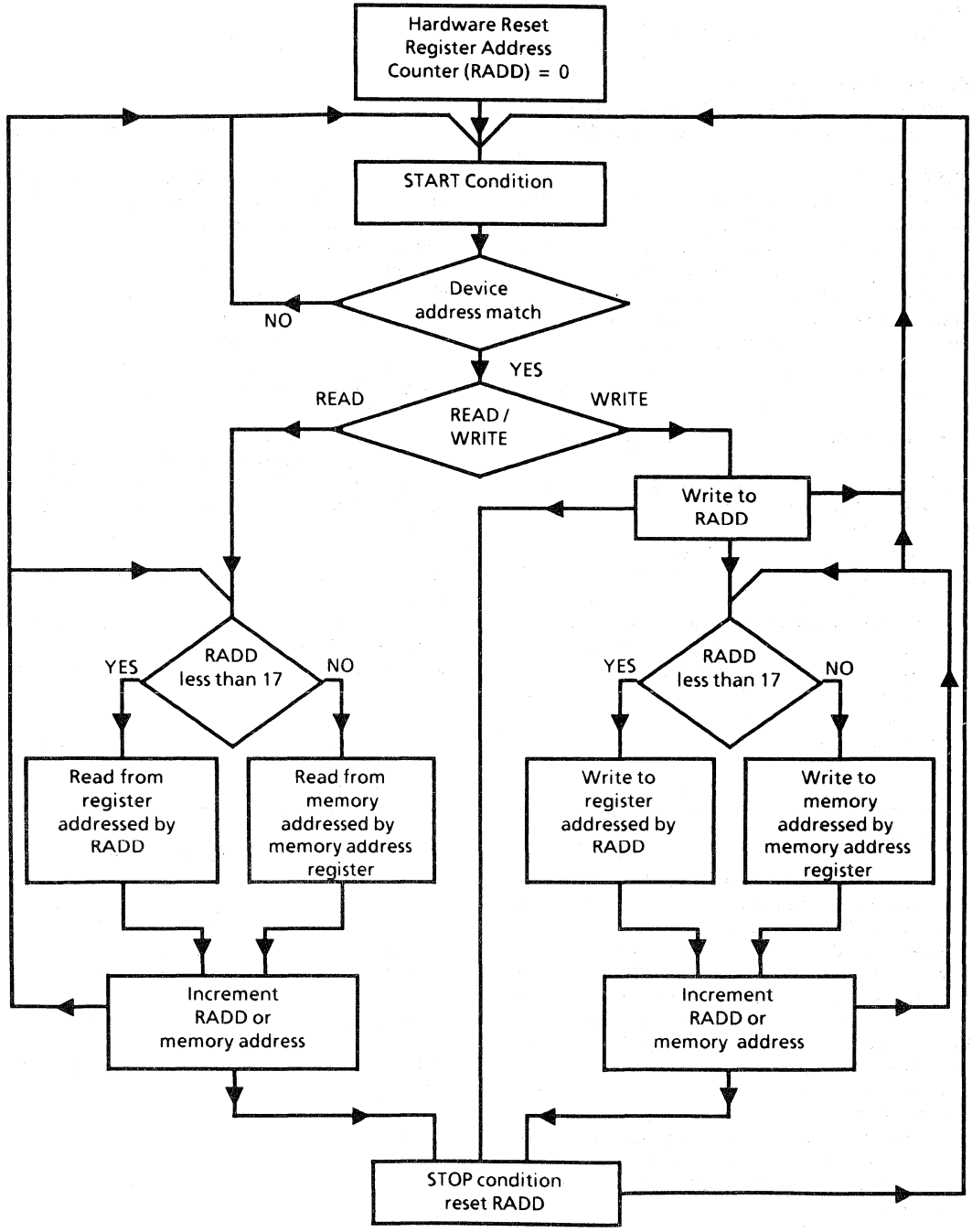


Figure 4. Memory addressing using I²C bus

WRITE REGISTERS

RADD - Register Address Counter.

The first data byte transmitted in any write sequence is the address of the first register to be written to, (see figure 4). Bits 0 to 4 define the register address. An Auto Increment Inhibit bit, disables the auto incrementing of the register or RAM address. The other two bits set the quadrant in which the memory address registers work.

ACON A/B - Acquisition control registers for A and B acquisition circuits (register numbers 1 & 5)

These two registers control the acquisition of data. They control which acquisition circuits are on and which of the magazine, page number or sub-code digits are of "don't care" status during reception of Teletext.

STOR A/B - Acquisition Store Select Registers (register numbers 1 & 6).

The eight bits in each register select which of the 254 page stores will be written to by each acquisition circuit The controlling microprocessor must ensure that the two registers are not written with the same value.

PGS A/B - Page Select Registers (register numbers 2,3,4,7,8 and 9)

These registers define the magazine, page and sub-page that each acquisition circuit will search for, depending on the information set in the ACON registers.

RECON - Receive Control Register (register number 10).

This register controls the data format of the teletext being received including the:-

Writing of Packet 0 to memory;
Writing of Packet 24 to memory;
Writing of Packet 25 to memory;
Parity check enable;
Accuracy of the framing code;
Full field or normal teletext data;
Rolling headers.

DISCON 1,2,3,4 - Display control registers (register numbers 11,12,13 and 14)

These four registers control the actual display of the teletext and picture. The features controlled include :-

Which acquisition circuit is displayed;
Language displayed;
Control of the display of the header;
Display of TEXT, PICTURE, or MIX;
Display of boxes of either text or picture;
Reveal of text hidden by "conceal" control codes;
Cursor control;
Control of separated graphics;
The display of lines 25 and 26;
Double height display of,
Top half of text,
Middle half of text,
Bottom half of text.

Double height of any area will be true double height, i.e. giving quad height characters if double height control characters are present. Double height control characters have no effect when on the bottom row of any displayed region.

HADD - High Address Word Register. (register number 15)

A8 to A15 - The high order address bits selecting one of the 256 sections of 256 bytes to be read through the data register.

LADD - Low Address Byte Register (register number 16)

A0 to A7 - The lower order address bits selecting one of 256 bytes in a given section. This register auto-increments after every read or write operation of the DATA registers if the AII bit is low. Auto incrementing of this register from FF to 00 will increment the HADD register, and overflow of HADD increments A16 & A17 in the RADD register.

WDATA - RAM contents Register. (register 17)

The video RAM data at the address set by HADD and LADD registers can be written via this register.

MEMORY ORGANISATION.

The display memory addresses as seen by the microprocessor via the I²C registers 'HADD' and 'LADD' bear little resemblance to the actual memory addresses that are used to store the data in the DRAMs, in conjunction with RAS and CAS strobes. This is of little consequence though to the system designer, unless he wishes to access the display DRAM data directly, which is inadvisable since the MV1815 needs access to the DRAMs during all TV lines.

The data address in HADD and LADD have been arranged as logically and as simply as possible, to allow a processor system easy access to the display (and non-display) data. Irrespective of the size of memory devices used, the lowest 2K (2048 bytes) of DRAM addresses, referred to as Store 0 and Store 1 contain all the non-display packets associated with the pages being acquired by both acquisition circuits. Space is reserved in Store 0 and Store 1 for up to 23 versions of packets X/26, X/27 or X/28. The only restriction is the total number of the three packets. These packets are stored in the same sequence as they are received. Reception of the same page will overwrite the memory space with new packets X/26, X/27 or X/28.

The first byte of rows 1 to 23 inclusive in both Store 0 and Store 1 can be read by the microprocessor to identify which non-display packet is stored in the particular row. This byte is made up of the 3 least significant bits of the packet number and the designation code value. In addition, packet 29's are stored in both stores and the two versions of packet 8/30 are stored, one in each of the two stores.

The lowest 24 bytes of store 0 (address 0000 to 0017 HEX) are allocated as follows. The first eight (0000 - 0007) are never written to by the MV1815 acquisition circuits. They are however read by the display circuits for display as the first eight characters in the top display row of the teletext page. This is normally where the requested page number is shown. There is no fixed format for this however and the MV1815 puts no constraints on what data is written to this part of the screen. When headers are 'rolling', MV1815 does not write any colour control characters to these locations. It is the responsibility of the control software to do this if it is required. It is therefore perfectly feasible to have red, yellow or cyan rolling headers to signify different states if so desired, or of course white, as the headers are actually transmitted. Allowing access to all eight characters allows a system to write e.g. "123-0001", or "432-XXXX", to show the magazine, page number and sub-code selected by the user, not just the page number as with previous systems. This address in store 1 is not used and may be used by the system for other purposes.

Address 0008 - 000F are written by the MV1815 acquisition circuit that is currently selected for display, with the last eight bytes from every header (packet 0) received by the MV1815 (or every header of the relevant parallel magazine). The only exception are 'out of sequence' headers, or if the 'WI0' bit is set, then no data will be written to these eight bytes. The microprocessor may then write them as required with, for instance, the time derived from packet 8/30. These eight bytes are displayed by the MV1815 as the last eight characters on the top display row, irrespective of which store is selected for display. Addresses 0010 - 0017 are used by the MV1815 to output packet 31 at receiver rate.

The display stores, 2 to 15 (63 or 255 if larger DRAMs are used), start at address 0800, the boundaries being in multiples of 1024 bytes, at 0C00, 1000 etc. (HEX). In each store, the first 24 bytes are nos. 14 to 37 inc. from the header for the requested page. The further 1000 bytes per store are used by packets 1 though to 25 (40 bytes per packet), in that order, irrespective of the order of the transmission.

TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH
2/3	£	#	#	£	é	ç	#
2/4	$	$	¤	$	ï	$	ů
4/0	@	§	É	é	à	¡	č
5/11	←	Ä	Ä	°	ë	á	ť
5/12	½	Ö	Ö	ç	ê	é	ž
5/13	→	Ü	Å	→	ù	í	ý
5/14	↑	^	Ü	^	î	ó	í
5/15	#	_	_	#	#	ú	ř
6/0	—	°	é	ù	è	¿	é
7/11	¼	ä	ä	à	â	ü	á
7/12	‖	ö	ö	ò	ô	ñ	ě
7/13	¾	ü	å	è	û	è	ú
7/14	÷	ß	ü	ì	ç	à	š

Table 2. International Character set

	COLUMN (bits 5,6, 7 & 8)							
ROW	0	1	2	3	4	5	6	7
0	Alpha Black	Graphic Black		0	@	P		p
1	Alpha Red	Graphics Red	!	1	A	Q	a	q
2	Alpha Green	Graphics Green	"	2	B	R	b	r
3	Alpha Yellow	Graphics Yellow	£	3	C	S	c	s
4	Alpha Blue	Graphics Blue	$	4	D	T	d	t
5	Alpha Magenta	Graphics Magenta	%	5	E	U	e	u
6	Alpha Cyan	Graphics Cyan	&	6	F	V	f	v
7	Alpha White	Graphics White	'	7	G	W	g	w
8	Flash	Conceal Display	(	8	H	X	h	x
9	Steady	Contiguous Graphics	)	9	I	Y	i	y
10	End Box	Separate Graphics	*	:	J	Z	j	z
11	Start Box	No action	+	;	K	←	k	¼
12	Normal Height	Black Background	,	<	L	½	l	‖
13	Double Height	New Background	-	=	M	→	m	¾
14	No action	Hold Graphics	.	>	N	↑	n	÷
15	No action	Release Graphics	/	?	O	#	o	

Table 3. Control Characters, Primary Character Set G0 and Mosaic Graphics Set G1

TIMING CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic		Value			Units	Conditions
		Min	Typ	Max		
SCL Clock frequency	f_{SCL}	0	100	1000	kHz	
Time the bus must be free before a new transision can start	t_{BUF}	4.7			µs	
Hold time start condition.After this periodthe first clock pulse is generated	$t_{HD;STA}$	4.0			µs	
Low period of clock	t_{LOW}	470			ns	All values refer to V_{IH} and
High period of clock	t_{HIGH}	400			ns	V_{IL} levels
Set up time DATA	$t_{SU;DAT}$	25			ns	
Rise time of SDA and SCL signals	t_R			1	µs	
Fall time of SDA and SCL signals	t_F			300	ns	
Set up time for STOP condition	$t_{SU;STO}$	4			µs	

Table 4 I²C Parameters

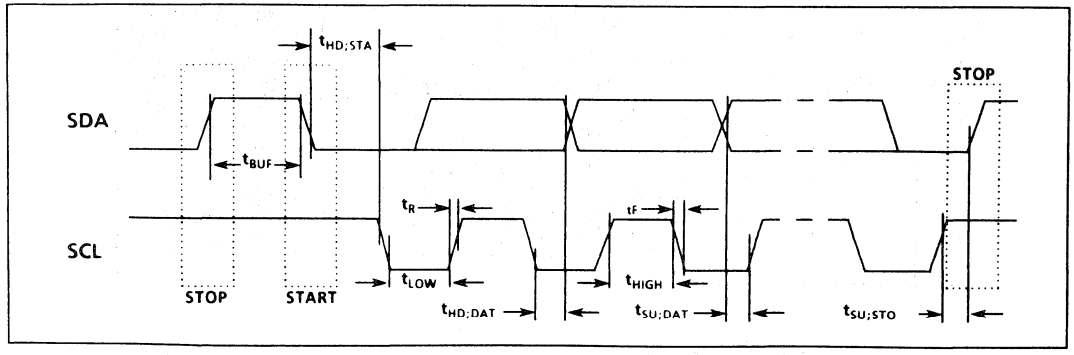


Figure 5 I²C bus timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
All Inputs (except XTI and TEST)						All inputs have 150KΩ pull-up resistor to V_{DD} except test
Input low current (source)		-10	-33	-100	µA	
Input high current (sink)				10	µA	
XTI and TEST inputs	3					
Input low current (source)	30			-10	µA	
Input high current (sink)				+ 10	µA	
SYNC and DATA inputs	14,15					
Input low voltage		-0.3		0.8	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
RESET, SDA, SCL input (Schmitt input)	13					
Input low voltage	38	-0.3		1.0	V	
Input high voltage	37	2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
Threshold voltage (rising)			1.85		V	V_{DD} = 5V
(falling)			1.05		V	V_{DD} = 5V
All other inputs						
Input low voltage		-0.3		1.5	V	
Input high voltage		3.5		5.3	V	$V_{IH\ MAX} = V_{dd} + 0.3V$
Outputs (A0 to A9,D0, D1, WE,CAS,RAS,EVENT)						
Output low (sink)		13	26		mA	V_{OL} = 0.4V
Output high (source)		21	45		mA	V_{OH} = 2.4V
XCK	4					
Output low(sink)		6.9	13		mA	V_{OL} = 0.4V
Output high(source)		10	22		mA	V_{OH} = 2.4V
Frequency			13.875		MHz	
XTO	2,					
Output low (sink)		6.9	13		mA	V_{OL} = 0.4V
(source)		10	22		mA	
Max Input Frequency, $F_{IN_{MAX}}$	3		27.75		MHz	

Table 5

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
R, G, B & Blanking outputs	23,24					
I_{OL}	25,26	23	43		mA	
I_{OH}	27	36	76		mA	V_{OL} = 0.4V
Composite sync I_{OL}		13	26		mA	V_{OH} = 2.4V
output I_{OH}	28	21	45		mA	
Video Input pin Input voltage	19	0.5		2.5	V	peak to peak
Operating temperature		0		70	°C	
Storage temperature		-65		150	°C	
Relative Humidity				85	%	
Absolute Max DC supply	21	-0.3		7.0	V	
	40					

Table 6

TIMING CHARACTERISTICS of DRAMS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic		Value			Units	Conditions
		Min	Typ	Max		
Access time from RAS	t_{RAC}			232	nS	DRAM timing
Access time from CAS	t_{CAC}			124	nS	characteristics required
RAS Precharge Time	t_{RP}			144	nS	by the MV1815
RAS Pulse Width	t_{RAS}			432	nS	
CAS Pulse Width	t_{CAS}			144	nS	
Row Address Hold Time	t_{RAH}			36	nS	
Column Address Hold Time	t_{CAH}	72			nS	
Data-inSet Time	t_{DS}	36			nS	
Data-in Hold Time	t_{DH}	72			nS	
	t_{CP}	108			nS	
	t_{PC}	252			nS	
Ramdon R/W Cycle Time	t_{RC}	576			nS	

Table 7 DRAM Parameters

PLESSEY
Semiconductors

MV1830

TELETEXT DATA BUFFER

The MV1830 is a 64 x 9 sequential data buffer designed to be used with the MV1812 Teletext Data Acquisition Circuit. The MV1830 can be used singly, or can be cascaded so that the data from multiple VBI lines may be stored, allowing time for a slow system to read the data during the rest of the frame period.

FEATURES

- 10MHz Guaranteed Cascade Rate
- <150mW Power Dissipation at 10MHz
- <55mW Standby
- Single +5V Supply
- Tri-state Outputs

ASSOCIATED PRODUCTS

MV1812 Teletext Data Acquisition circuit
SL9100 Teletext Data Slicer and Clock

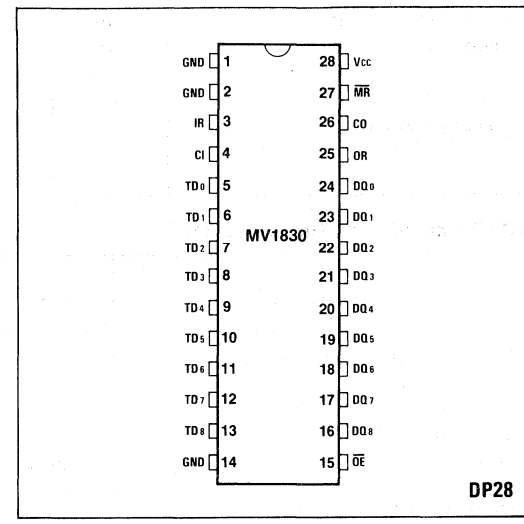


Fig.1 Pin connections - top view

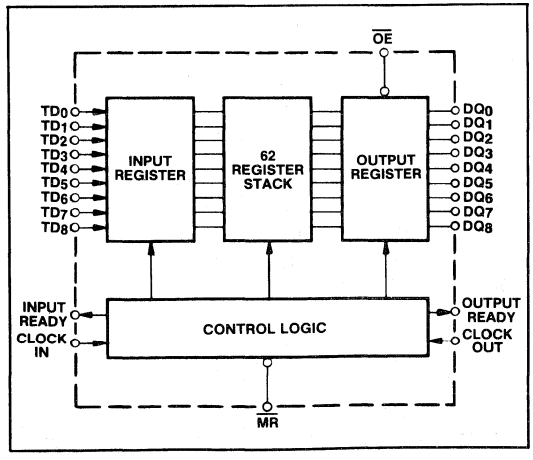


Fig.2 Block diagram

BUFFER OPERATION

The MV1830 data buffer contains 64 nine-bit data registers. Data is initially loaded from the data inputs TD0-TD8 by applying a low to high transition on the Clock In (CI) input. Input Ready (IR) goes low indicating that data has been entered into the first register and the input is unable to accept more data. When CI goes low again, the fall through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second and IR goes high indicating that the buffer is ready to accept new data.

Data falling through the registers stacks up at the output end. A high level on OR indicates that there is valid data waiting on DQ0-8. A Clock Out (CO) can then be used to shift data out of the buffer. The low to high transition on CO causes Output Ready (OR) to go low indicating that the data on the outputs may no longer be valid. When CO goes low, the data in the next to last register moves into the last register and OR goes high again.

The depth of the buffer can be extended by connecting the data outputs of one device to the inputs of the next, as shown in Fig.10. The Input Ready pin of the receiving device is connected to the Clock Out pin of the sending device. Similarly the Output Ready pin of the sending device is connected to the Clock In pin of the receiving device.

Master Reset ($\overline{MR}$) is used to reset the control logic and remove the data from the outputs (i.e. resets to all zeros).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.5V to +5.5V

DC Characteristics

Characteristic	Symbol	Value		Unit	Conditions
		Min.	Max.		
Output high level	V_{OH}	2.4		V	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OH} = -1mA$
Output low level	V_{OL}		0.5	V	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OL} = 8mA$
Input high level	V_{IH}	2		V	
Input low level	V_{IL}		0.8	V	
Input leakage	I_{IN}	-10	+10	μA	$V_{IN} = V_{IH}$ or V_{IL}
Output leakage GND $\leqslant V_{OUT} \leqslant V_{CC}$	I_{OZ}	-50	+50	μA	V_{CC} = +5.5V
Short circuit current	I_{OS}		80	mA	Note 8
Supply current	I_{CC}		30	mA	V_{CC} = +5.5V T_{amb} = 70°C I_{LOAD} = 0mA
Standby current			10	mA	V_{CC} = +5.5V I_{LOAD} = 0mA All inputs at V_{IL}

AC Characteristics - Using test circuit

Characteristic	Symbol	Value		Unit	Conditions
		Min.	Max.		
Maximum operating frequency	f_O	10		MHz	Note 1
CI HIGH time	t_{PHCI}	30		ns	
CI LOW time	t_{PLCI}	40		ns	
Data setup to CI	t_{SCI}	0		ns	Note 2
Data hold from CI	$t_{HCI\ (a)}$	50		ns	Note 2 and 3
	$t_{HCI\ (b)}$	t_{PHCI} + 5		ns	
Delay, CI HIGH to IR LOW	t_{DLIR}		30	ns	
Delay, CI LOW to IR HIGH	t_{DHIR}		40	ns	
CO HIGH time	t_{PHCO}	30		ns	
CO LOW time	t_{PLCO}	40		ns	
Delay, CO HIGH to OR LOW	t_{DLOR}		30	ns	
Delay, CO LOW to OR HIGH	t_{DHOR}		40	ns	
Data setup to OR HIGH	t_{SOR}	-20		ns	
Data hold from CO LOW	t_{HCO}	10		ns	
IR pulse HIGH	t_{PIR}	9		ns	
OR pulse HIGH	t_{POR}	10		ns	
Data setup to IR	t_{SIR}	0		ns	Note 5
Data hold from IR	t_{HIR}	50		ns	Note 5
Bubble through time	t_{BT}		2400	ns	
$\overline{MR}$ pulse width	t_{PMR}	60		ns	Note 6
$\overline{MR}$ HIGH to CI HIGH	t_{DCI}	60		ns	
$\overline{MR}$ LOW to OR LOW	t_{DOR}		60	ns	
$\overline{MR}$ LOW to IR HIGH	t_{DIR}		60	ns	
$\overline{MR}$ LOW to output LOW	t_{LZMR}		60	ns	Note 4
Output valid from $\overline{OE}$ LOW	t_{OOE}		60	ns	
Output HIGH-Z from $\overline{OE}$ HIGH	t_{HZOE}		60	ns	

NOTES
1. $1/f_O > t_{PHCI} + t_{DHIR}$, $1/f_O > t_{PHCO} + t_{DHOR}$.
2. t_{SCI} and t_{HCI} apply when memory is not full.
3. Hold time is the lesser of the two parameters (a) and (b).
4. All data outputs will be at LOW level after reset goes high until data is entered into the buffer.
5. These times apply when the device is full and CI is held high.
6. For cascade applications, t_{PMR} must be double that specified above.

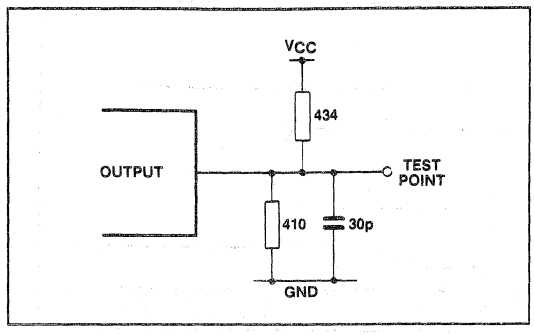


Fig.3 Test circuit

ABSOLUTE MAXIMUM RATINGS (Note 7)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN} (see Note 9)	-0.9V to V_{CC} +0.9V
DC voltage applied to output when high impedance	-0.5V to 7.0V
Clamp diode current per pin (see Note 8)	+18mA
Storage temperature T_S	-65°C to +150°C

NOTES
7. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
8. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
9. Input voltages more negative than —0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

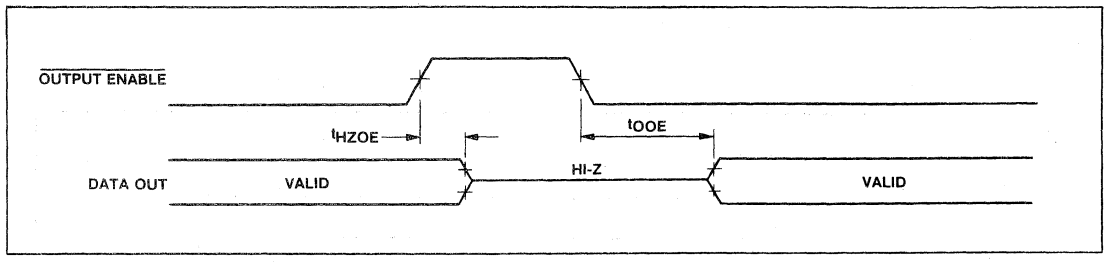


Fig.4 Output enable timing

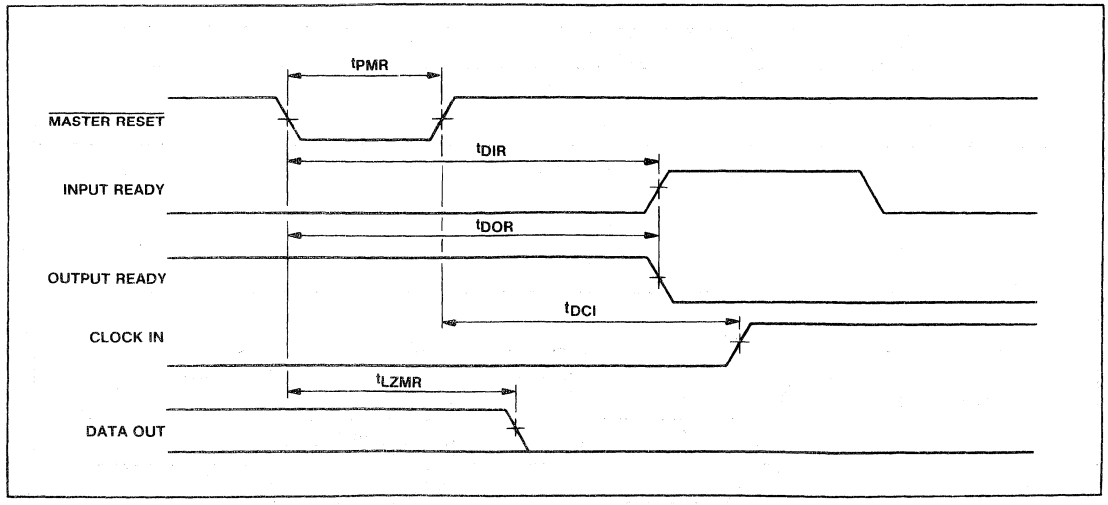


Fig.5 Master reset timing

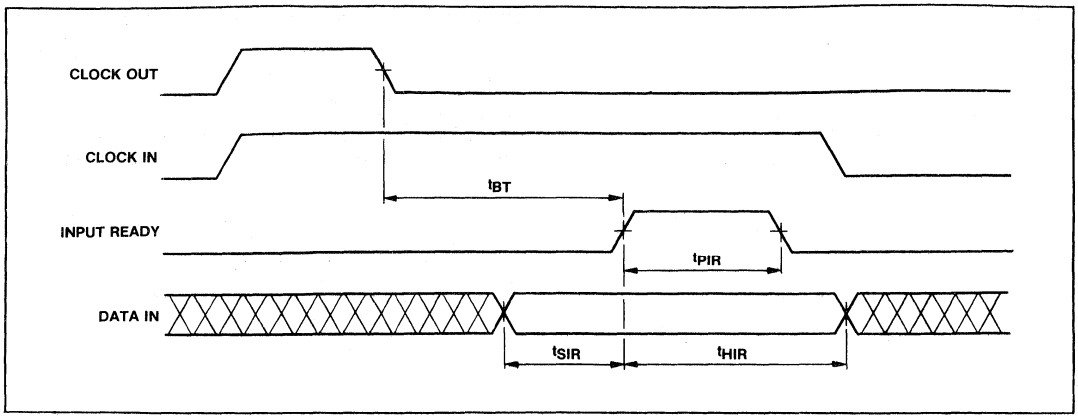


Fig.6 Data Out to Data In bubble through time

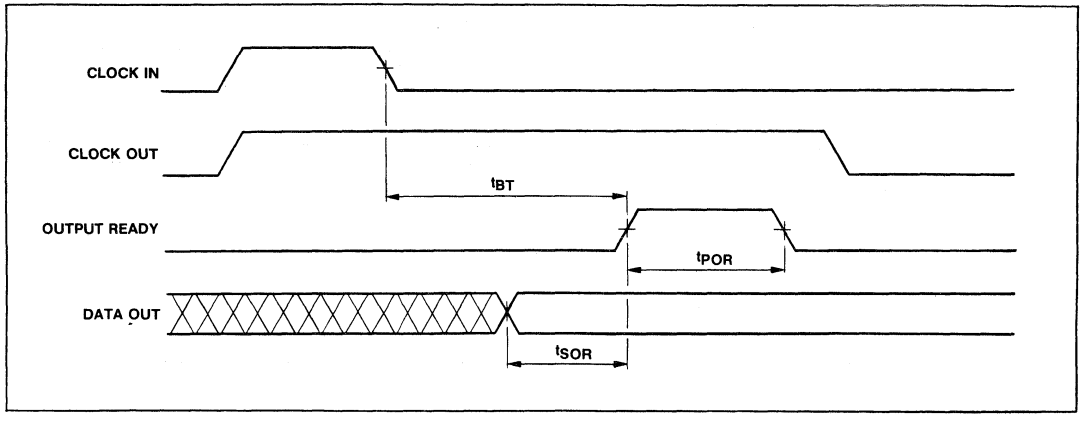


Fig.7 Data In to Data Out bubble through time

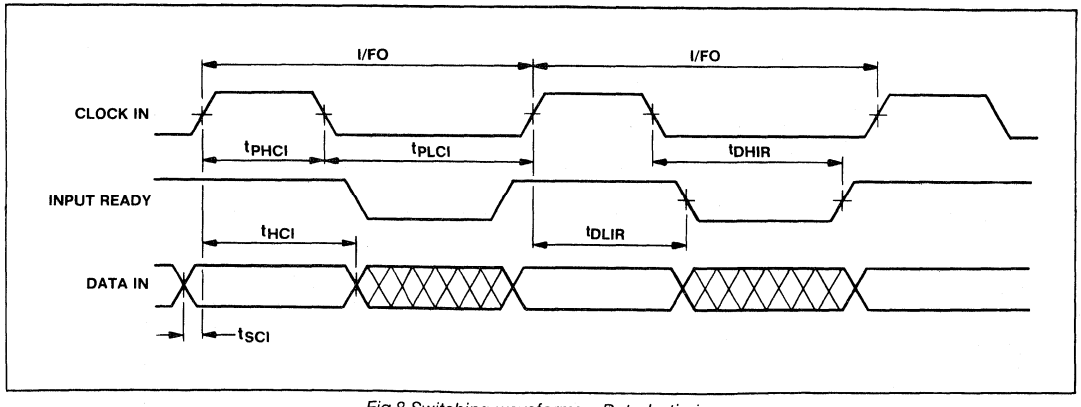


Fig.8 Switching waveforms - Data In timing

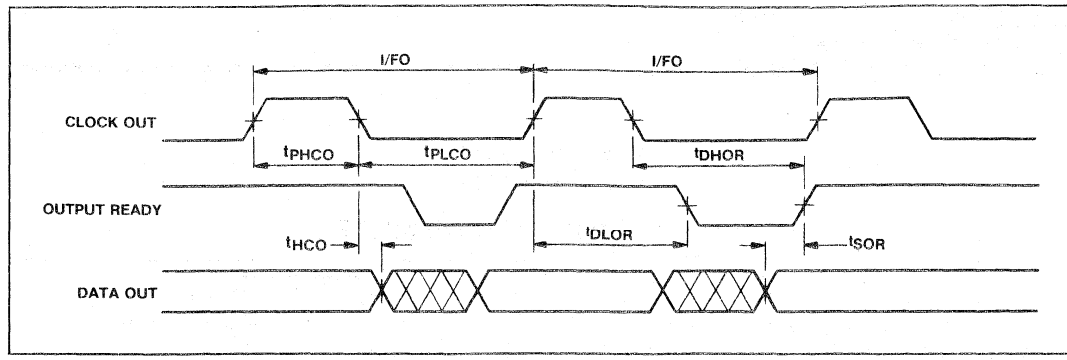


Fig.9 Switching waveforms - Data Out timing

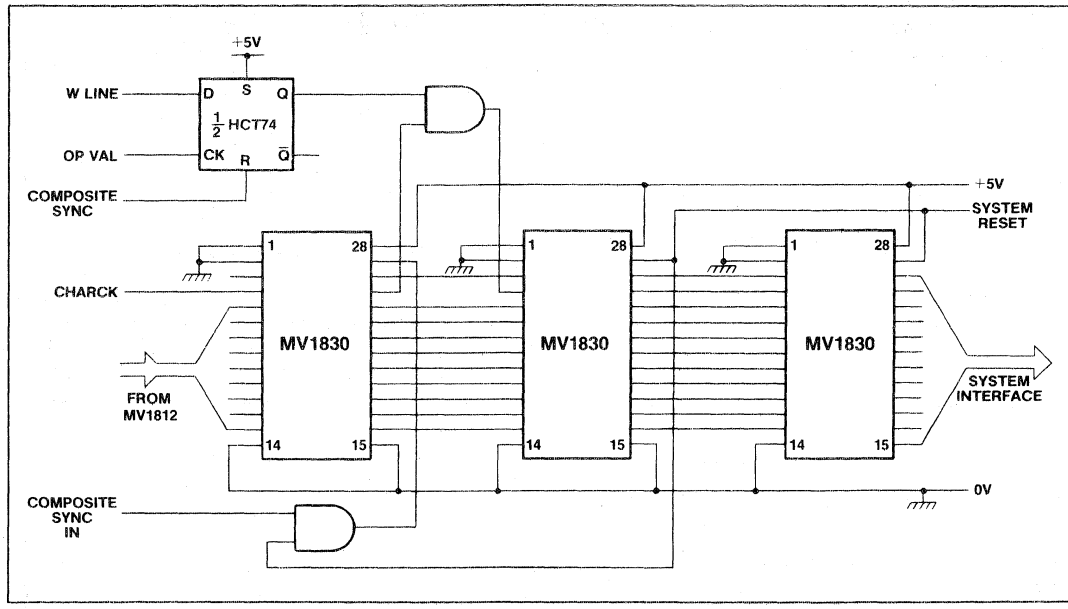


Fig.10 Interface to MV1812

USER NOTES

1. When the buffer is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on CO, the OR signal always goes LOW before there is any change in output data.
3. If CO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the buffer to the output. OR will go HIGH for one internal cycle (t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the buffer, they will line up behind the first word and will not appear on the outputs until CO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If CI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the buffer and IR will return to the LOW state until CI is brought LOW. If CI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the buffer until CI goes HIGH.

MV2000

REMOTE KEYBOARD TRANSMITTER

The MV2000 is a fully integrated keyswitch encoder and pulse position modulation (PPM) transmitter, designed for the encoding of a keyboard with up to 88 switches.
Three seperate shift or control inputs are also provided to give up to eight functions for each keyswitch.
The PPM output may be used to drive an infra-red LED for remote keyboard operation or provide a simple direct wire link to a VDU.
The output codes are intended to be decoded directly by a microprocessor.

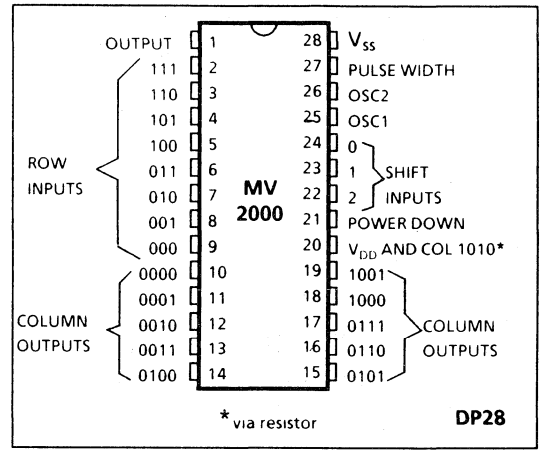


Fig 1 Pin Connections (top view)

FEATURES

- Infra-red transmission for remote operation
- Very low supply current
- PPM output gives excelent immunity from noise and multi path reflections
- Error check code for data integrity
- Few external components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5V to 11V
Input voltage (all pins)	-0.5V to V_{DD} + 0.5V
Operating temperature range	0°C to + 70°C
Storage temperature range	-55°C to + 125°C

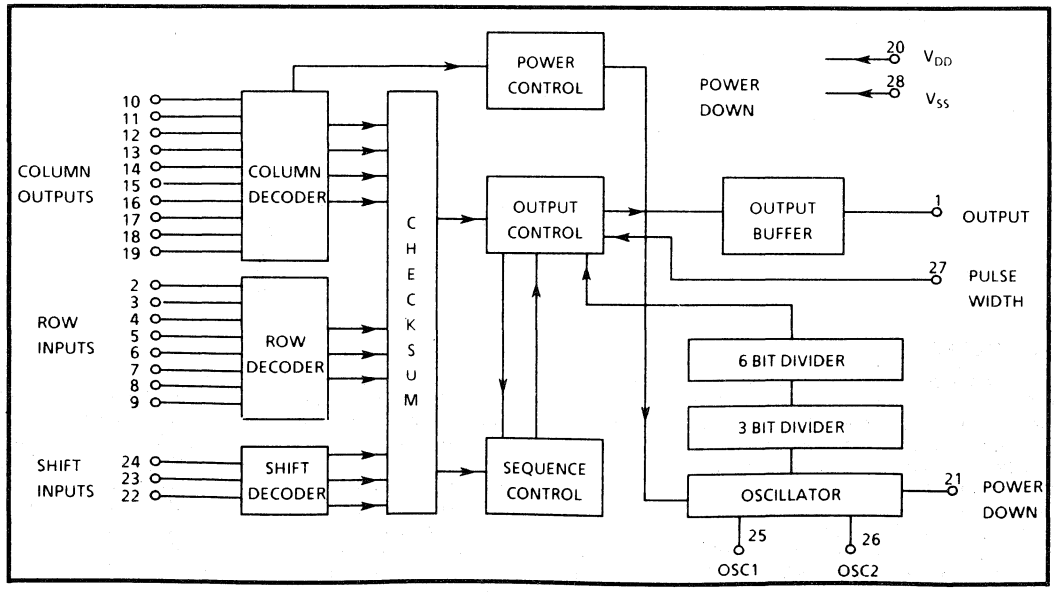


Fig MV2000 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +3V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Operating supply current	20		2.5	10	mA	Circuit fig 4
Standby supply current	20		0.1	2	µA	All inputs open circuit
Output source current	1	100	200	300	mA	V_{DD} = 9V, V_{OH} = 1V
		50	100	200	mA	V_{DD} = 6V, V_{OH} = 1V
Keyboard contact resistance	2-19					
Closed		0		20	kΩ	
Open		100		∞	kΩ	
Oscillator Frequency	25,26	200	500	4000	kHz	
				10	MHz	V_{DD} = 10.5V

PIN DESCRIPTIONS

Pin No.	Description
1	Totem pole output for driving NPN switching transistor
2-9	Keyboard matrix row inputs (7-0)
10-19	Keyboard matrix column outputs (0-9)
20	Positive supply, V_{DD}. Also column 10 via resistor
21	Power down input - normally held at V_{DD}. Taking this input low will force the device into its power down state
22-24	Shift/Control inputs, may be pulled high or low by resistors or connected directly to V_{DD} or V_{SS}
25	Oscillator 1 - input to internally biased inverter. May be driven from external source
26	Oscillator 2 - output of internally biased inverter
27	Pulse Width input - time constant determines output pulse width
28	Negative supply, V_{SS}

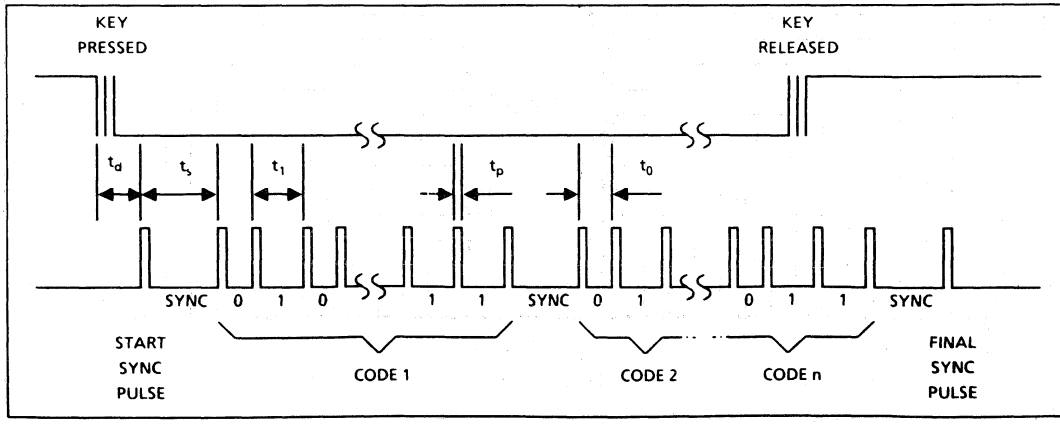


Fig 3 PPM Data Timing

TIMING (see fig 3)

Delay time, t_d = 1024 clock cycles (min)
Sync time, t_s = 2560 clock cycles
Logic 0 time, t_0 = 1536 clock cycles
Logic 1 time, t_1 = 2048 clock cycles
Pulse time, t_p, determined by time constant on pin 27

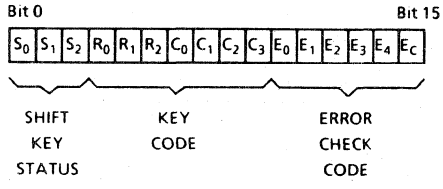
Ratio $t_0:t_1:t_s$ = 3:4:5

CODE FORMAT

A sixteen bit code is output, consisting of a seven bit key code, three shift key status bits and a six bit error check code.

MSB LSB
Key Code = $C_3C_2C_1C_0\ R_2R_1R_0$
(COLUMN) (ROW)

Transmitted sequence:- (Bit 0 transmitted first)



The Error Check Code is obtained by first adding the two halves of the previous ten bits of the code (LSBs first) and then inverting the resultant 6-bit code (E_C being the carry bit).

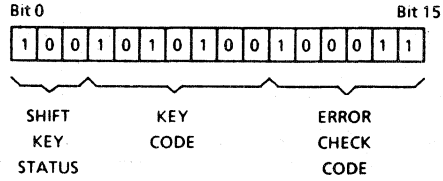
ie. $R_1 R_0 S_2 S_1 S_0$
$C_3 C_2 C_1 C_0 R_3$ +
$\overline{E_C E_4 E_3 E_2 E_1 E_0}$

Example

Shift 0 input held at V_{DD}
Shift 1 and 2 inputs held at V_{SS}
Column 2 connected to Row 5

Key Code = 0 0 1 0 1 0 1
(COLUMN) (ROW)

Transmitted sequence:-



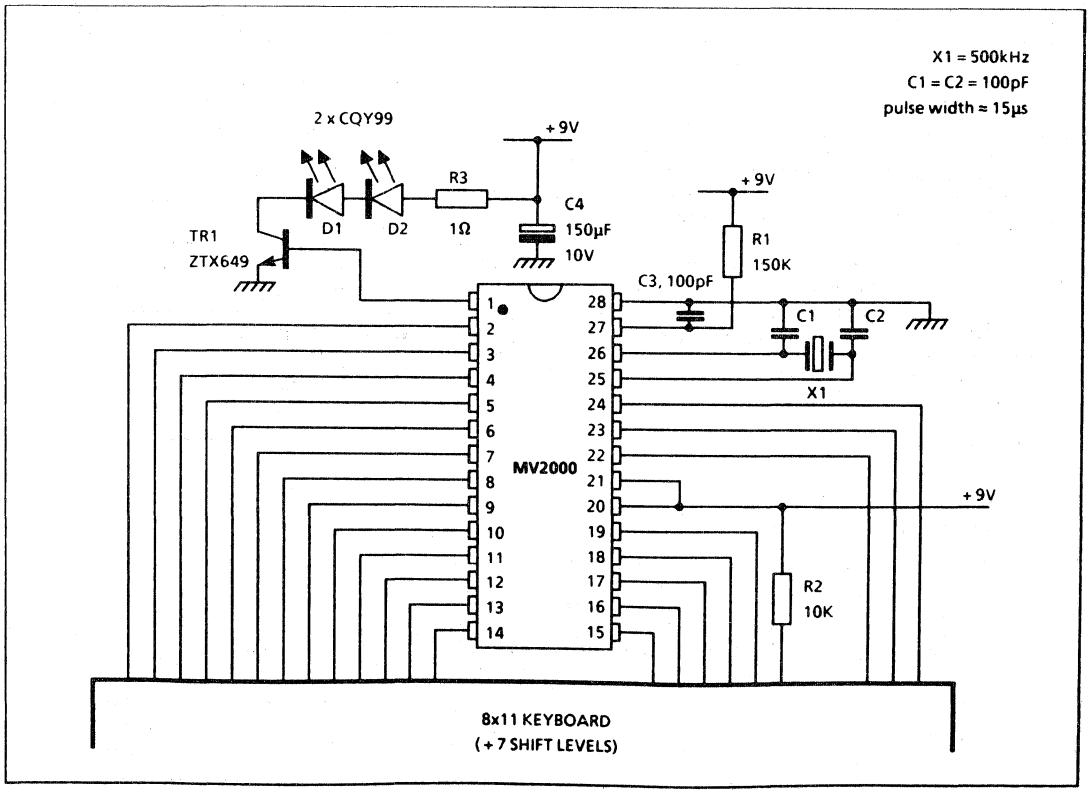


Fig 4 Infra-Red Application Circuit

OPERATION

The circuit diagram of Fig. 4 shows a typical application using the MV2000 with data being transmitted via an infra-red link. Until a key is pressed, the device remains in its standby mode with power internally disconnected from the oscillator and most of the logic to minimise the drain on the supply.

When a column and a row are connected by the pressing of a key, power is applied to the rest of the device, the oscillator started and a delay imposed before any change at the output occurs. After this time, an initial synchronising pulse is transmitted, followed by the code word, which is repeated, separated by sync bits, for as long as the key remains pressed (Fig. 3). When the key is released, the word being transmitted is completed. If another key is pressed, the code for this new key is transmitted immediately following the end of the code for the previous key, but separated from it by a sync bit. If no other key is pressed, a final sync pulse is added to the end of the last word to be transmitted and the MV2000 then returns to its power down mode.

If more than one key is pressed at the same time, the code transmitted will be that corresponding to the first key detected in the matrix scan of the keyboard.

Pressing one or more of the "shift" keys on the keyboard in conjunction with another key changes the state of the corresponding shift bits in the code transmitted. Pressing a shift key on its own does not initiate a transmission.

In any design using the MV2000 for infra-red transmission, consideration must be given to the arrangement of diodes used, possibly using a small resistance in series to limit the current. The transistor TR1 must also be chosen such that its characteristics include high current gain and fast switching speeds.

PLESSEY
Semiconductors

MV95308

8-BIT 30MHz DIGITAL TO ANALOG CONVERTER

The Plessey CMOS MV95308 has been designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the reference amplifier and reference voltage source on chip.

The device also contains an input register and registered video controls (Blank, Ref. White, Over Bright and Sync.). These control inputs and associated internal circuitry allow the MV95308 to be used in video graphics systems.

A control on/off input also allows the video pedestals to be overridden for conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard (RS343) video levels.

Pullup resistors have been added to tie all unused inputs into their inactive states.

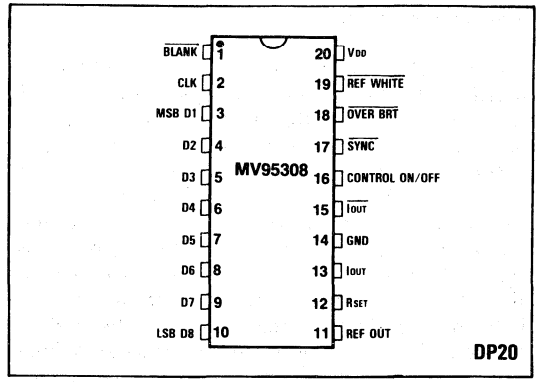


Fig.1 Pin connections - top view

ORDERING INFORMATION

MV95308 C DP (Industrial - Plastic DIL package)

FEATURES

- Low Power
- RS 343 Compatible Levels
- 20ns Settling to ±1 LSB
- On Chip Reference Voltage Source
- Graphics Ready
- Registered CMOS Inputs
- Guaranteed Monotonic
- Drives 75 Ohm Loads Directly
- Single 5V Power Supply
- 0°C to +70°C Temperature Range
- 7ns Output Rise Time (10% to 90%)

APPLICATIONS

- Data Conversion (General)
- Commercial TV
- Computer Graphics
- Instrumentation
- Test Equipment
- Waveform Synthesis

RECOMMENDED OPERATING CONDITIONS

R_{Load} (both outputs)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8k
R_{SET} (other DAC applications)	1.2k

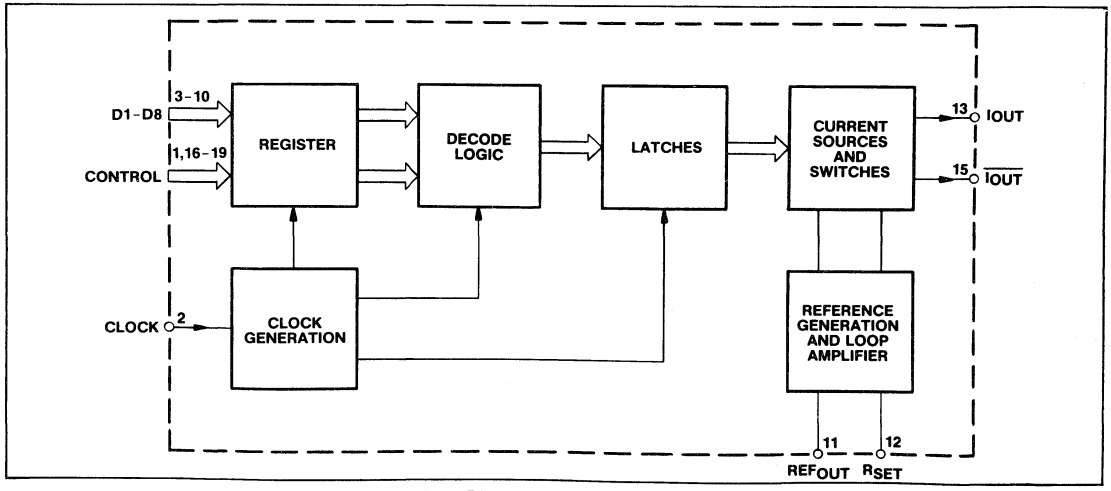


Fig.2 Block diagram of MV95308

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{DD} = +5V ± 0.5V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		58	70	mA	
Resolution		8			Bits	
Differential linearity				±1	LSB	R_{SET} = 1.8k
Integral linearity				±1	LSB	R_{SET} = 1.8k
Internal reference voltage	V_{ref}		1.0		V	Pin 11
Update rate	f_C	30	50		MHz	
Maximum output current	I_{out}	16			mA	
Clock minimum high	t_H	7			ns	
Clock minimum low	t_L	7			ns	
Input voltage high	V_{INH}	3			V	
Input voltage low	V_{INL}			1.2	V	
Data input current				20	μA	V_{IN} = 5.0V (At f_{max})
Output rise time	t_r			6	ns	10% to 90%
Settling time	t_{st}			20	ns	To ±1 LSB (75Ω load)
Clock to output delay	t_i		6		ns	Output at 10% full scale
Glitch energy			<100		ps V	

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Storage temperature	-55°C to 125°C
Chip temperature	150°C

THERMAL CHARACTERISTICS

Chip to case θ_{JC}	30°C/W
Chip to ambient θ_{JA}	86°C/W

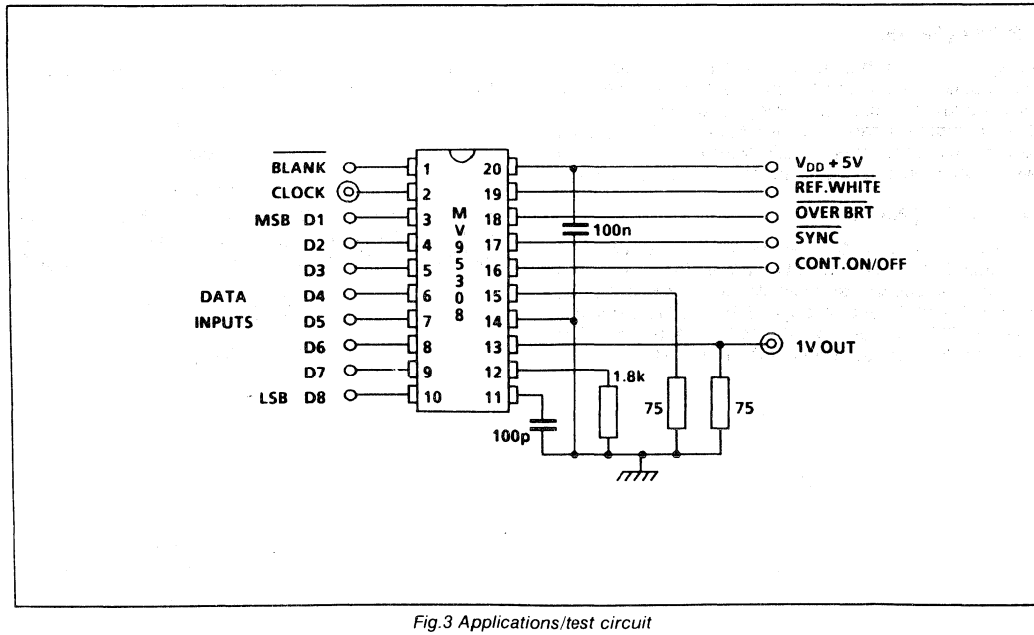


Fig.3 Applications/test circuit

OPERATING NOTES

For optimum performance the device should be used in a low profile socket located over a solid ground plane. It is also important that the decoupling capacitor on pin 20 (V_{DD}) is located close to the device pin.

The outputs from this D to A converter are open drain current sources and hence require pulldown load resistors. The value of the load resistors will therefore determine the peak to peak output voltage from the DAC. This should not exceed 1.2V.

With all the data inputs high and a load of 75Ω on each output, a full scale output of 1V will be seen, (Fig.3). Fine adjustment of the output voltage can be achieved by varying the value of R_{SET}. Increasing R_{SET} will decrease the output amplitude.

For optimum slew rate and settling time, the unused output should be connected to ground via the same resistance as on the used output. This will balance the currents within the output stage of the DAC and hence provide cleaner switching.

Table 1 shows the output currents from the MV95308 with combinations of input data and control settings.

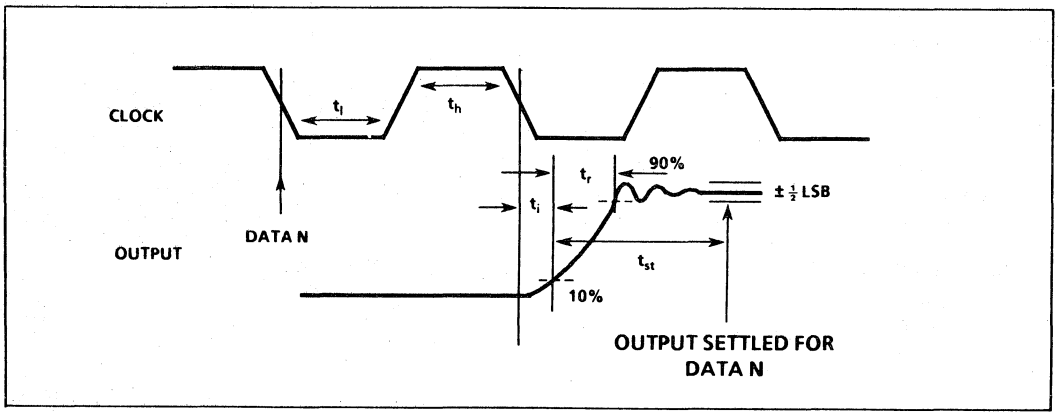


Fig.4 Timing diagram

Over Bright (Pin 18)

This control input has been introduced specially for graphics applications. It can be used to illuminate areas of graphics displays for borders, headings or cursors etc. When held low this input will cause a 10% of blank to full white level increase in the output current. Unlike the other control inputs the over bright input does not override the data. See Table 1.

Control On/Off (Pin 16)

This feature allows the MV95308 to be used in conventional DAC applications. When held low this pin will remove the sync pedestal and disable the Over Bright input. This allows the full 1V output range of the DAC to be used, 0 to 13mA into 75Ω. To gain this extra active output range, it is necessary to decrease the value of R_{SET} to 1.2kΩ.

With the control on/off pin low and all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}}$$

V_{ref} = 1.0V typ.

With the control on/off input open circuit the device will be configured for video graphics. In this mode and with all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}} + 4.533\text{mA}$$

V_{ref} = 1.0V typ.

Description	Control On/Off	Sync Bar	Blank Bar	Ref. White Bar	10 % Over.BRT Bar	Input Data	I_{OUT} (mA) R_{SET} = 1.8k
Ref. White +10 %	1	1	1	0	0	X	14.285
Ref. White	1	1	1	0	1	X	13.333
Full White	1	1	1	1	1	FF	13.333
Over Bright	1	1	1	1	0	Data	I_{CODE} +0.952
Full Black	1	1	1	1	1	00	4.533
Blank	1	1	0	X	X	X	3.183
Data-Sync	1	0	1	1	1	Data	I_{CODE} -3.813
Sync	1	0	0	X	X	X	0.000
Control On/Off	0	X	1	1	X	Data	I_{CODE} (0 to 13mA) R_{SET} = 1.2k

Table 1

X = Don't Care '1' = +5V, '0' = 0V, FF = All '1's

PLESSEY
Semiconductors

SL486

INFRA RED REMOTE CONTROL PREAMPLIFIER

The SL486 is a high gain preamplifier designed to form an interface between an infra-red receiving diode and the digital input of remote control receiving circuits. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

FEATURES

- Fast Acting AGC Improves Operation in Noisy Environments
- Differential Inputs Reduce Noise Pick-up and Improve Stability
- Gyrator Circuit Allows Operation in Environments with High Brightness Background Light Levels
- Output Pulse Stretcher for use with Microprocessor Decoders
- On-Chip Stabiliser Allows Operation with a Wide Range of Supply Voltages
- Direct Interface to Plessey MV601 and ML920 Series Remote Control Receivers
- Low Noise Output

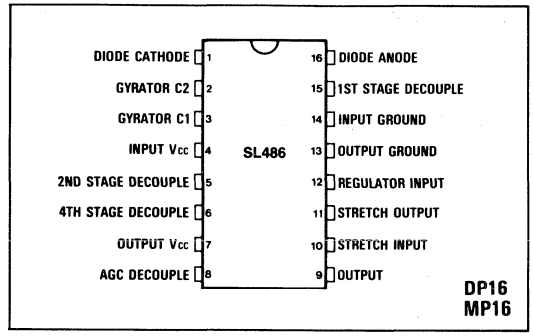


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V Pins 4 & 7)	+10V wrt V Pins 13 & 14
Regulator input voltage (V Pin 12)	-20V wrt V Pin 7
Output current	5mA
Stretch output current	5mA
Operating temperature range	0°C to +70°C
Storage temperature	-55°C to +125°C

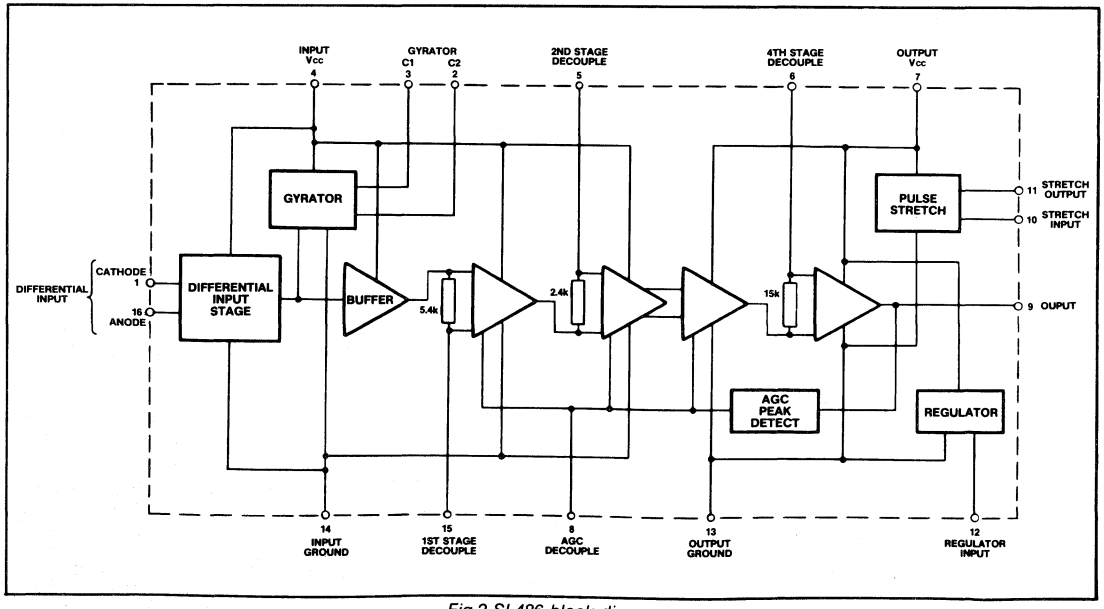


Fig.2 SL486 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C, V_{CC} = 4.5V to 7.0V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current (See Note 1)	4,7		6.5	9.0	mA	V_{CC} = 5.0V, I_{DIODE} = 1.0μA } Pins 13 & 14
	4	3.5+3xI_D	4.2+3xI_D	5+3xI_D	mA	V_{CC} = 4.5V, $I_{DIODE} \leqslant$ 1.5mA } ground
	4,7		8.5	10	mA	V_{CC} = 18V, I_{DIODE} = 1.0μA Pin 12 ground
Low voltage supply (external)	4,7(+ve), 13,14(-ve)	4.5		9.5	V	Input and output V_{CC} commoned, input and output ground commoned
High voltage supply (external)	4,7(+ve), 12(-ve)	8.4		18.0	V	Input and output V_{CC} commoned, input and output ground at internal regulated voltage
Internal regulated voltage	13(wrt 7)	5.9	6.2	6.5	-V	V Pin 7(+) to V Pin 12(-) = +16V
Voltage between input and output V_{CC}	4,7			1.5	V	At room temperature
				1.1	V	At 70° C
Minimum sensitivity of differential input	1,16	9.0		2.3	nA	I_{DIODE} = 1.0μA
		74.0		18.5	nA	I_{DIODE} = 100μA
		168.0		42.0	nA	I_{DIODE} = 0.5mA
Common mode rejection	1,16		35.0		dB	
Maximum signal input	1,16	3.0	4.0		mA(peak)	
AGC range			68.0		dB	
Output and stretch output pull-up resistance (internal)	9,11		55.0		kΩ	At 25° C
Stretch output pulse width (T_p)	11		2.4		ms	Capacitance Pin 9 to Pin 10 = 10nF; $T_p \simeq$ -Rx C ln $\left\{\frac{1.5}{V_{CC}}\right\}$,
T co-efficient on Rx			0.7		%/° C	Where Rx = 200kΩ ± 25 % (internal resistance)
Output low	9			Output ground +0.35	V	0.2mA Sink, max.
Output high	9	Output V_{CC} -0.5			V	5μA Source
Stretch output low	11			Output ground +0.5	V	1.6mA Sink, max.
Stretch output high	11	Output V_{CC} -0.1			V	Output open circuit 5μA Source
Supply rejection, input V_{CC}	4		1.5		V(peak)	Ripple amplitude at 100Hz, Pin 12 ground
			0.8		V(peak)	Ripple amplitude at 100Hz, Pins 13 & 14 ground

NOTE
1. I_D = I_{DIODE} = IR diode forward current

APPLICATION NOTES - REFER TO FIGURE 4

Diode Anode and Cathode (Pins 1 and 16) The infra-red receiving diode is connected between pins 1 and 16. The input circuit is configured so as to reject signals common to both pins. This improves the stability of the device, and greatly reduces the sensitivity to radiated electrical noise. The diode is reverse biased by a nominal 0.65V.

Gyrator C2 and C1 (Pins 2 and 3) The decoupling, provided by gyrator C2 and C1, rolls off the gain of the feedback loop which balances the DC component of the infra-red diode current. The values of C2 and C1 are chosen to produce a low frequency cut-off characteristic below a nominal 2kHz. Hence, the gyrator produces approximately 20dB rejection at 100Hz.

The gyrator consists of two feedback loops operating in tandem. Only one feedback path is functional when the DC component of the diode current is less than 200μA. This loop is decoupled by gyrator C2. For diode currents between 200μA and 1.5mA the second control loop is operative, and this is decoupled by gyrator C1.

The decoupling capacitors, gyrator C2 and C1, must be connected between pins 2 and 3, to pin 4. The series impedance of C2 and C1 should be kept to a minimum.

First Stage Decouple (Pin 15) The capacitor on pin 15 decouples the signal from the non-inverting input of the first difference amplifier (see also Figure 2). The capacitance of 15nF is chosen to produce a 2kHz low frequency roll-off.

The capacitor must be connected between pins 15 and 14 (the input ground).

Second Stage Decouple (Pin 5) The capacitor on pin 5 decouples the signal from the non-inverting input of the second difference amplifier. The capacitance of 33nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 5 and 4 (the input V_{CC}).

Fourth Stage Decouple (Pin 6) The capacitor on pin 6 decouples the signal from the non-inverting input of the fourth difference amplifier. The capacitance of 4.7nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 6 and 7 (the output V_{CC}).

AGC Decouple/Delay Adjust (Pin 8) The output of the fourth difference amplifier is followed by a peak detector, which is used to provide an AGC control level. This produces a current source which is limited to 10mA at pin 8. The AGC decouple capacitor (C5 normally 150nF) filters the pulsed input, and the resultant level controls the gain of the first three difference amplifiers.

The AGC control level exhibits a fast attack/slow decay characteristic. Immediately infra-red pulses are detected, the gain will be reduced, so that any weaker noise pulses that are also received will not be seen at the output. Thus, provided the infra-red pulses are the most intense, it is possible to receive data in noisy environments. The slow decay keeps the AGC level intact during data reception, and produces a delay before any received noise may become present at the output, when transmission ceases.

Output (Pin 9) The output will be low, pulsing high with a source impedance of a nominal 55kΩ, for a received infra-red pulse. It is a linear amplification of the input and swings between output ground and output V_{CC}.

Stretch Input and Stretch Output (Pins 10 and 11) A typical infra-red PPM system transmits very narrow pulses. The duration of these pulses is typically 15μs, so in order to utilise a microprocessor based decoder system it is necessary to lengthen the received pulse. This stretched output can be obtained from pin 11 when a capacitor is connected between pins 9 and 10.

The width of the pulse is determined by the value of this coupling capacitor (C8 in Figure 3) and is given by:

$$T_P = -R_X C_8 \ln \left\{ \frac{1.5}{(V_4 - V_{13})} \right\}$$

where T_P = pulse width in ms
R_X = 200kΩ (see electrical characteristics)
C_8 = coupling capacitance
and $(V_4 - V_{13})$ = potential between input V_{CC} and ground (pins 13 and 14)

The stretch output is normally high pulsing low for a received infra-red pulse, and swings between output V_{CC} and output ground.

Regulator Input (Pin 12) The device can be operated with supplies of between 4.5V and 9.0V connected between input/output ground (pins 14 and 13) and input and output V_{CC} (pins 4 and 7) as shown in Figure 3.

The device can be operated with supplies in excess of 9.0V by utilising the on-chip regulator. In this case connections are made between output V_{CC} (pin 7) and the regulator input (pin 12) as shown in Figure 4. A supply voltage of between 9.0V and 18V will then cause the output ground to be regulated at a level nominally 6.4V below the output V_{CC} (pin 7).

The regulator will, however, lose control with a potential difference of less than 9.0V. Below this level the voltage on pin 13 will track nominally 1.5V above the level of pin 12.

When the regulator is not used (low voltage operation), pin 12 must be shorted to output ground (pin 13).

OPERATING NOTES - REFER TO FIGURES 3 AND 4

Gyrator C1 (Pin 3) If the environment in which the device is operating, limits the background light such that the DC component of the diode current has a maximum of 200μA, it may be desirable to omit (see Figure 3) the more bulky and costly 68μF capacitor, gyrator C1 shown in Figure 4. In this case pin 3 can be left open circuit. The resultant application will then have a characteristic of greatly reduced gain when the ambient light causes the DC current to rise above this threshold.

The 68μF capacitor can alternatively be replaced by a resistor. The outcome of this is to further reduce the gain in ambient light levels above the 200μA threshold. Below this threshold the overall gain is slightly enhanced as the light level approaches the threshold value. If chosen this resistance should lie between 10kΩ and 200kΩ.

Noise Immunity The stretch output can also be used as a means of improving performance relating to a receiver system, over and above its main purpose of providing a stretched output facility. Including C8 (Figure 4) causes the output pulses (from pin 9) to be subjected to the stretch input threshold. Thus any noise pulses from pin 9 that are below this threshold will not be seen at the stretch output (pin 11).

A further improvement can be made, utilising this stretch input threshold by including some additional filtering of the output (C10 in Figure 4). This can be adjusted in value (typically 100pF) to reduce some of the noise pulses that otherwise cross the threshold, to a level below the threshold.

It must be noted that the stretch output logic sense is inverse (for microprocessor applications) from that of the output (pin 9), and the cost of re-inversion may be deemed uneconomical for the improvements gained.

Screening Use of screening for the device, and associated components, improves the performance and immunity to externally radiated noise. The screening method used must protect the sensitive front-end of the device; provided that

the diode, pin 1, pin 16, C2 (pin 2) and the first stage decouple (pin 15) are screened, it may be found that for the application considered, the remaining circuitry need not be so protected.

In applications where externally radiated noise is minimal, it may be possible to reduce any screening to pins 1 and 16, and the diode connections, only. In some instances, no screening may be necessary, but this largely depends on the level of radiated noise, the decoupling/filtering employed and the receivers decoding technique.

Decoupling Typical decoupling arrangements for use with or without the regulator, are given in Figures 4 and 3 respectively. When using the regulator, further improvements in high frequency supply rejection are possible by the inclusion of R2. The value can be chosen so as to keep the pin 12 end of R2 within the -9.0 to -18V (w.r.t. pin 7) specified voltage range. For example if using the 920 series remote control receivers, on a supply of 16V, a typical value for R2 would be 200Ω.

Note that the regulator is a low impedance point between pins 12 and 13. C7 thus maintains a low impedance path between pins 4 and 12 at high frequencies.

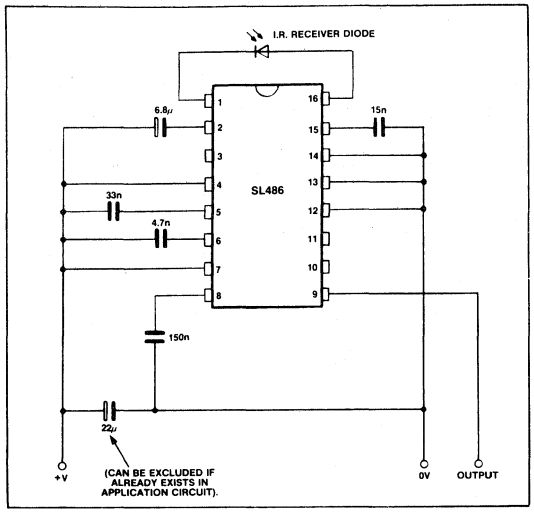


Fig.3 Circuit diagram of minimum component application (showing low voltage operation)

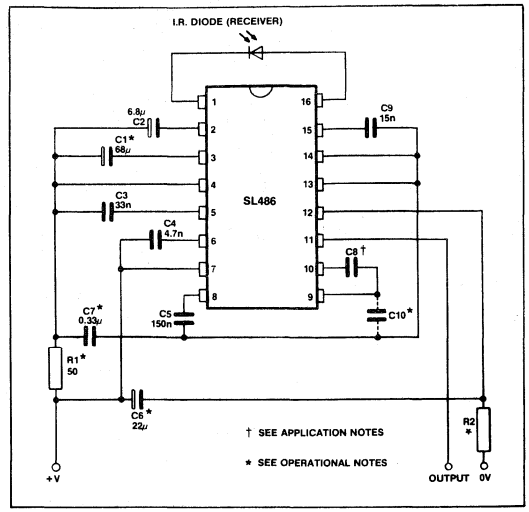
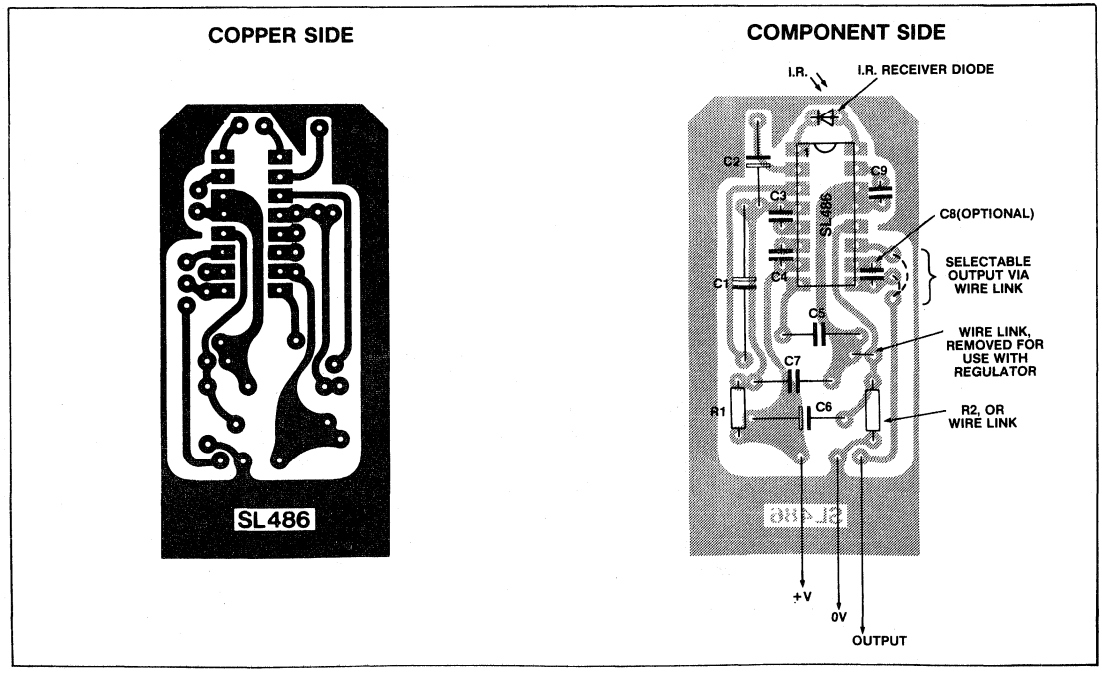


Fig.4 SL486 application diagram showing all optional circuitry (Note: Supply decoupling and connections for use of voltage regulator; also pulse stretched output)



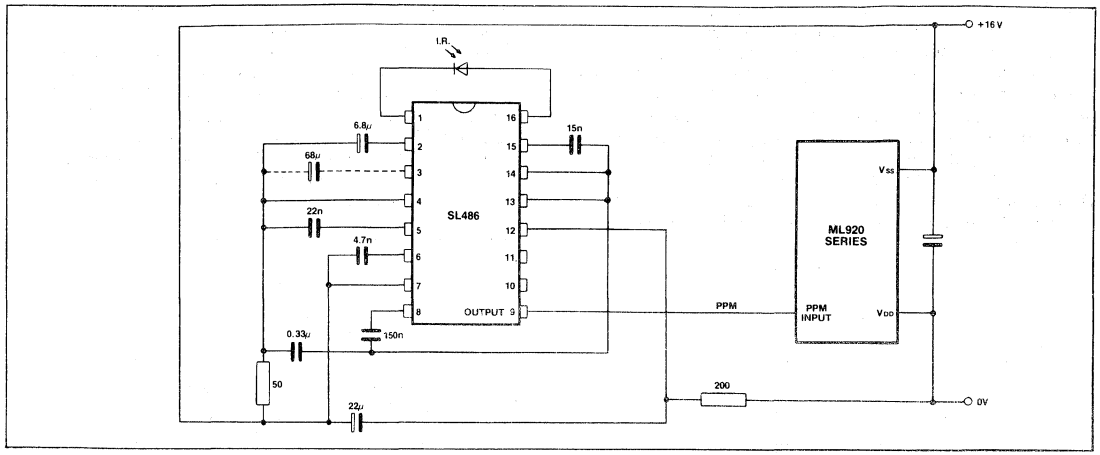


Fig.6 Application diagram for use with ML920 series remote control receivers, utilising on-chip supply stabiliser

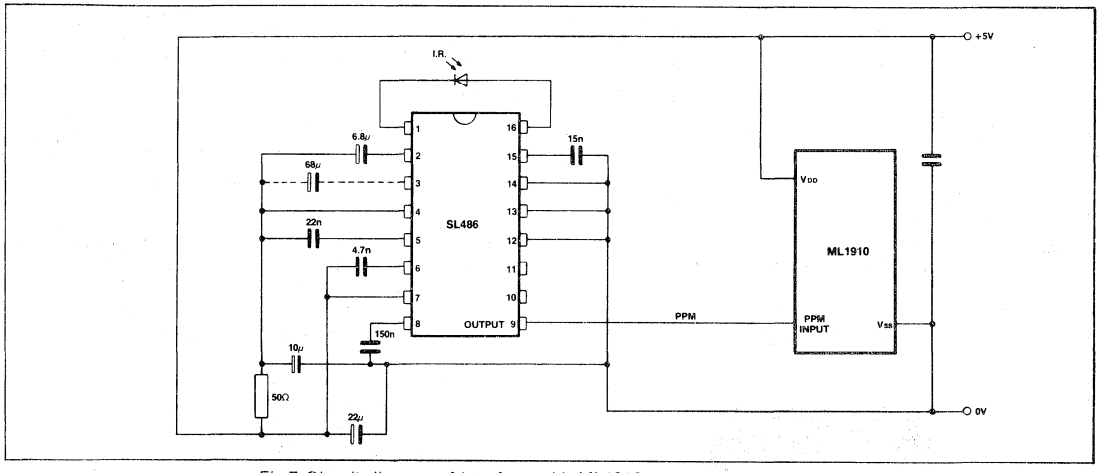


Fig.7 Circuit diagram of interface with ML1910 remote control receiver

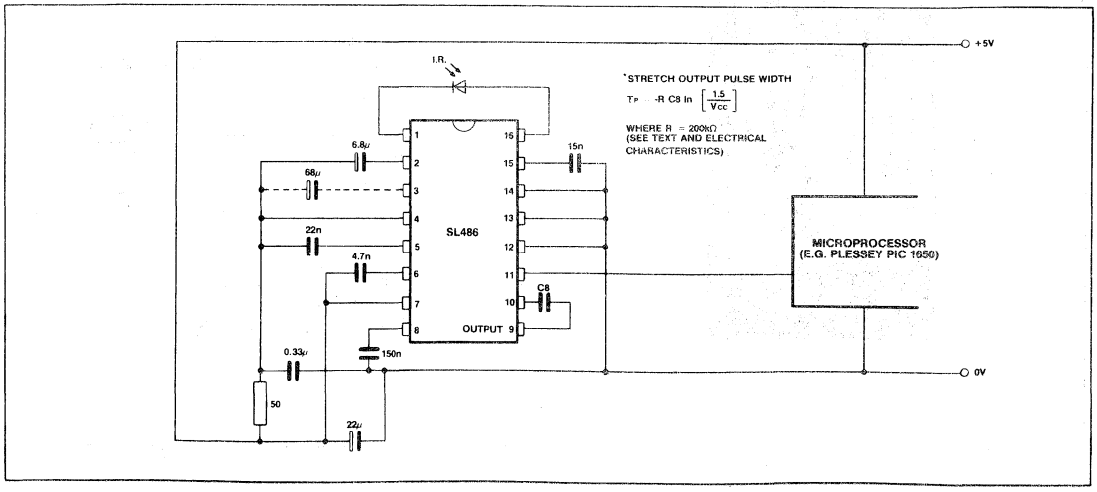


Fig.8 Circuit diagram of microprocessor interface, utilising on-chip pulse stretching facility

PLESSEY
Semiconductors

SL490B

REMOTE CONTROL TRANSMITTER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490B is an easily extendable, 32 command, pulse position modulation transmitter drawing neglible standby current. It may be used with the ML920 series of remote control receivers.

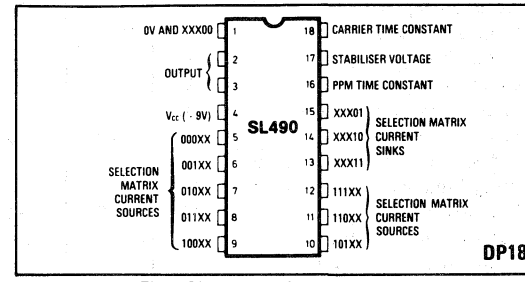


Fig.1 Pin connections - top view

FEATURES

- Ultrasonic or Infra-red Transmission
- Direct Drive for Ultrasonic Transducer
- Direct Drive of Visible LED when using Infra-red
- Very Low Power Requirements
- Pulse Position Modulation gives Excellent Immunity from Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance up to 1kohms Tolerated
- Few External Components
- Anti-bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6microamps, Operating 8mA
- Modulation: Pulse Position with or without Carrier
- Coding: 5 Bit Word giving a Primary Command Set of 32 Commands
- Key Entry: 8 x 4 Single Pole Key Matrix
- Data Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (No Carrier) to 200kHz

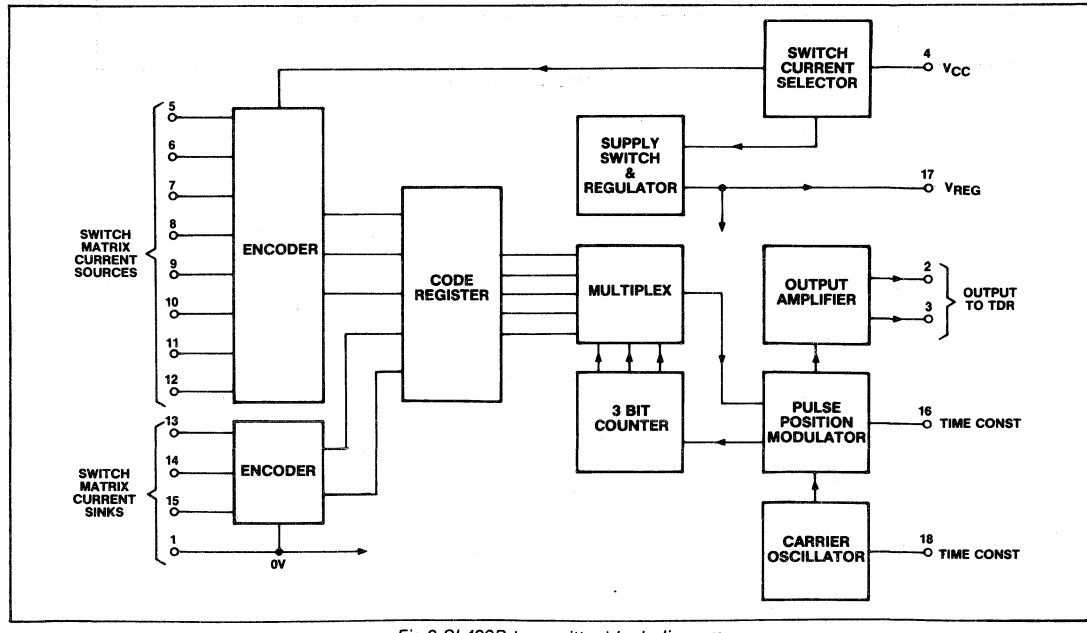


Fig.2 SL490B transmitter block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 25° C V_{CC} = +7V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		9.5	16	mA	V_{CC} = 9.5V
Standby supply current	4			10	μA	
Stabilised voltage	17	4.1		4.9	V	
Output current available from stabilised supply	17			1	mA	
Output voltage swing	2,3	V_{CC} -1			V	Unloaded
Output voltage	2			1	V	I_2 = 10mA } Peak value < 1ms
Output voltage	3			1	V	I_3 = 5mA } Peak value < 1ms
External switch resistance	5-15			5	kΩ	
External carrier resistor R2	18	20	40	80	kΩ	C2 = 680pF fc = 40kHz
t_1 deviation from calculated value	2,3			±10	%	R1 = 15k } t_1 = 0.95 C1 R1
using fixed timing components	2,3			±10	%	R1 = 60k } See Fig.4
PPM resistor	16	15	30	60	kΩ	
Variation of t_1 and t_0 with V_{CC} t_1 with V_{CC} = 7V/t_1 with V_{CC} = 10.5V	2,3			±4	%	
t_0 with V_{CC} = 7V/t_0 with V_{CC} = 10.5V	2,3			±4	%	
Ratio t_0/t_1	2,3	1.4		1.6		
Pulse width t_p	2,3	0.11 t_1		0.22 t_1		
Interword gap	2,3		3			The interword gap is 3 times t_1 derived by counting

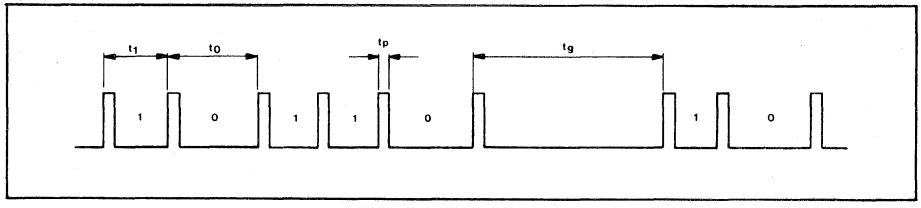


Fig.3 PPM word notation

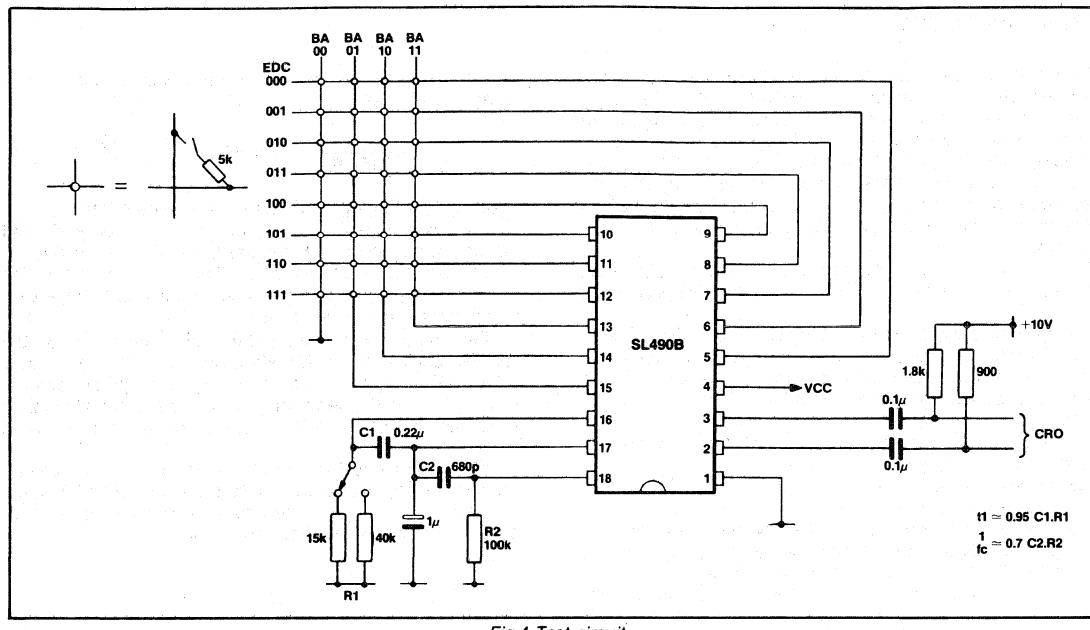


Fig.4 Test circuit

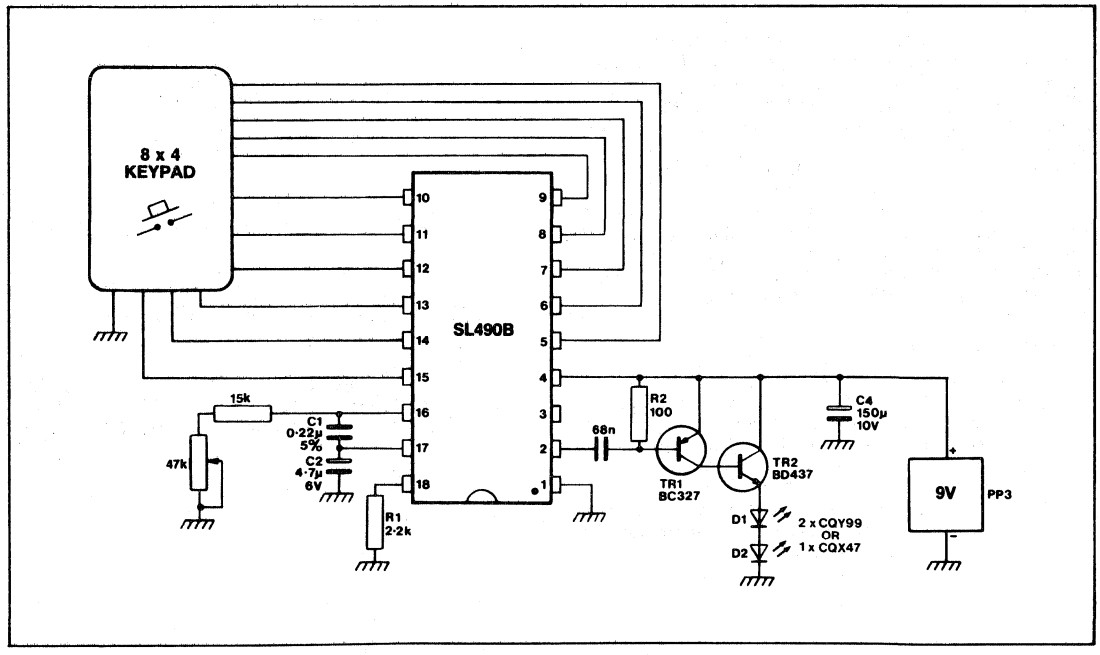


Fig.5 Infra-red application circuit

OPERATING NOTES

Fig.5 shows the circuit for a simple infra-red transmitter where the PPM output from pin 2 of the SL490B is fed to the base of the PNP transmitter TR1, producing an amplified current pulse about 15μsec wide. This pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain at high currents of the transistors.

The most common solution where cost is important is to use 2 single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but it is usually simpler to use 2 multichip diodes such as the CQX47 connected in parallel or a single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C4land with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8Amps.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

Although the ML920 series of remote control receivers is designed to work over a wide range of PPM frequencies, the actual usable range may be restricted by the application. The analogue outputs on the ML920, ML922 and ML923 serve as a good example, since the outputs will step up or down, one step for each pair of PPM words received. This in turn fixes the rate of increment or decrement of the volume or colour controls of a TV set.

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.5, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

Setting Up Procedure

When designing a remote control system using the SL490 in conjunction with the ML920 range of receiving circuits it is important from a manufacturing point of view for all transmitters to be interchangeable. The timing capacitor C1 should be chosen to give the required T1 time calculated from the formula T1 = 1.4CR with R $\simeq$ 33k. The R value should be made up of a series potentiometer resistor combination with sufficient adjustment to compensate for the I.C. and component tolerances.

The timing components on the receiver can be selected using the formula

$$f_{RX} = \frac{1}{0.15CR} \pm 20\% \text{ where } f_{RX} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

If the recommended value of potentiometer and fixed resistor, as shown in Fig.6, are used, then the value of R in the above formula should be 84kΩ. This gives the maximum frequency adjustment range, which is needed to cope with component and IC tolerances.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic 0 time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

When adjusting the ML920, the monitor output can be used for setting up, but in this case, a figure of 1/20th of the transmitter PPM logic 0 time should be used as the monitor output is at half the oscillator frequency.

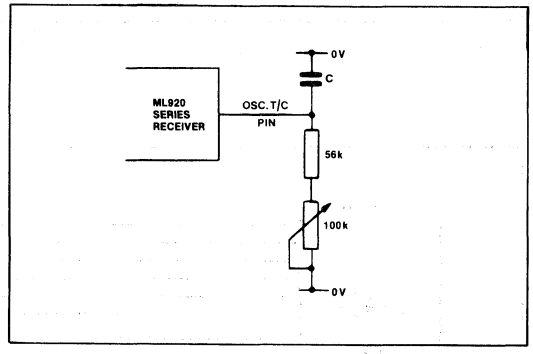


Fig.6 Recommended receiver time constant components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

PLESSEY
Semiconductors

SL 1430

TV IF PREAMPLIFIER

The SL1430 is a fixed gain IF preamplifier for television with an output optimised for driving Plessey second generation low capacitance surface acoustic wave (SAW) filters. The addition of one external capacitor allows the amplifier to drive normal capacitance SAW filters from Plessey or from other manufacturers.

The device features on chip decoupling and differerential output, requiring a minimal number of external components to be used.

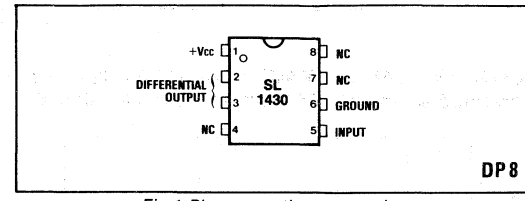


Fig.1 Pin connections - top view

FEATURES

- Low cost
- Low noise
- Low external component count
- Low distortion
- Direct 12V operation
- Can be used with different types of SAW filters

QUICK REFERENCE DATA

- 22dB gain at 40MHz
- 12V supply at 25mA
- 120mV rms. input handling

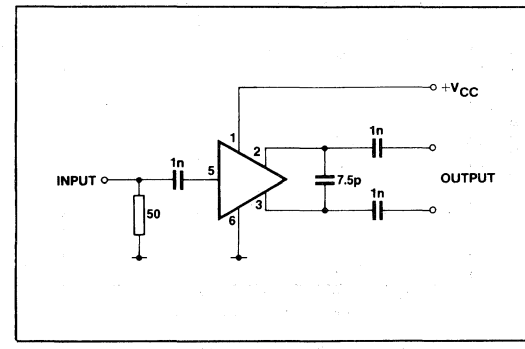


Fig. 2 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5 pF (Pins 2 and 3)
Measurements made using test circuit Fig. 2.

Characteristic	Pin	Value Min	Value Typ	Value Max	Units	Conditions
Supply voltage	1	7	12	13.5	V	
Quescent current	1	22	33	40	mA	Pins 2, 3O/C
Cut-off frequency (–3dB)	5, 2/3	60	110		MHz	
Voltage gain		18	22	26	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% crossmodulation	5		75		mV	(wanted level 20mV unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mV	rms.
Noise figure	5		4		dB	
Input impedance	5		300Ω// 4.2pF			

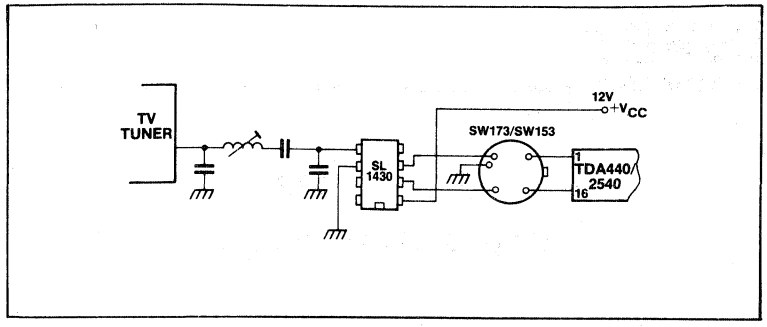


Fig. 3 Typical applications

SL1430 TYPICAL CHARACTERISTICS AT 12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS.5 TO 10)
Unwanted signal with 65% amplitude modulation at 10kHz

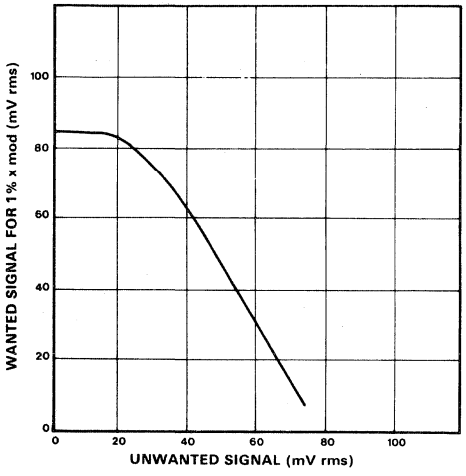


Fig. 4 Cross modulation performance (see note 1)

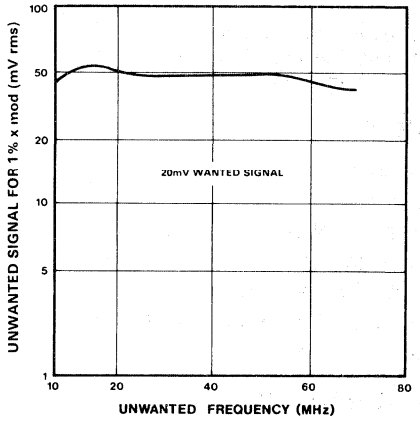


Fig. 6 Cross modulation performance V frequency of unwanted signal (see note 1)

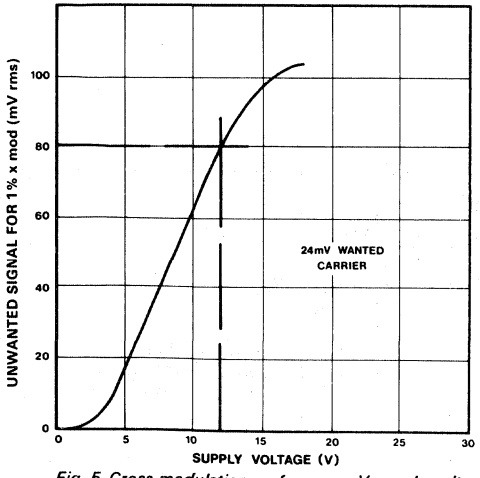


Fig. 5 Cross modulation performance V supply voltage (see note 1)

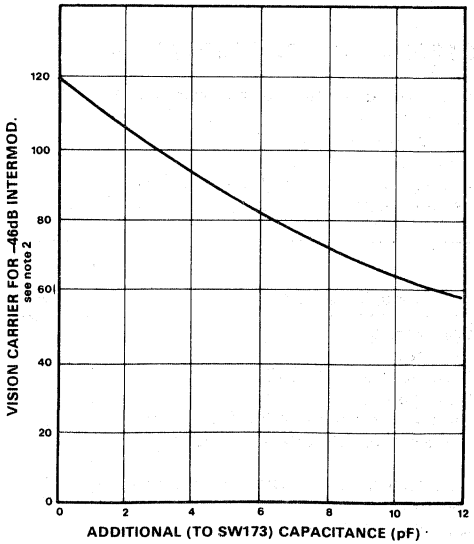


Fig. 7 Intermodulation performance v. load capacitance

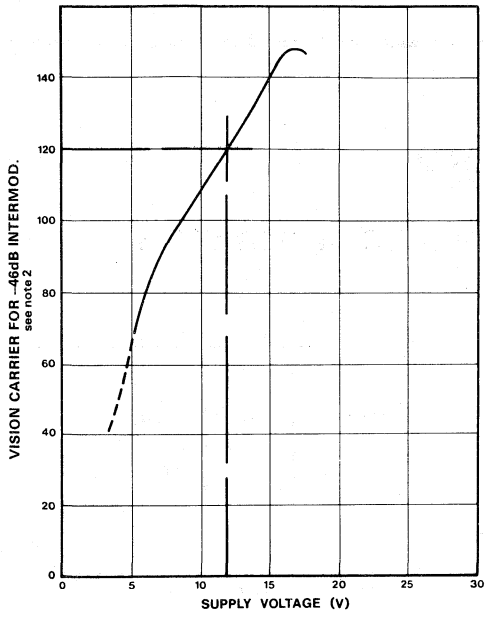


Fig. 8 Intermodulation performance v. supply voltage

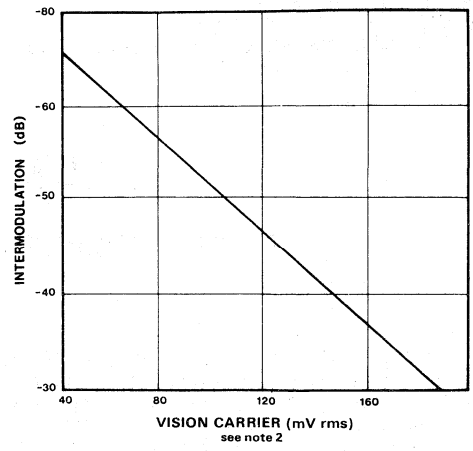


Fig. 9 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

SL1431/2

TV IF PREAMPLIFIERS WITH AGC GENERATOR

The SL1431 and SL1432 are fixed gain IF preamplifiers for television with a differential output optimised for driving Plessey surface acoustic wave (SAW) filters. Besides providing the necessary gain block between the tuner and SAW filter they also supply a properly derived, broadband AGC signal to the tuner, the SL1431 providing the correct sense signal for a NPN tuner, and the SL1432 for an PNP tuner. The tuner AGC threshold is internally preset to a value to allow adequate signal handling in the SL1431 and SL1432 and does not normally require any external adjustment. However, to account for the large variations in signal handling capability which is encountered on some tuners, the tuner AGC threshold may be externally adjusted by altering the bias on pin 1.

Both devices feature on-chip decoupling for a minimum external component count.

AGC Signal

For high input signal levels the voltage on pin 7 goes low with SL1431 and high with the SL1432.

QUICK REFERENCE DATA

- 23dB Gain at 40MHz
- 12V Supply at 25mA
- 120mV R.M.S. Input Handling
- 15mA Tuner AGC Capability

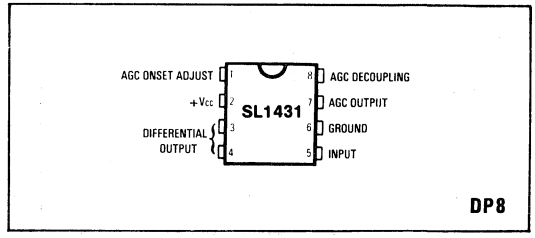


Fig.1 Pin connections - top view

FEATURES

- Properly Derived Tuner AGC
- Low Cost
- Low Noise
- Low External Component Count
- Low Distortion
- Direct 12V Operation
- Can be used with Different Types of SAW Filters

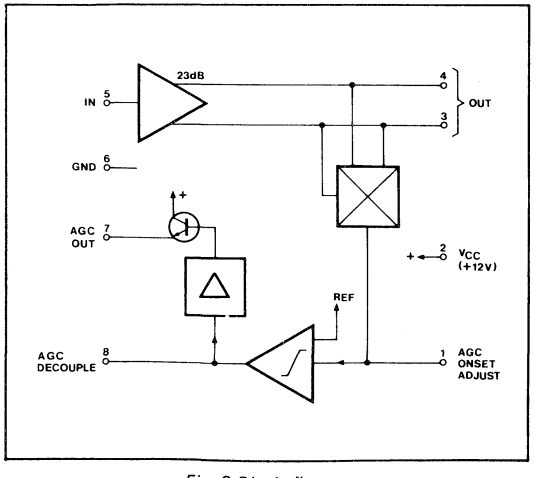


Fig. 2 Block diagram

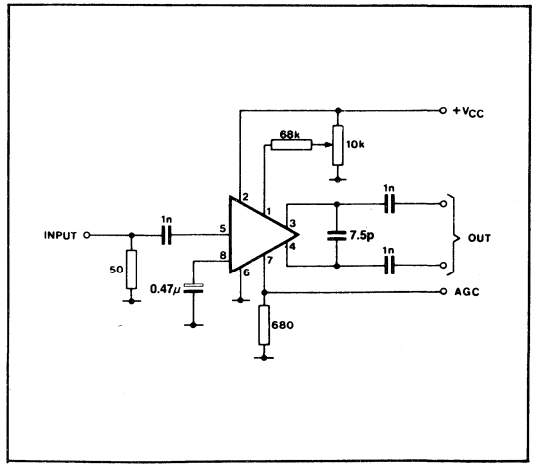


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5pF (Pins 3 and 4)
Measurements made using test circuit Fig. 3.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Voltage	2	7	12	13.5	V	
Quiescent Current	2	22	33	40	mA	Pins o/c
Cut-off frequency (—3dB)	5	60	110		MHz	
Voltage gain		20	23	26	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% cross-modulation	5		75		mV	(wanted level 20mV, unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mVrms	
Noise figure	5		4		dB	
Input impedance	5		300Ω //4.2pF			
Tuner AGC						
Output current	7	15	20		mA	@ 10.0 V
Input impedance	1		6		kΩ	

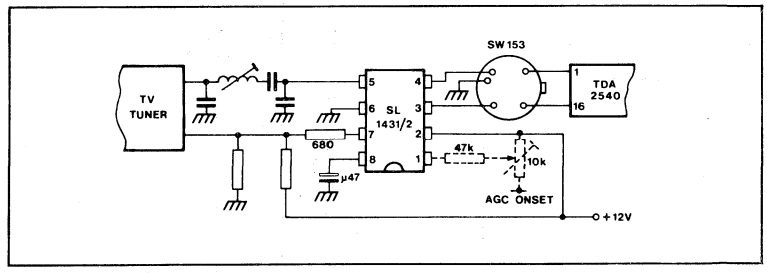


Fig. 4 Typical applications

SL1431 TYPICAL CHARACTERISTICS AT 12V, +25°C, WITH SW173 AS LOAD (7.5pF)
(FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10kHz

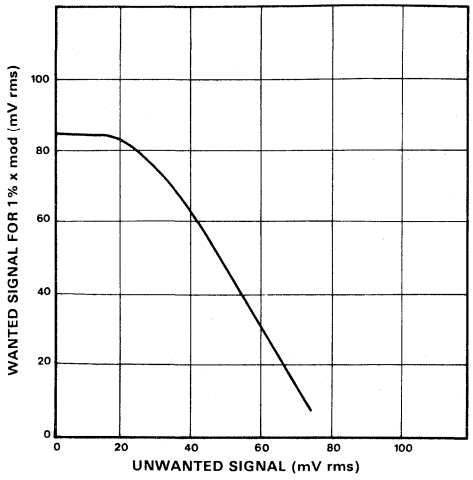


Fig. 5 Cross modulation performance (see note 1)

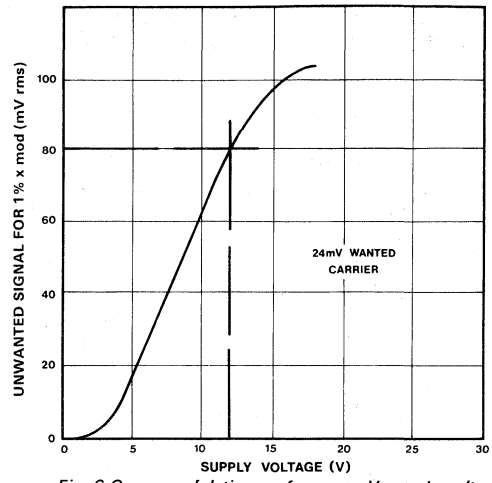


Fig. 6 Cross modulation performance V supply voltage (see note 1)

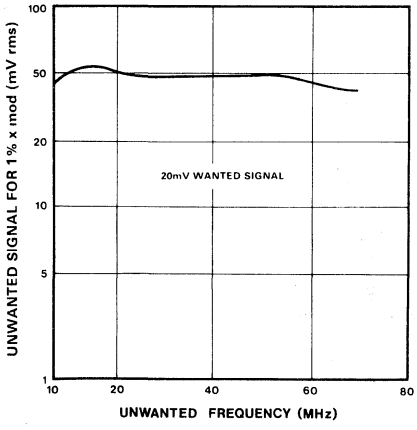


Fig. 7 Cross modulation performance V frequency of unwanted signal (see note 1)

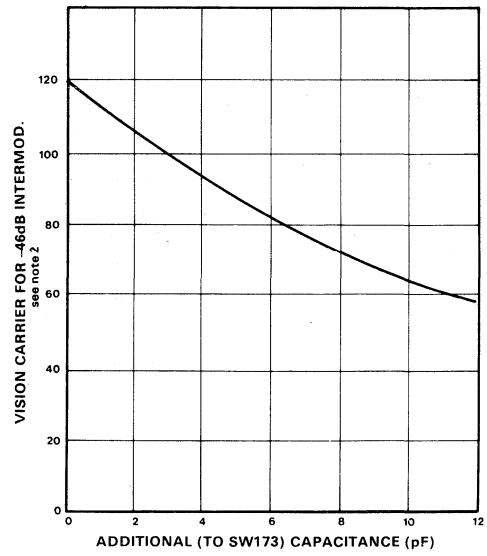


Fig. 8 Intermodulation performance v. load capacitance

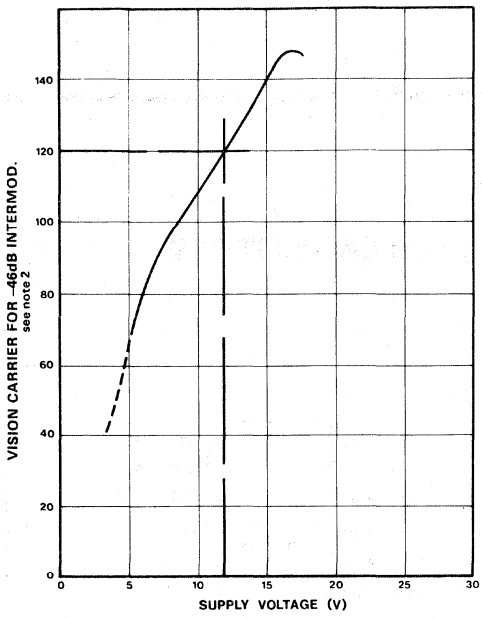


Fig. 9 Intermodulation performance v. supply voltage

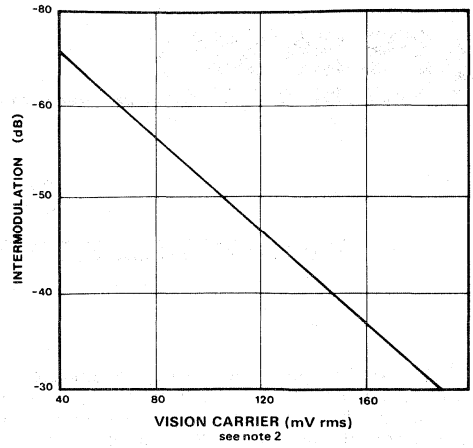


Fig. 10 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

PLESSEY
Semiconductors

SL1451

WIDEBAND PLL FM DETECTOR FOR SATELLITE TV

The SL1451 EXP is a phase locked loop demodulator for use in wideband FM systems. It is intended for use with an IF input frequency from 300MHz to 700MHz in satellite receivers. It consists of an input RF amplifier, signal level detector, UHF phase detector, UHF oscillator and video/loop amplifier. Both positive and negative going video outputs are available.

FEATURES

- Complete PLL System for Wideband FM Demodulator
- 8dB Noise Threshold Performance Typical
- Low External Component Count
- Positive and Negative Going Video Output Available
- Demodulates FM Signals with up to 28MHz Pk to Pk Deviation

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulation

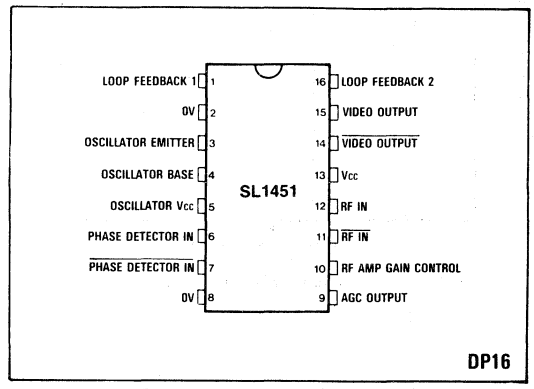


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10° C to 80° C**
Supply voltage	11V
Storage temperature range	-55° C to 125° C
Junction temperature	+175° C

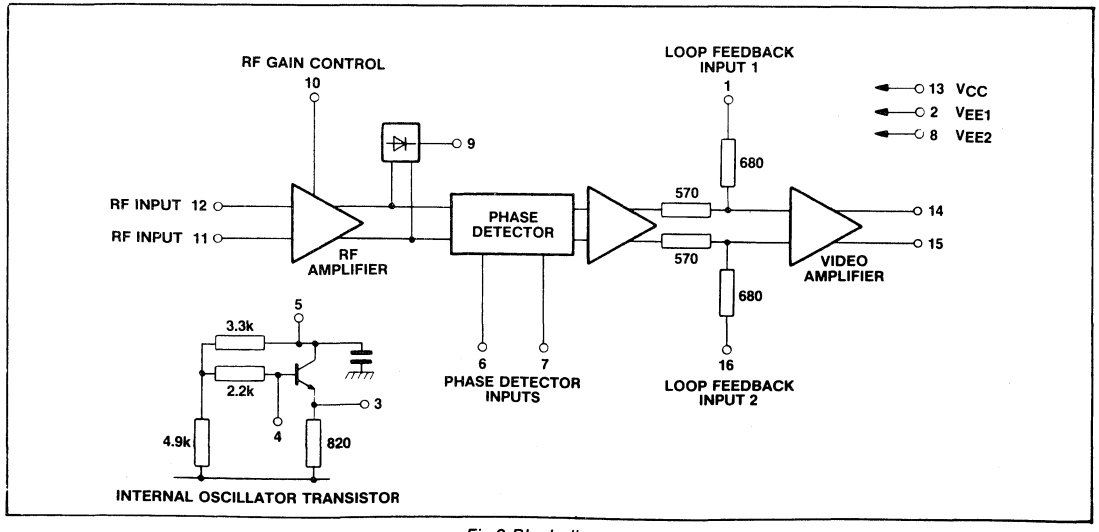


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = 7.4V to 9V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	13,5	40	55	70	mA	
Supply voltage	13,5	7.4	8.2	9	V	
Minimum oscillator frequency			300		MHz	
Maximum oscillator frequency			700		MHz	
Phase detector input level from oscillator	6,7	400	70	100	mV	
RF input level	11,12	12.5	40	125	mV	
Phase detector gain			0.5		V/Radian	
AGC output	9		300		μA	No input signal
			140		μA	-20dBm input signal
Oscillator lock range			50		MHz	See Note 1
VCO slope			14		MHz/V	
Video output voltage	14,15		1.5		Vt pk to pk	21.4MHz pk to pk deviation
Intermodulation products			-40		dBm	See Note 2
Video bandwidth			18		MHz	

NOTES
1. All characteristics from oscillator lock range to video bandwidth are determined by the application circuit. These results were gained with the circuit in Fig.3.
2. Signal 1 4.433MHz Deviation = 21.4MHz pk-pk
   Signal 2 6MHz Deviation = 3MHz pk-pk

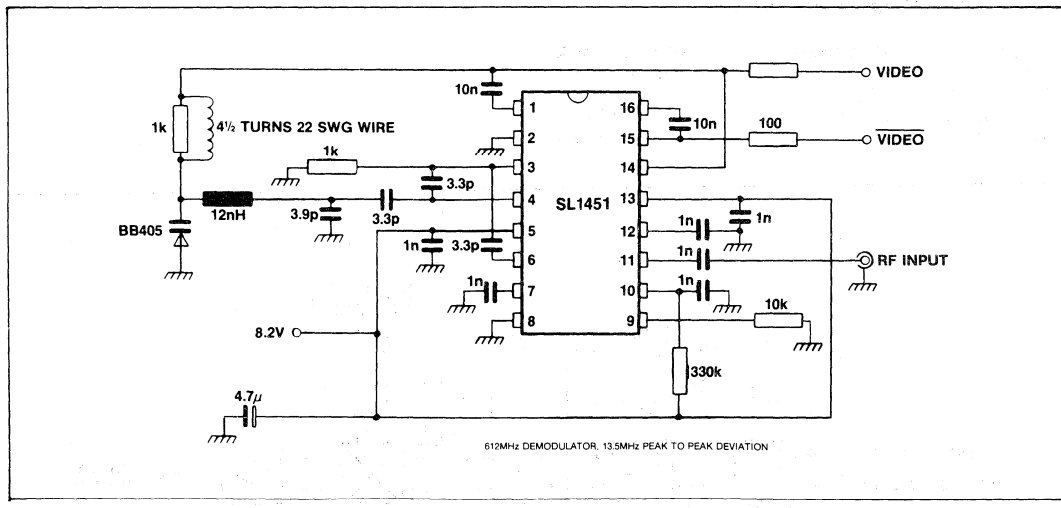


Fig.3 Typical application circuit

PLESSEY
Semiconductors

SL1452

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

With a minimum of external components, the SL1452 forms a complete wideband FM detector suitable for use in satellite TV. The video output voltage and bandwidth may be optimised by adjustment of the working Q of the quadrature coil. The device features electrostatic protection on all pins.

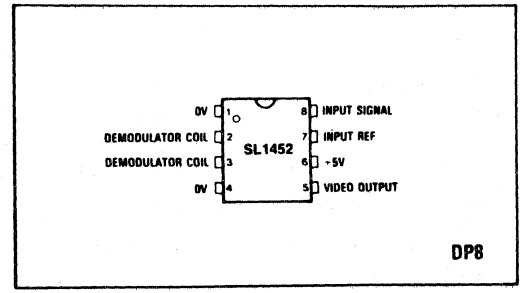


Fig.1 Pin connections - top view

FEATURES

- High Operating Frequency Simplifies Image Filtering
- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide operating frequency range 300 to 1000MHz

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +80°C**
Storage temperature	-55°C to +125°C
Supply voltage Pin 6	7V
Input voltage Pin 7 or 8	2.5V p-p
Junction temperature	+175°C

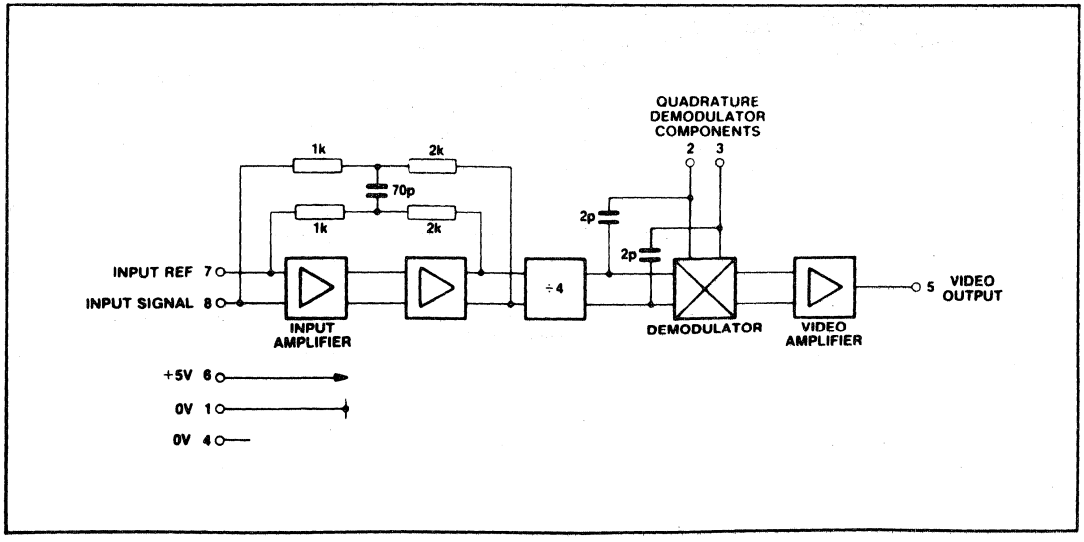


Fig.2 SL1452 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C; V_{CC} = +4.5V to +5.5V; Q = 6 f = 612MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current Ic	6		40	50	mA	Vcc = 5V
Video output voltage	5		0.7		V p-p	Δf = 13.5MHz p-p
Video bandwidth	5		14		MHz	
Minimum operating frequency	8		300		MHz	
Maximum operating frequency	8		1000		MHz	
Input sensitivity	8		5	10	mV rms	
Input overload	8	0.3	0.7		V rms	
Intermodulation	5		-60		dB	product of input modulation f = 4.4MHz Δf = 13.5MHz p-p and f = 6MHz Δf = 2MHz p-p (PAL colour and sound subcarriers)
Differential gain	5		<±1%			Δf = 13.5MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase	5		<±1		deg	demodulated colour bar waveform referred to waveform before modulation
Signal to noise ratio	5	70			dB	ratio of output with Δf = 13.5MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0

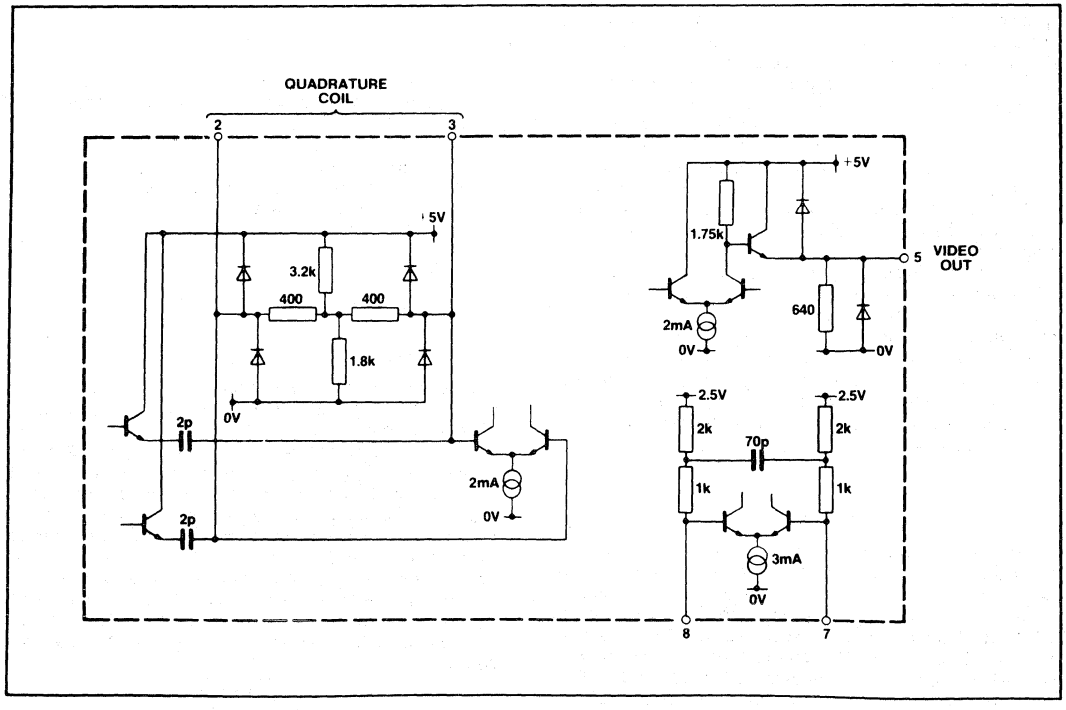


Fig.3 Input/output interface circuits

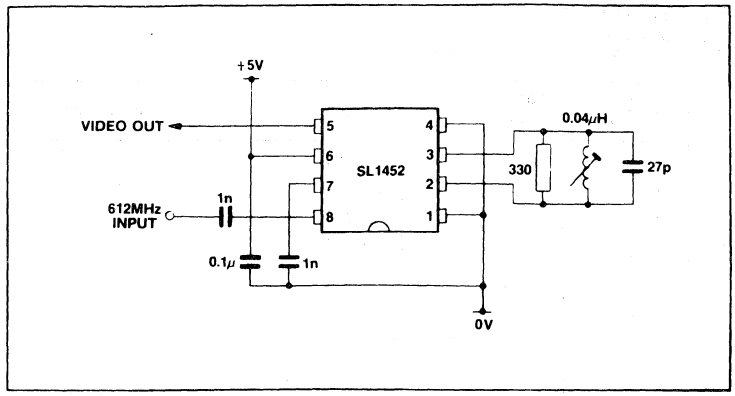


Fig.4 Typical application

SL1452 QUADRATURE DEMODULATOR

The SL1452 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies: multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency, which is a quarter of the input frequency on pin 8 due to the two internal divide by 2 circuits (see Fig.2).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{(LC)}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restrict the video output available. In general for operation in the 400 to 600MHz range, an inductance value between 40 and 60nH is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800 resistor between pins 2 and 3 must be allowed for when calculating R.

Example

Design a quadrature circuit to demodulate a carrier on pin 8 with centre frequency 480MHz and video bandwidth of 10MHz.

For L = 40nH and f_{quad} = 120MHz,
C = 43.98pF (nearest preferred value 47pF)
From Table 1, Q required is approximately 6
therefore total R required is:

$$R = Q2\pi fL$$

$$= 6 \times 2 \times \pi \times \frac{480}{4} \times 10^6 \times 0.04 \times 10^{-6}$$

$$= 181 \text{ ohms}$$

allowing for the internal 800 ohm resistance between pins 2 and 3 (see Fig.3), the external resistance required is 234 ohms. Choose 270 ohms.

It should be remembered that the internal 800 ohm resistance is subject to production tolerances and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270 ohms obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	BANDWIDTH
10	7.5MHz
6	14MHz
4	23MHz

Table 1

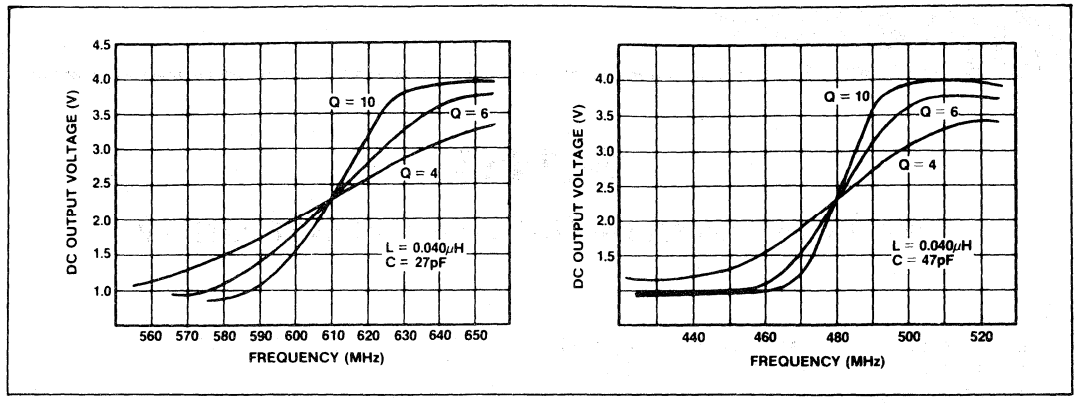


Fig.5 Output voltage versus input frequency

PLESSEY
Semiconductors

SL1454

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

The SL1454 is a wideband FM demodulator designed to operate with a carrier frequency between 70 and 150MHz. The internal circuitry of the device is similar to that of the SL1452 except that the quadrature demodulator is working at the input frequency.

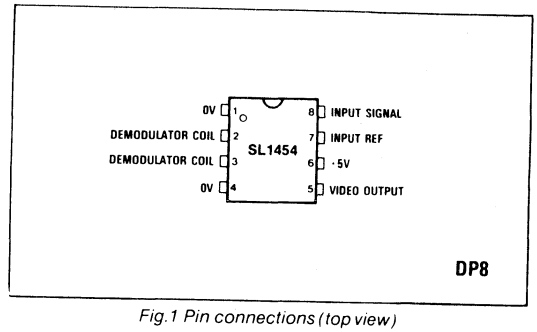


Fig.1 Pin connections (top view)

FEATURES

- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide Operating Frequency Range 70 to 150MHz

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +70°C**
Storage temperature	-55°C to +125°C
Supply voltage Pin 6	7V
Input voltage Pin 7 or 8	2.5V p-p
Junction temperature	+175°C

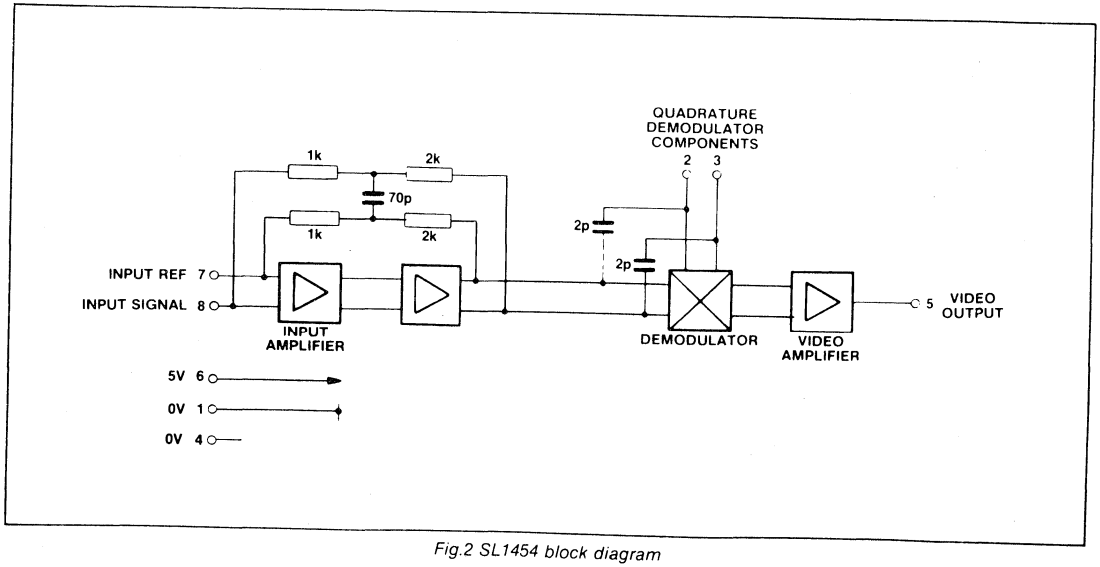


Fig.2 SL1454 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{CC} = +4.5V to +5.5V; Q = 2; f = 140MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current Ic	6		30	35	mA	V_{CC} = 5V
Video output voltage	5		0.4		V p-p	Δf = 21.4MHz p-p
Video bandwidth	5		10		MHz	
Minimum operating frequency	8		70		MHz	
Maximum operating frequency	8		150		MHz	
Input sensitivity	8		5	10	mV rms	
Input overload	8	0.7			V rms	
Intermodulation	5		-50		dB	product of input modulation f = 4.4MHz Δf = 21.4MHz p-p and f = 6MHz Δf = 3MHz p-p (PAL colour and sound subcarriers)
Differential gain	5		<±2		%	Δf = 21.4MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase	5		<±2		deg	demodulated colour bar waveform referred to waveform before modulation
Signal to noise ratio	5	70			dB	ratio of output with Δf = 21.4MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0

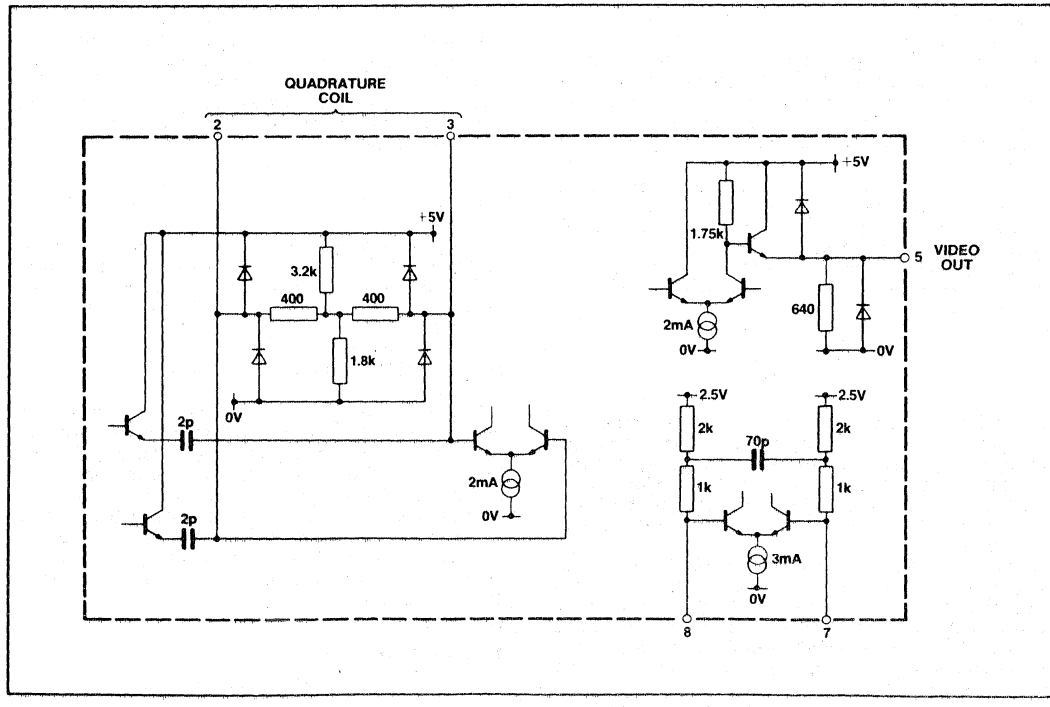


Fig.3 Input/output interface circuits

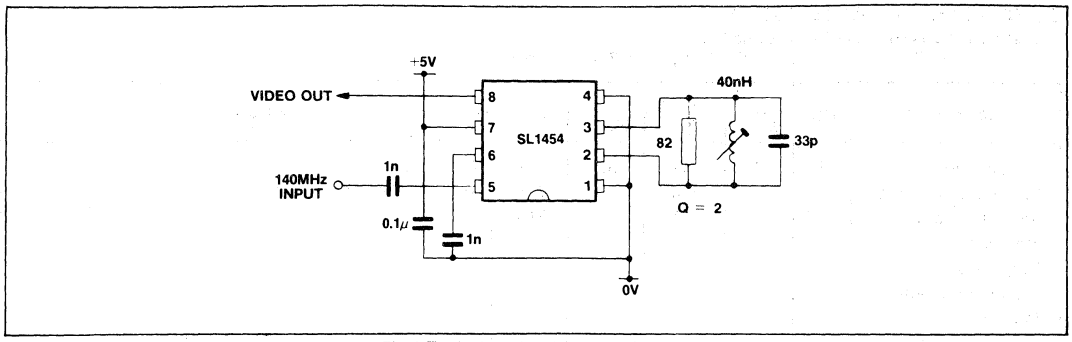


Fig.4 Typical application for 140MHz

APPLICATION NOTES

The SL1454 FM demodulator has a very simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1454, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies. A fairly stable component should be selected for the quadrature coil tuning capacitor to prevent excessive drift. The power supply decouplng capacitor from pin 6 to ground should be 0.1μF minimum, but the input coupling and decoupling values can be smaller, about 1nF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if optimum performance is to be obtained.

Choose suitable values for L and C to resonate at the intermediate frequency you are applying to the device using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation S curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive lead to the demodulator and thereby restrict the video output available.

Once suitable values for L and C have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistor between pins 2 and 3 must be taken into account when calculating R.

As can be seen from the graphs in Fig.5 for the demodulator to be demodulate a 20MHz peak to peak deviation signal with optimum linearity a very low Q value needs to be chosen (<2). But this has the disadvantage of producing a demodulator with a very low peak to peak video output level.

One way of increasing the linear region of the S curve without reducing the video output level is to incorporate a dual tuned circuit in the quadrature network. This can easily be done by capacitatively coupling another parallel tuned circuit to the normal quadrature tuned circuit.

Fig.6 shows an example of this form of dual tuned circuit, both sections have the same Q factor and the coupling capacitors are chosen to give the best linearity (Linear phase response). Fig.5(b) shows the advantages of the dual tuned circuit. The effect of varying the Q factor of the dual tuned circuit on bandwidth is also described by Table 1.

Example

Design a quadrature circuit to demodulate a 140MHz carrier with 21.4MHz peak to peak deviation, modulated with a 25Hz triangular dispersion waveform of 2MHz peak to peak deviation. The video bandwidth required is 9MHz.

Choose L = 40nH
then C = 32.309pF (nearest preferred value 33pF)

The next value to choose is the Q factor. As dispersion is employed linearity over the full 21.4MHz range needs to be optimised. The graphs in Fig.5 show that either a single tuned circuit with a Q of 2, or a dual tuned circuit with a Q of 3 is adequate. The dual tuned circuit has the advantage that the peak to peak video output is larger than that of the single tuned circuit, but extra components are required. Both circuits have a larger video bandwidth than the required 9MHz. The value of the damping resistor for the required Q is calculated below:

For Q = 2

Total $R = Q2\pi fL$

$= 2 \times 2 \times \pi \times 140 \times 10^{6} \times 0.04 \times 10^{-6}$

$= 70.3717\Omega$

allowing for the internal 800Ω resistance between pins 2 and 3 (see Fig.3), the external resistance should be 77.1Ω, choose 82Ω.

For Q = 3

Total R = $Q2\pi fL$

$= 3 \times 2 \times \pi \times 140 \times 10^{6} \times 0.04 \times 10^{-6}$

$= 105.56\Omega$

allowing for the internal 800Ω resistance, the external resistance should be 121.5Ω, choose 120Ω.

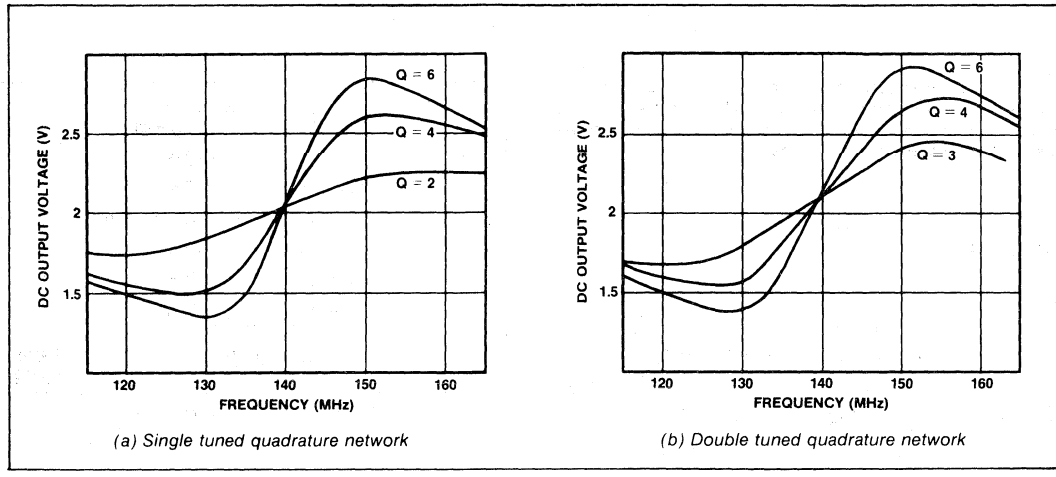
When using a dual tuned circuit the value of coupling capacitor is dependent on the Q factor. Table 2 give a guide to the values needed for best linearity.

Q	BANDWIDTH
6	10MHz
4	11MHz
2	12MHz

Table 1

Q	COUPLING CAPACITOR
6	3.9pF
4	5.6pF
3	10pF

Table 2



(a) Single tuned quadrature network

(b) Double tuned quadrature network

Fig.5 Output voltage v frequency

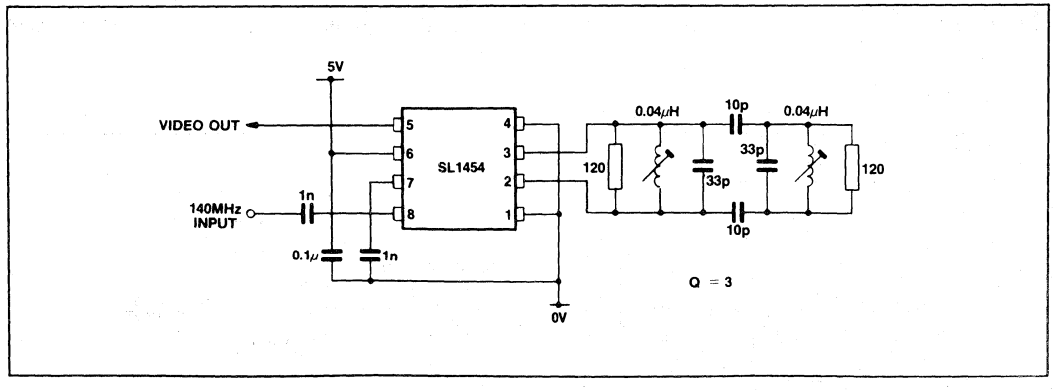


Fig.6 Example of double tuned quadrature circuit

PLESSEY
Semiconductors

SL1455

WIDEBAND FM DEMODULATOR WITH THRESHOLD EXTENSION

The SL1455 is a wideband FM demodulator with threshold extension. It is intended for use in satellite receivers with an IF between 300MHz and 700MHz. The device features electrostatic protection on all pins.

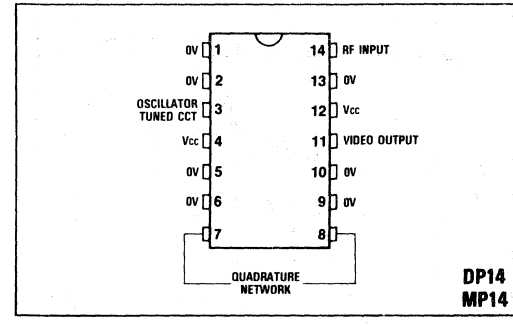


Fig.1 Pin connections (top view)

FEATURES

- 7dB Noise Threshold Obtainable
- Low External Component Count
- Negligible Differential Gain and Phase Error
- Wide Operating Frequency Range 300 to 700MHz
- Demodulates FM Signals with up to 28MHz Pk to Pk Deviation

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulator

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10° C to 80° C**
Supply voltage	7V
Storage temperature range	-55° C to 125° C

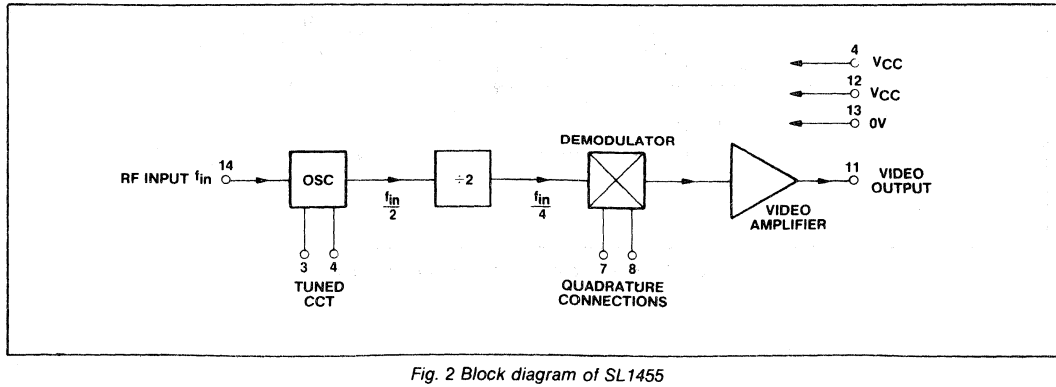


Fig. 2 Block diagram of SL1455

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C V_{CC} = 4.5V - 5.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	12,4	4.5	5	5.5	V	
Supply current	12,4	25	30	35	mA	
Differential gain			<±1		%	Δf = 21.4MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase			<±1		Deg	Demodulated colour bar waveform referred to waveform before modulation
IF range		300	610	700	MHz	
Input level	14		22	400	mV rms	
Noise threshold			7		dB	See Note 1
Output level	11		1.3		V pk to pk	21.4MHz pk to pk deviation
Intermodulation products	11		-60		dB	See Note 2
Video bandwidth			10		MHz	

NOTES
1. All parameters from Noise threshold to Video bandwidth are determined by the application circuit. These results were gained with the circuit in Fig.3.
2. Signal 1 4.433MHz : Deviation = 21.4MHz pk-pk
   Signal 2 6MHz : Deviation = 3MHz pk-pk (PAL and Sound Subcarriers)

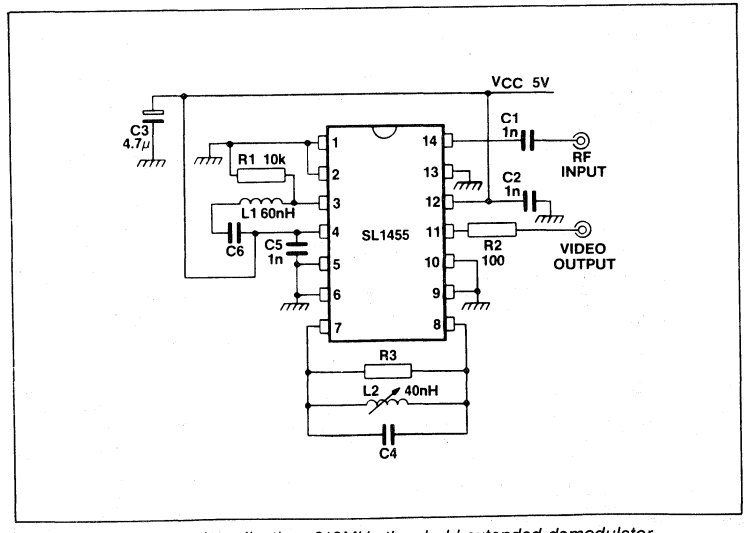


Fig.3 Typical application, 612MHz threshold extended demodulator

SL9100

VIDEOTEXT DATA SLICER AND CLOCK REGENERATOR

The SL9100 has been designed to recover data from composite video type signals, e.g. Teletext broadcasts. As well as retrieving data, the SL9100 will resynchronise a Clock output to the Data stream and also provide a composite sync output.

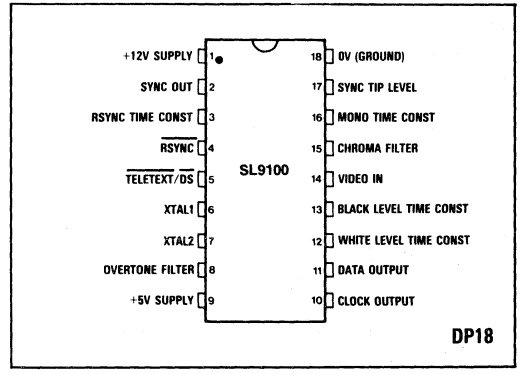


Fig.1 Pin connection - top view

FEATURES

- Slicing Of Data Adapts To Both The Black And White Video Levels
- Pre-Adaption Of The White Level Occurs At The Beginning Of Each Video Line
- Pre-Adaption Avoids Slicing Of The Colour Burst Signal
- TTL Compatible Data Output
- TTL Compatible Resynchronised Clock Output
- TTL Compatible Composite Sync Output
- Interfaces Directly To The Plessey Teleview System, Specifically The MR9710 And MR9735

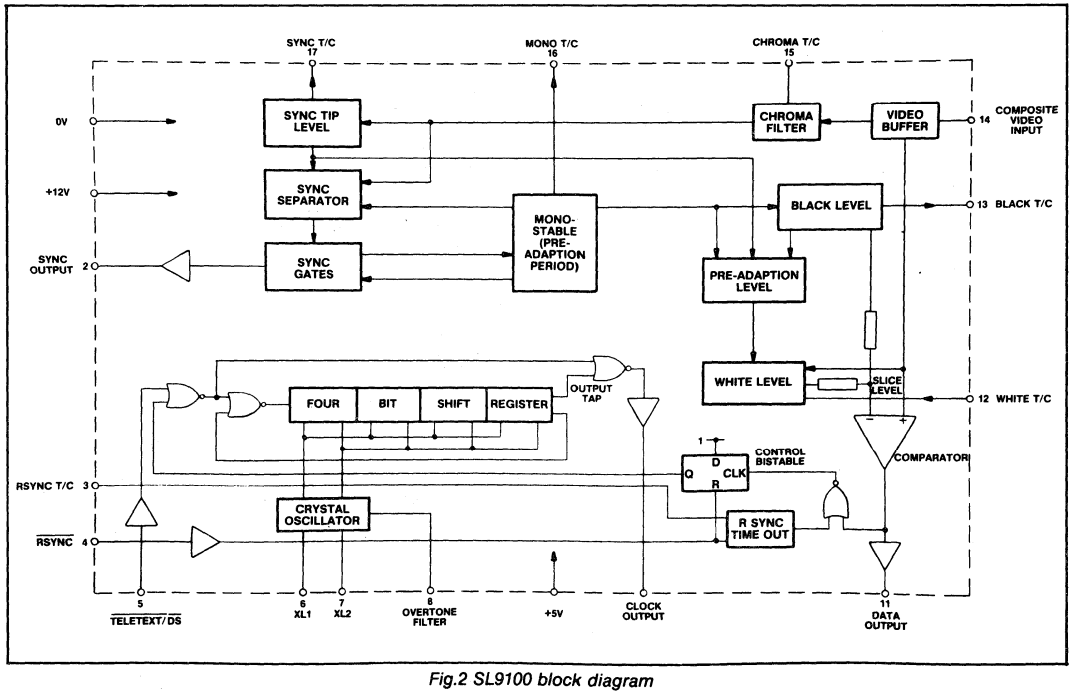


Fig.2 SL9100 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} = 25°C

Characteristic	Pin No. (Symbol)	Value			Unit	Conditions
		Min.	Typ.	Max.		
5V supply voltage	9	4.2		5.8	V	
5V supply current	9		40	45	mA	5V rail = 5V
12V supply voltage	1	10.8		13.2	V	
12V supply current	1		11	15	mA	12V rail = 12V
Video input (p-p)	14	1.5		4.5	V	AC coupled, positive video
Input impedance	14		10		kΩ	
Signal/noise ratio	14	20			dB	W.R.T. data height, during data line, with band limited white noise
Co-channel interference	14		130		mV(pk)	26.042kHz sine wave added to video
Co-channel interference	14		130		mV(pk)	52.083kHz sine wave added to video
$\overline{\text{RSYNC}}$ input pull-up	4	3.0			kΩ	Internal to +5V
$\overline{\text{RSYNC}}$ input low level	4			0.5	V	0.5mA max. source
$\overline{\text{RSYNC}}$ input high level	4	4.8			V	20μA max. source from pin
$\overline{\text{RSYNC}}$ input capacitance	4			5	pF	
$\overline{\text{Teletext/DS}}$ pull-up	5		10		kΩ	Internal to +5V
$\overline{\text{Teletext/DS}}$ input low	5			0.5	V	500μA max. source
Sync output low level	2			0.4	V	
Sync output high level	2	3.5			V	
Data output low level	11			0.4	V	Sink 1.5mA min. } Drive
Data output high level	11	3.0			V	Source 1.5mA min. } 25pF max.
Clock output low level	10			0.4	V	Sink 1.5mA min. } Drive
Clock output high level	10	3.5			V	Source 1.5mA min. } 25pF max.
Black level source	13		25		μA	
White level sink	12		25		μA	
Mono source	16		50		μA	
Sync tip level source	17		20		μA	
Pre-adaption	12	60		100	%	Over video input range
Data slice level	(11)		50		%	Over video input range
Sink slice level	(14)		150		mV	Level above sync tips at pin 14
Crystal oscillator frequency (fx)	6/7		55.5		MHz	Components as in Fig.5
Clock output frequency	10	1.5	fx/8	7.5	MHz	Free running (no video input)
Data output frequency	11	1.5		7.5	MHz	
Regenerated clock phase	10	60		90	ns	Trailing edge lag w.r.t. data output trailing edge

CIRCUIT DESCRIPTION

Video Input (Pin 14) And Chroma Time Constant (Pin 15)

The incoming video is AC-coupled into an emitter follower, biased to 6.4V through 10kΩ. This provides 'buffered video' which is then fed to an external pad through 1kΩ, where an external capacitor (C8 = 1nF) acts as a single pole filter. This filter subdues the chrominance signal, providing 'filtered video', after correcting for the voltage drop in the 1kΩ resistor.

Sync Time Constant (Pin 17) And Sync Output (Pin 2)

'Filtered video' is fed into a conventional negative peak detector using a current source into an external capacitor (C10 = 22nF). The output of this is modified in two ways:

1. With no signal present, it is clamped typically 0.2V below the quiescent video level, ensuring no SYNC output or
2. With SYNC detected the output will represent a SYNC slice level typically 0.15V above the SYNC tips (positive video).

This provides slicing of 'filtered video' which produces positive SYNC's at ECL levels for internal use. This signal is then inverted in a TTL output buffer, producing negative going composite SYNC.

Monostable Time Constant (Pin 16)

This provides the 'pre-adaption period' which has the following functions:

1. To determine when pre-adaption takes place and
2. Clamp a capacitor to the black level for subsequent reference.

The monostable is triggered on the trailing SYNC edge with a typical period of 4μs. This is set by an external capacitor (C9 = 100pF) on pin 16.

The associated SYNC gates ensure that slicing of the colour burst, or other noise immediately following SYNC, does not give rise to a false SYNC pulse or pre-adpation period. Fig.3 shows the resultant action.

Black Level Time Constant (Pin 13) And Pre-Adaption Level

The black level circuit comprises two separate peak detectors. The first tracks negative excursions of DATA in the video signal, while the positive detector resets the black level during the pre-adaption period. The positive detector is normally gated out. The negative peak detector includes a current source which charges the external black level time constant capacitor (C6 = 2.2nF) on pin 13.

During the pre-adaption period, a fixed gain amplifier is enabled to produce a 'pre-adaption level'.

A voltage proportional to the SYNC height w.r.t. black level is added to the black level and fed to the white level circuitry (i.e. estimated data size).

White Level Time Constant (Pin 12) And Data Output (Pin 11)

The white level is determined by a positive peak detector which stores either the most positive data level, or estimated data level (pre-adaption). The white level time constant is determined by an external capacitor (C5 = 2.2nF, pin 12) which is drained by an internal current sink.

The mean value of both black and white levels is chosen to be the slice level at which DATA is recovered from the video signal. This mean level is normally set at 50% of the difference of black and white levels as indicated by the two resistors shown in Fig.2. The DATA, at ECL levels, is used for Clock regeneration and also feeds a TTL buffer for output at pin 11.

Crystal Oscillator (Pins 6 And 7) And Overtone Filter (Pin 8)

The crystal oscillator uses a third overtone crystal and a parallel tuned circuit (pin 8) to ensure oscillation at 55.5MHz. It provides two anti-phase clocks for driving an on-chip four-bit shift register.

Clock Output (Pin 10) And $\overline{\text{Teletext}}/\overline{\text{DS}}$ (Pin 5)

The crystal oscillator output is divided by eight by the 4-bit shift register to provide a 7MHz (typ.) clock from incoming data. The output of the control bistable provides synchronisation of the regenerated clock to the recovered data.

When the control bistable output and $\overline{\text{Teletext}}/\overline{\text{DS}}$ pin are both low, the shift register will fill with zeros. Note that DS is grounded for Teletext operation, and that an $\overline{\text{RSYNC}}$ pulse will reset the control bistable output to zero. The output of the first NOR gate associated with the register will hold the clock output to zero until a negative transition of Data clocks the control bistable. This NOR gate output will then go low, allowing the zeros in the register to be clocked out as ones, and also fed back to the input and re-loaded as ones. This provides resynchronisation, and the output tap on the shift register is such that the negative clock edge occurs during the middle of each Data bit to provide correct clock phase w.r.t. recovered data.

Note that if the $\overline{\text{Teletext}}/\overline{\text{DS}}$ pin is held high, the clock output is a free-running division of the 55.5MHz oscillator.

$\overline{\text{RSYNC}}$ Input (Pin 4) And $\overline{\text{RSYNC}}$ Time Constant (Pin 3)

Clock resynchronisation takes place at the start of each line. An $\overline{\text{RSYNC}}$ pulse will occur at the beginning of each possible Teletext line. If data is present, the clock is re-started, checked for frequency by the Televiews system and a second $\overline{\text{RSYNC}}$ pulse occurs to provide final resynchronisation (see Timing Diagram, Fig.4). If, on a possible Teletext line, no data is present then the $\overline{\text{RSYNC}}$ time-out circuit provides re-start of the clock before the end of the line (typically 20μs after the last $\overline{\text{RSYNC}}$ pulse). This uses an external capacitor (C1 = 1nF) on pin 3, pulled up through a 20kΩ resistor, which is discharged by each $\overline{\text{RSYNC}}$ pulse.

APPLICATION NOTES

Black And White Time Constants

The black and white time constants are set by the external capacitors, C6 and C5 respectively, and the internal source and sink currents of 25μA, on pins 13 and 12. The values of C6 and C5 can be calculated once the rate at which the levels must change, in order to accommodate signal level fluctuations, has been pre-determined.

For the white level, an additional restriction must be taken into account in order to avoid false data to be sliced. This level must not fall to that of the black level, within a line period, or it will be similar to the quiescent black level, and hence the data slice level also. In order to be safe, this means that the value of C5 should not be less than 2.2nF.

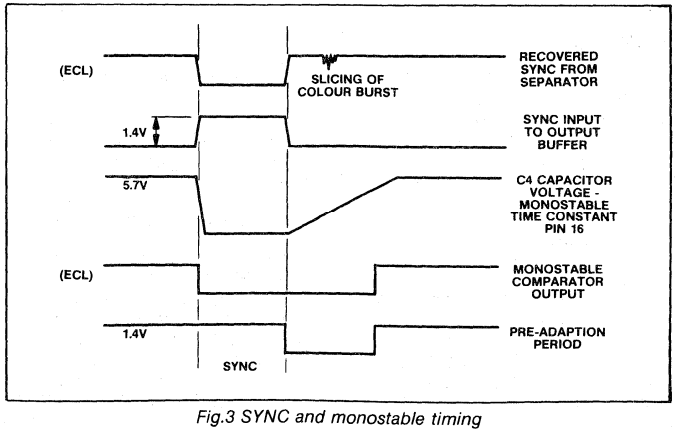


Fig.3 SYNC and monostable timing

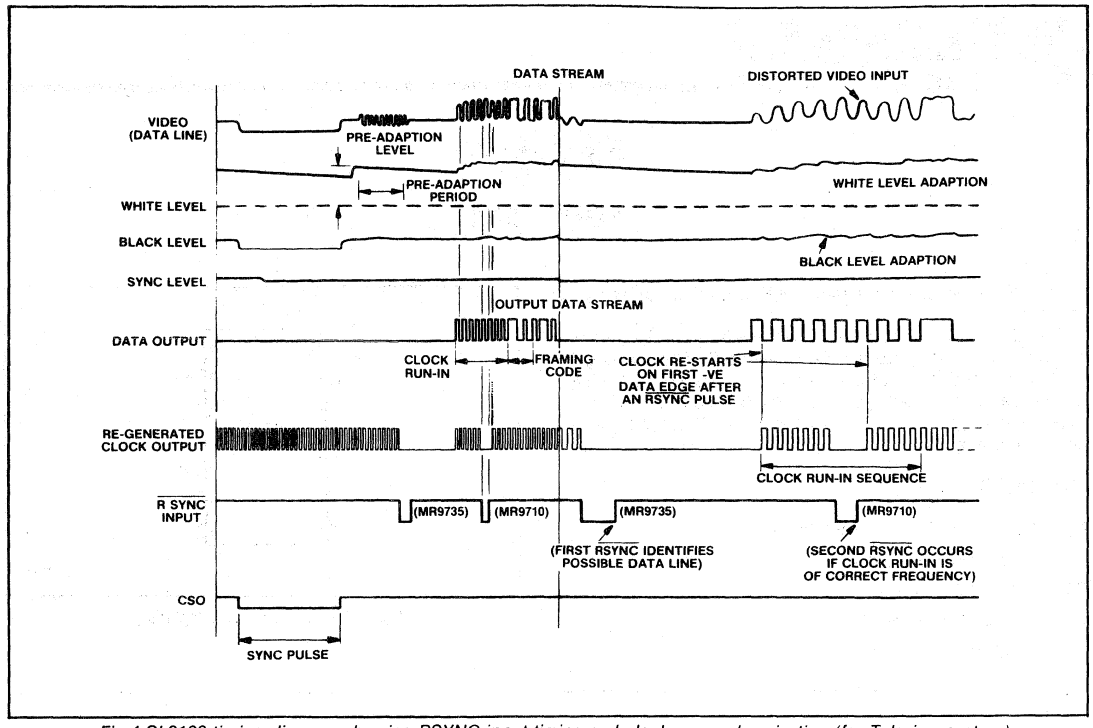


Fig.4 SL9100 timing diagram showing RSYNC input timing and clock re-synchronisation (for Teleview system)

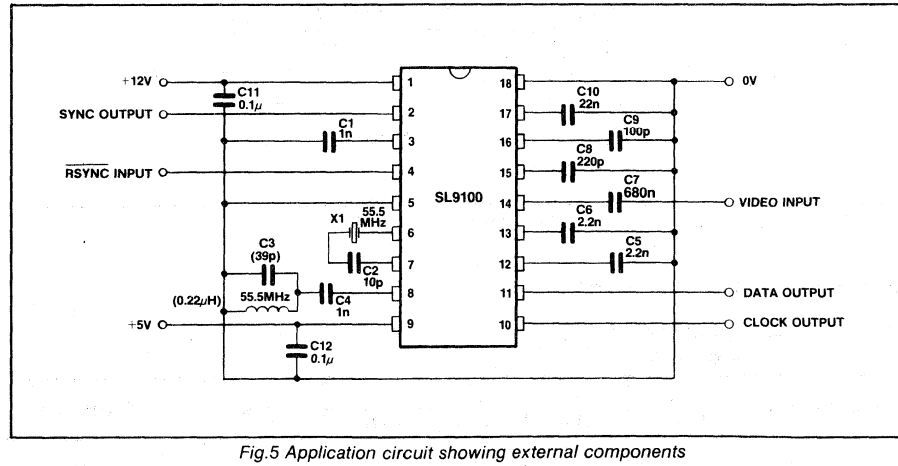


Fig.5 Application circuit showing external components

SP4541

1 GHz ÷ 256

The SP4541 is one of the range of Plessey Consumer high speed dividers.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 256 with a single TTL output and incorporates an on-chip preamplifier with a differential input. The input pins may be used as UHF and VHF, with only a slight loss of sensitivity, if suitable drive circuitry is employed.

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- TTL output

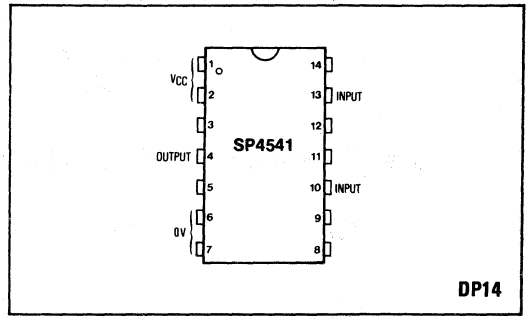


Fig.1 Pin connections - top view

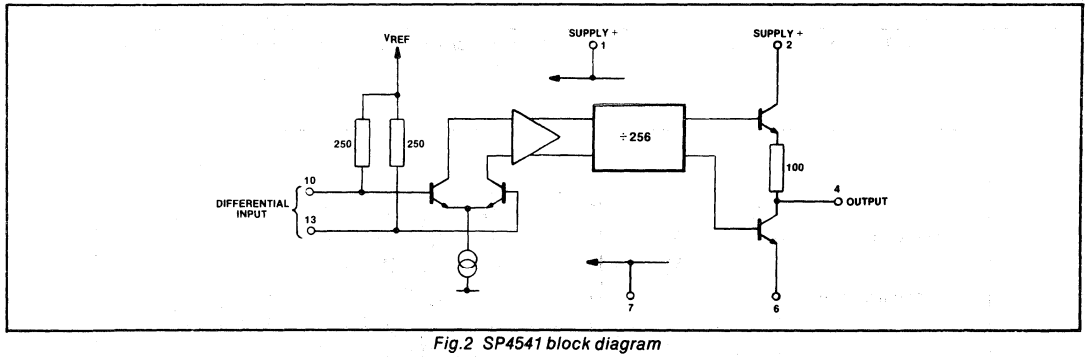


Fig.2 SP4541 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
T_{amb} = 0°C to +65°C, V_{CC} = +5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1, 2	4.5	5	5.5	V	
Supply current	1, 2		70	90	mA	
Input voltage, V_{IN}, 80MHz	10	17.5		200	mVrms	Sine wave into 50Ω
300MHz	10	17.5		200	mVrms	
500MHz	10	17.5		200	mVrms	
700MHz	10	17.5		200	mVrms	
1000MHz	10	17.5		200	mVrms	
Output voltage High		3.3			V	Sourcing 0.2mA
Low				0.4	V	Sinking 2mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

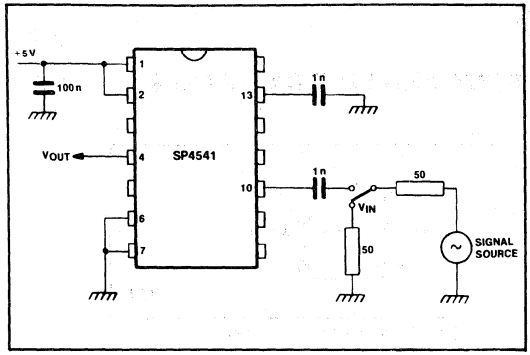


Fig.3 Test configuration

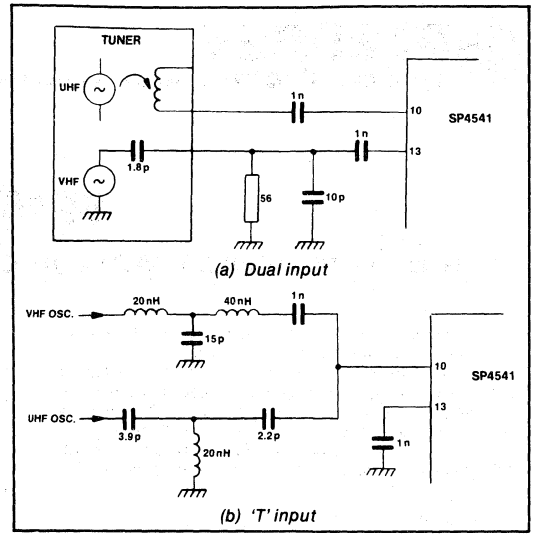


Fig.4 Combined input operation

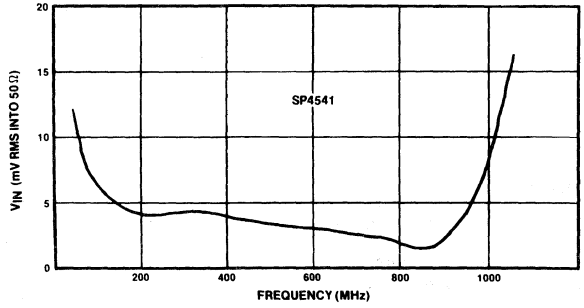


Fig.5 Typical input sensitivity

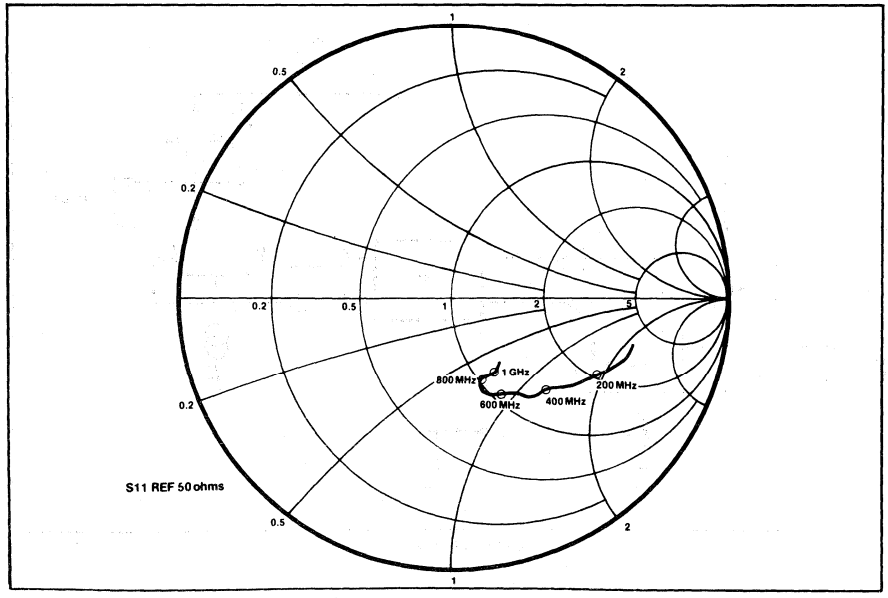


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4632

1GHz ÷ 64 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4632 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4632 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

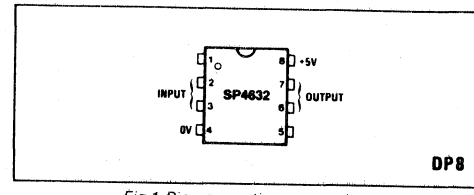


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

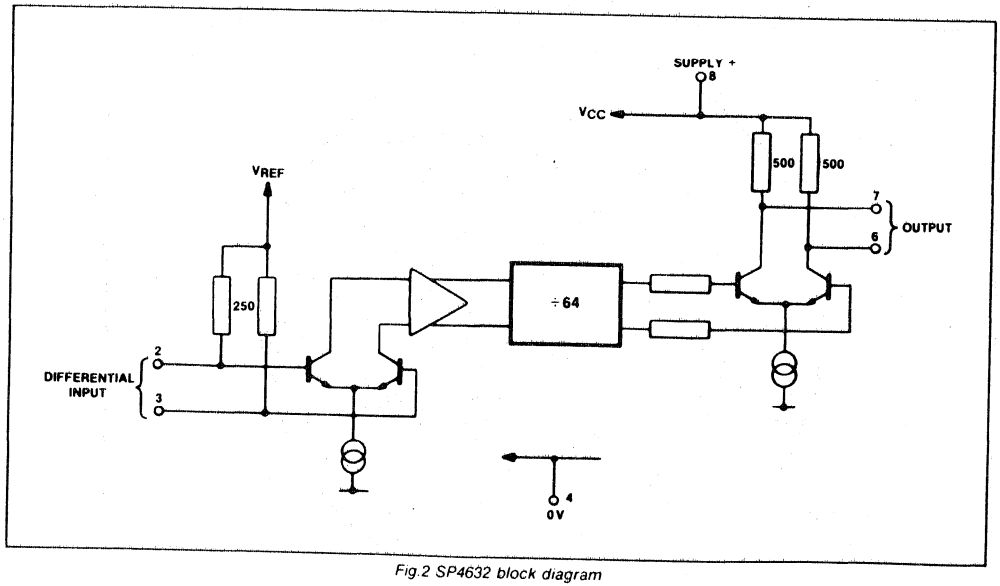


Fig.2 SP4632 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload	2,3	200			mV	80MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage with load as Fig.3	6	0.55			V	fin = 1GHz V_{CC} = 5V
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

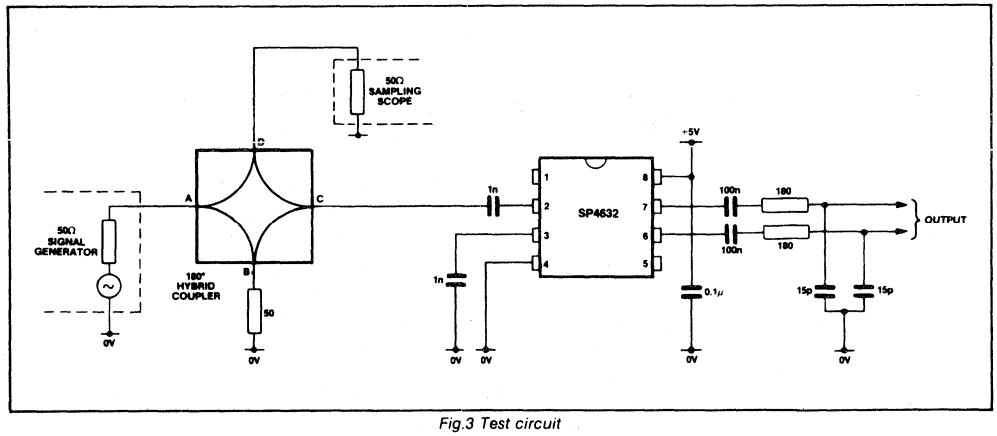


Fig.3 Test circuit

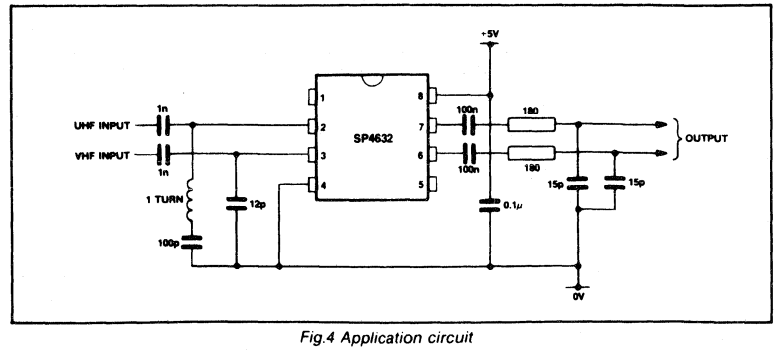


Fig.4 Application circuit

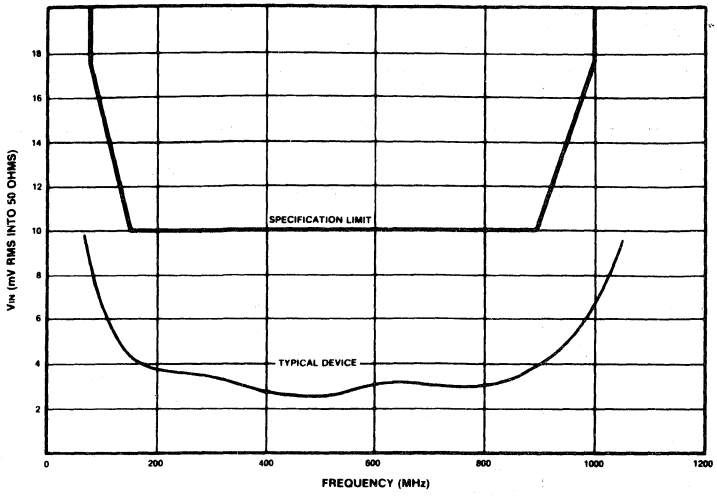


Fig.5 Typical input sensitivity

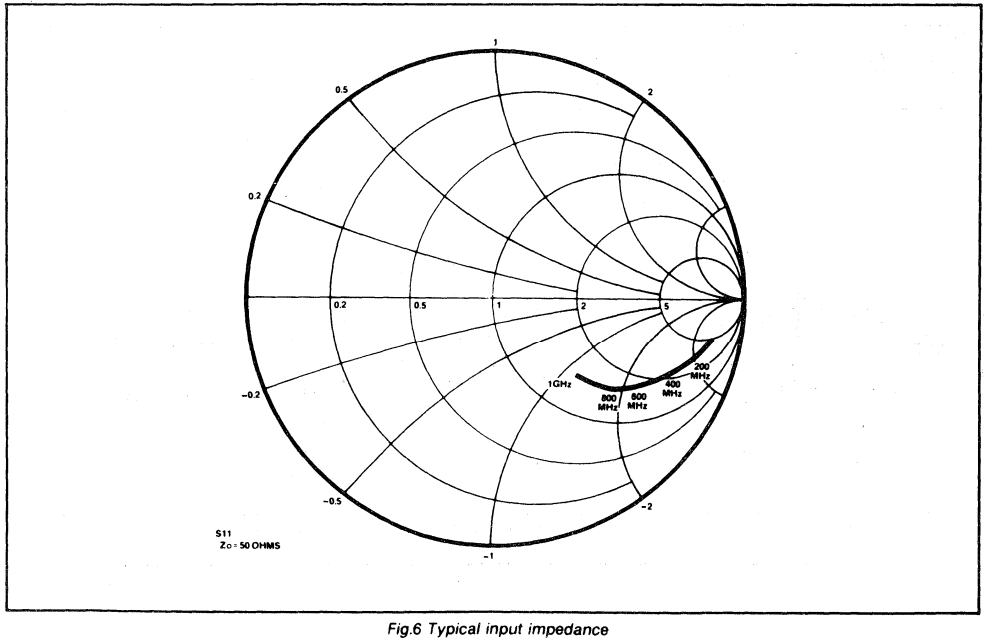


Fig.6 Typical input impedance

SP4633

1GHz ÷ 64 NON SELF OSCILLATING PRESCALER

The SP4633 ÷ 64 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4633 incorporates a two stage preamplifier which gives good low frequency sensitivity and prevents self oscillation.

Electrostatic protection is provided on all pins.

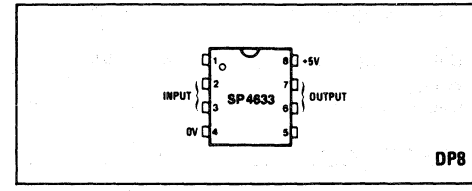


Fig.1 Pin connections - top view

FEATURES

- Does Not Self Oscillate
- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

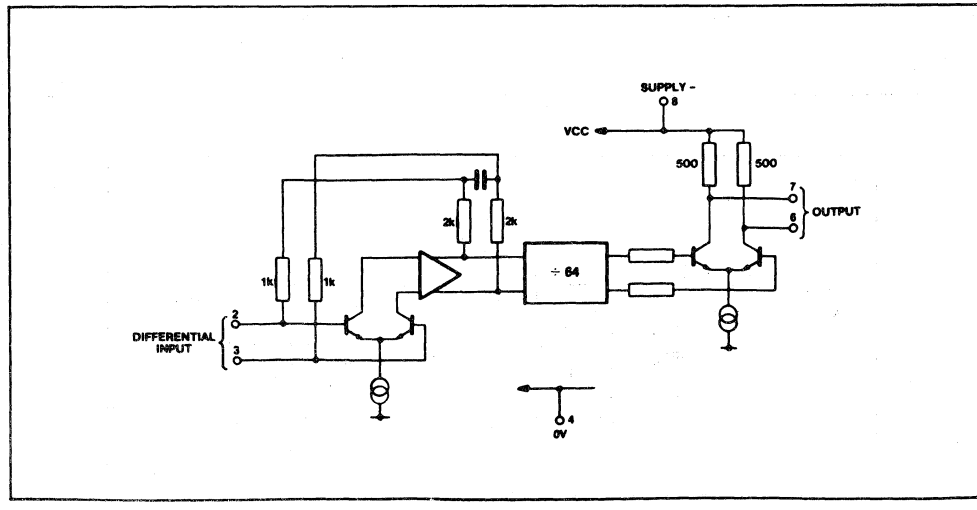


Fig.2 SP4633 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		32	45	mA	Vcc + 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz to 400MHz			1.5	5	mV	
600MHz			2	7.5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	f_{in} = 1GHz Vcc = 5V
	7	0.8			V p-p	
Output voltage with load as Fig.3	6	0.55			V	f_{in} = 1GHz Vcc = 5V
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

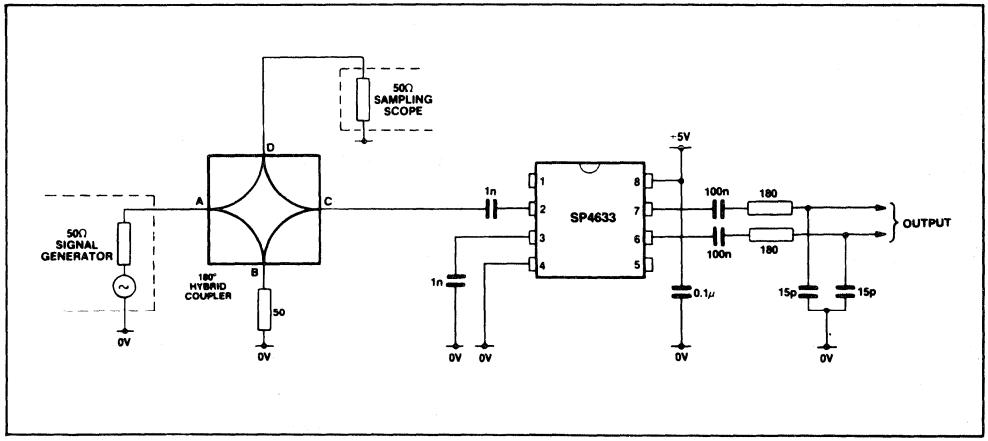


Fig.3 Test circuit

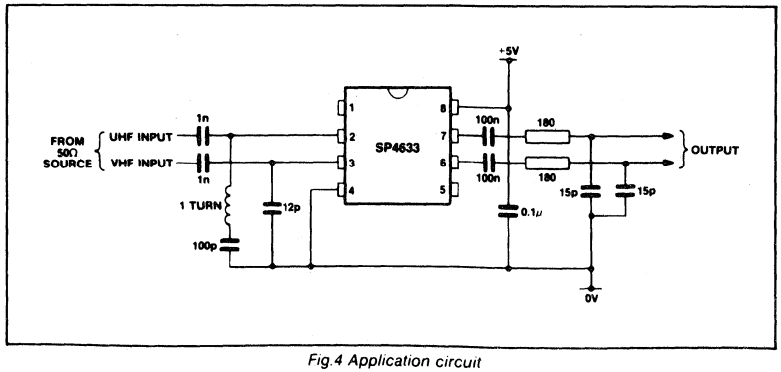


Fig.4 Application circuit

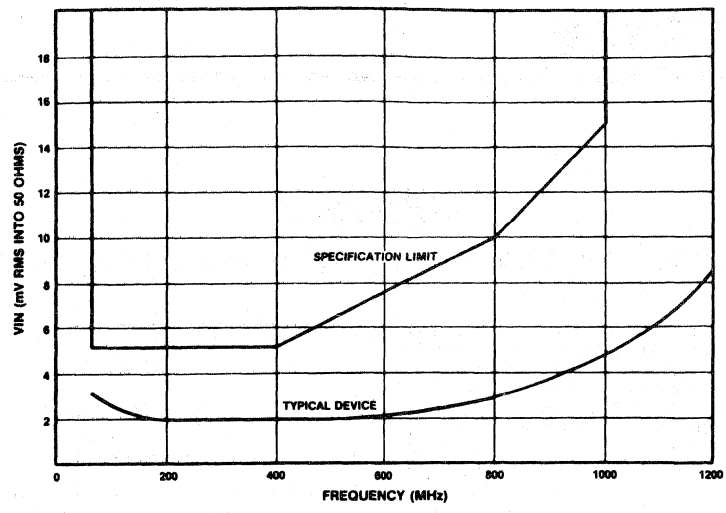


Fig.5 Typical input sensitivity

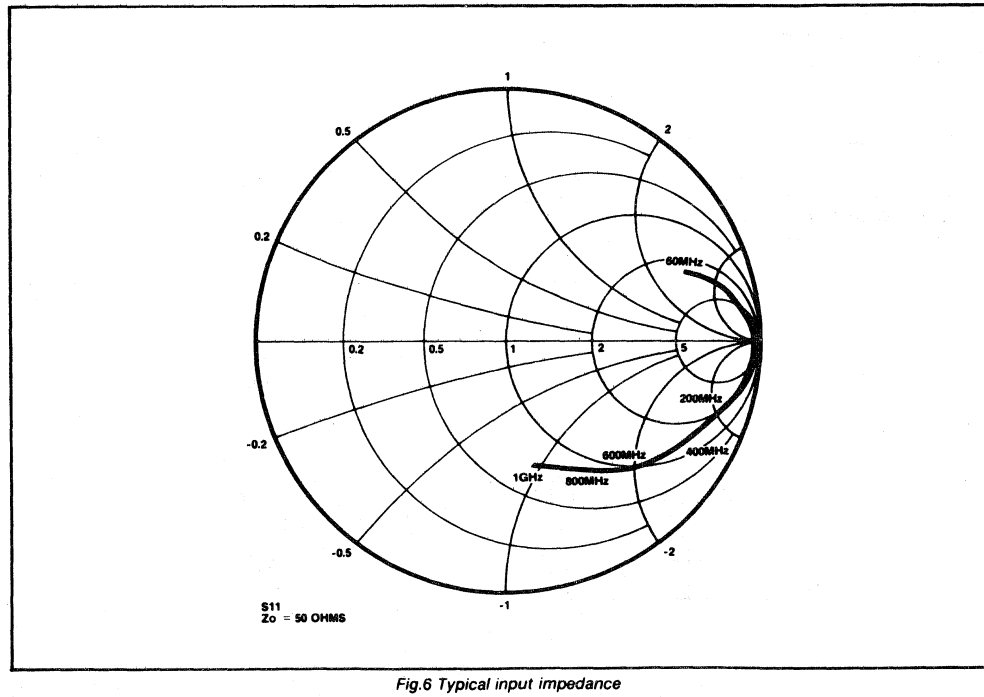


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4653

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4653 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4653 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

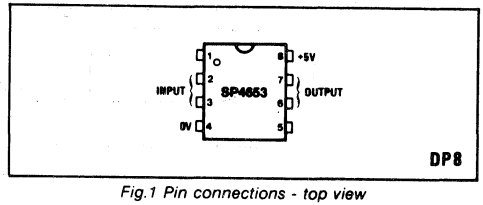


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

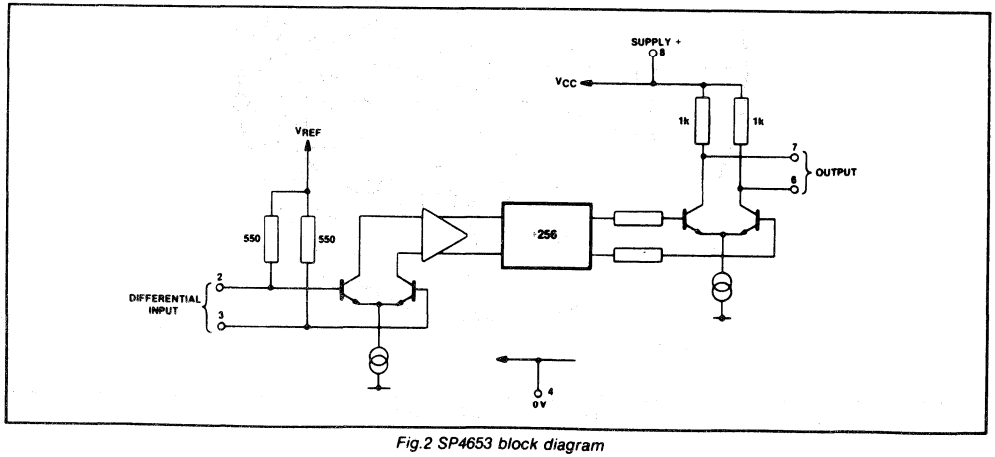


Fig.2 SP4653 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, Vcc = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	Vcc = 5V
Input sensitivity	2,3			17.5		RMS sinewave
70MHz			8	14	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	14	mV	
Input overload	2,3	200			mV	70MHz to 1050MHz operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz Vcc = 5V
	7	0.8			V p-p	
Output voltage load	6	0.6			V p-p	fin = 1GHz Vcc = 5V
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7		0.1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

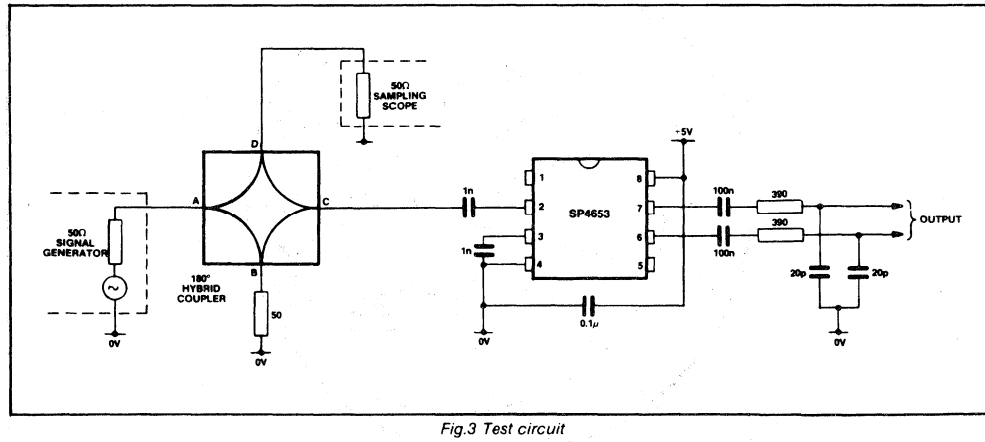


Fig.3 Test circuit

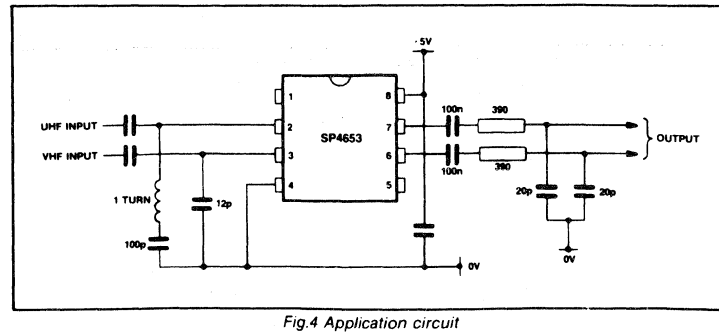


Fig.4 Application circuit

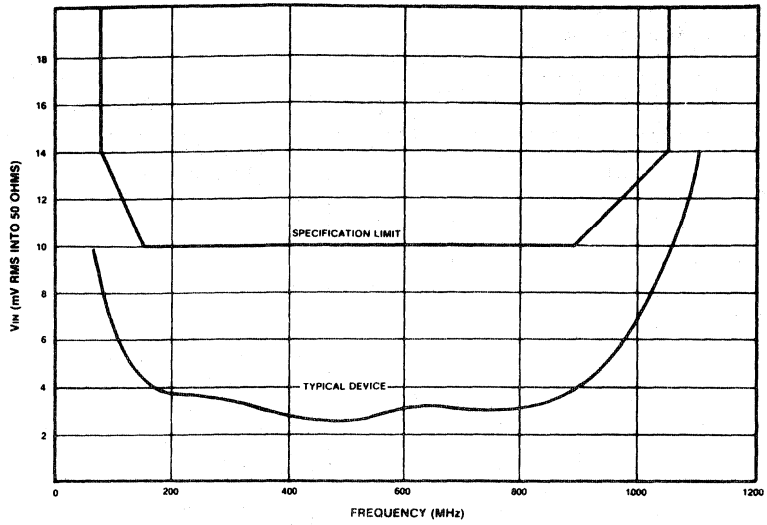


Fig.5 Typical input sensitivity

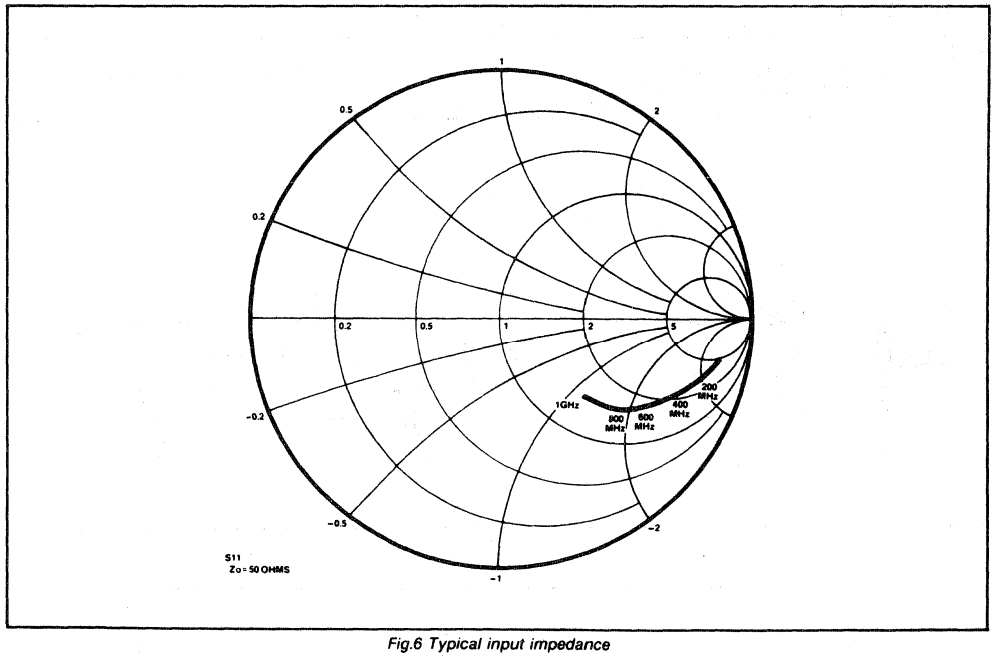


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4656

1.2GHz ÷ 128 PRESCALER

The SP4656 ÷ 128 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has low power current giving reduced power dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4656 incorporates an on chip preamplifier with differential inputs, and has balanced ECL outputs.

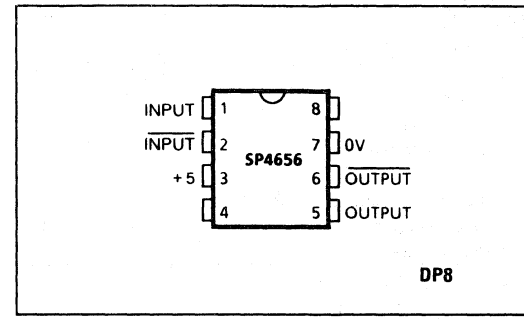


Fig.1 Pin connections-top view

FEATURES

- Low Radiation
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc	+7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to +125°C
Operating temperating range	0°C to +80°C

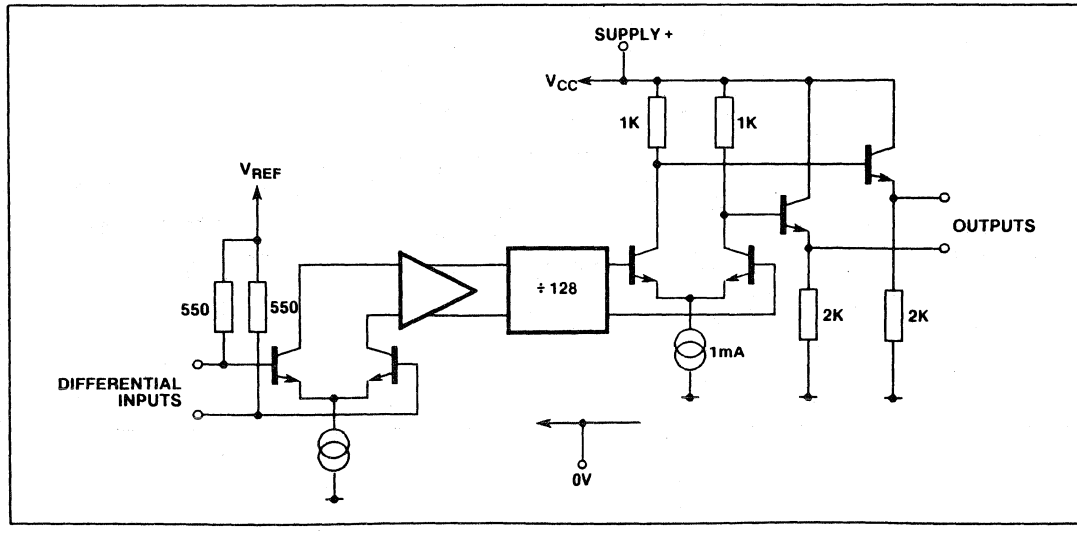


Fig.2 SP4656 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +80°C, VCC = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Max	Typ	Min		
Supply current	8		32	38	mA	V_{CC} = 5V
Input sensitivity	1,2					RMS sine wave
80MHz			8	14	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	14	mV	
1200MHz			15	35	mV	
Input overload	1,2	300			mV	
Input impedance	1,2		50		ohms	See fig. 6
			2		pF	
Output voltage load as fig.3	5,6	0.5	0.8		Vp-p	F_{OUT} = 7.8MHz, V_{CC} = 5V
Output voltage no load	5,6	0.8	1		Vp-p	F_{OUT} = 7.8MHz, V_{CC} = 5V
Output imbalance	5,6		0.1		V	

NOTE

The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device. For correct operation the input signal must be maintained between these limits at all frequencies.

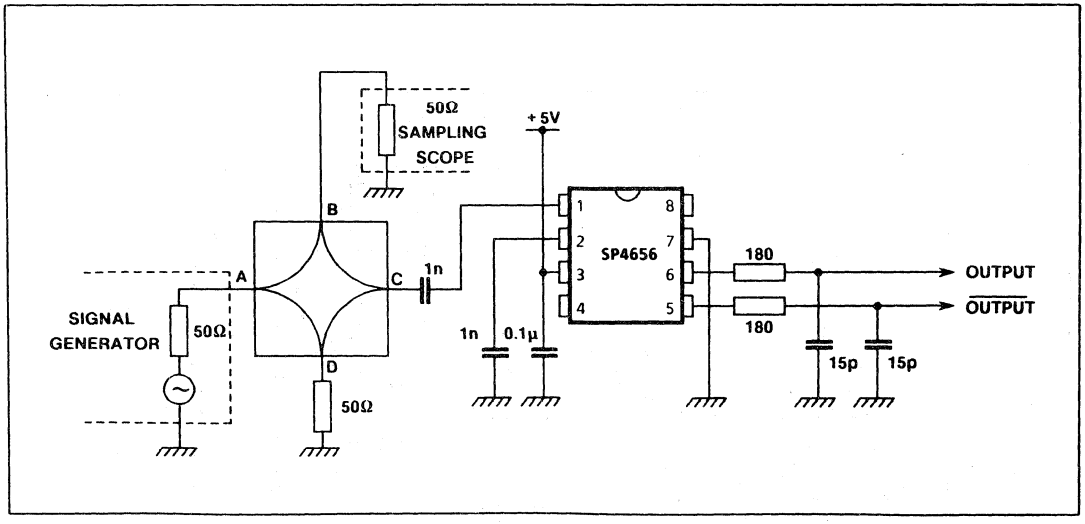


Fig.3 Test Circuit

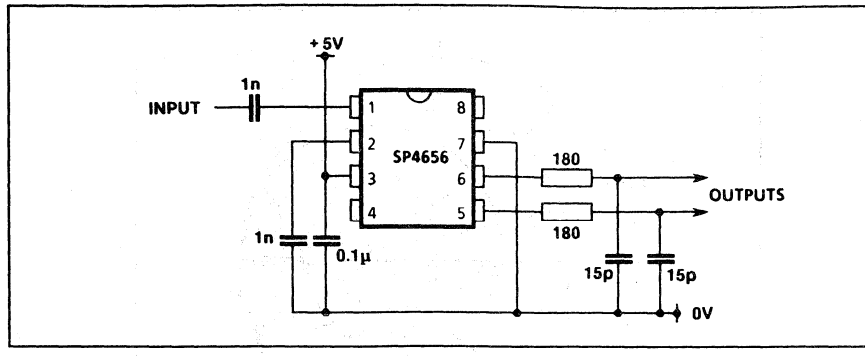


Fig.4 Application circuit

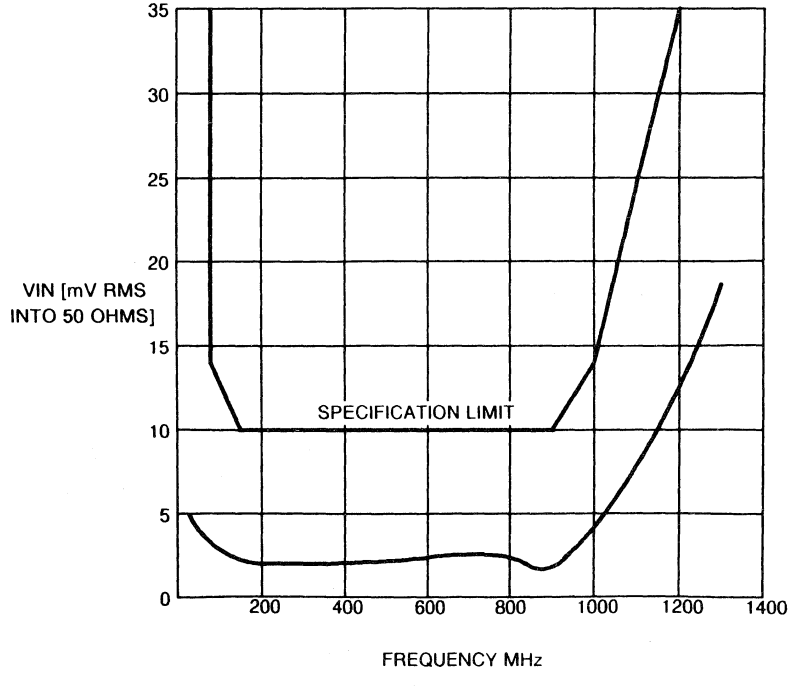


Fig.5 Input sensitivity

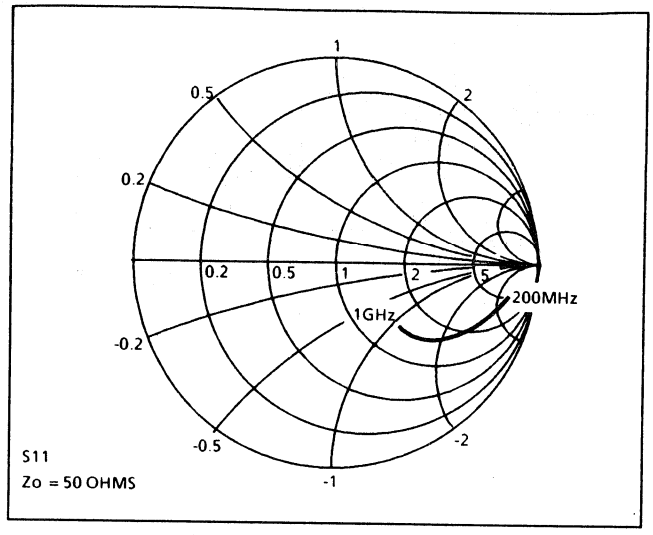


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4660

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4660 ÷ 256 prescaler is one of Plessey Semiconductors' lastest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4660 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

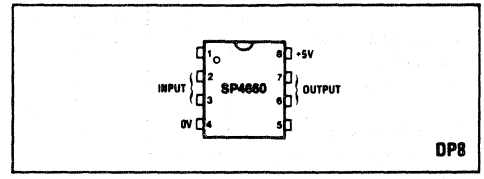


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity from 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

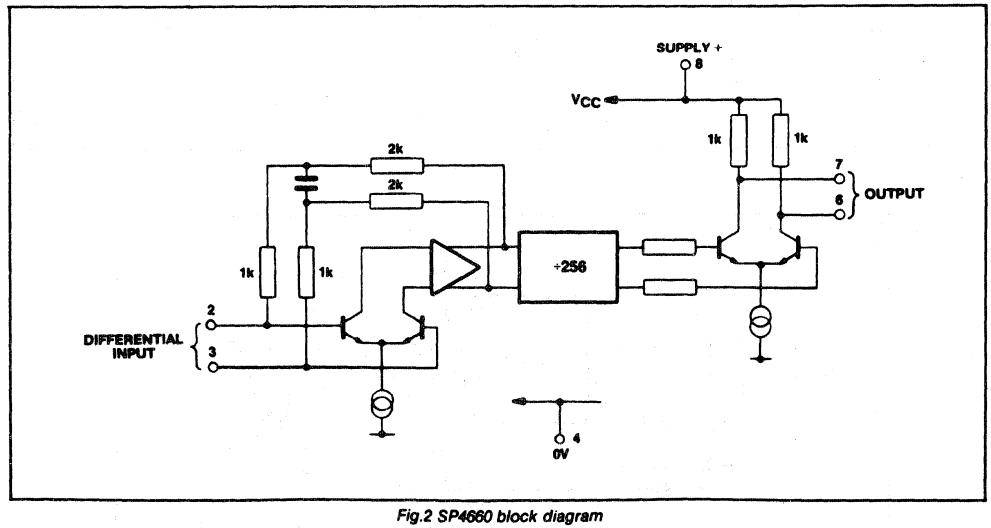


Fig.2 SP4660 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		32	45	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
Input overload	2,3					
		300			mV	50MHz to 1.0GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage load	6	0.6			V p-p	fin = 1GHz V_{CC} = 5V
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

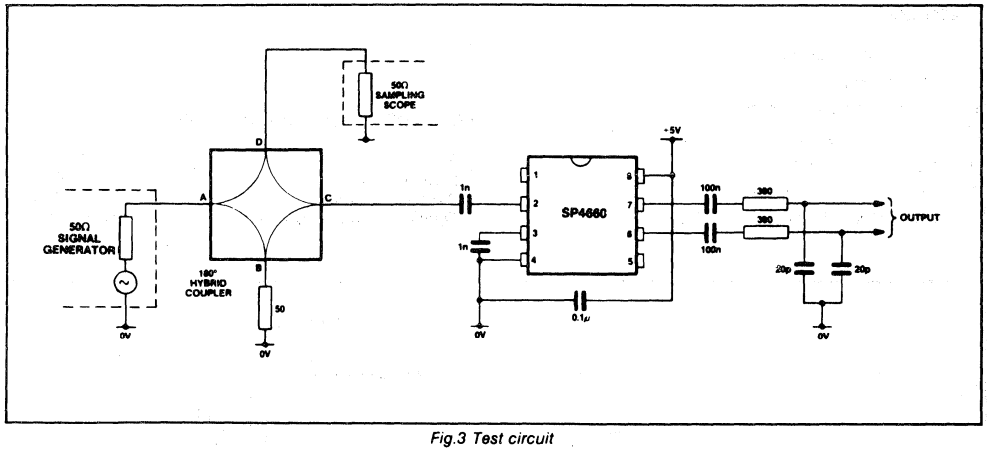


Fig.3 Test circuit

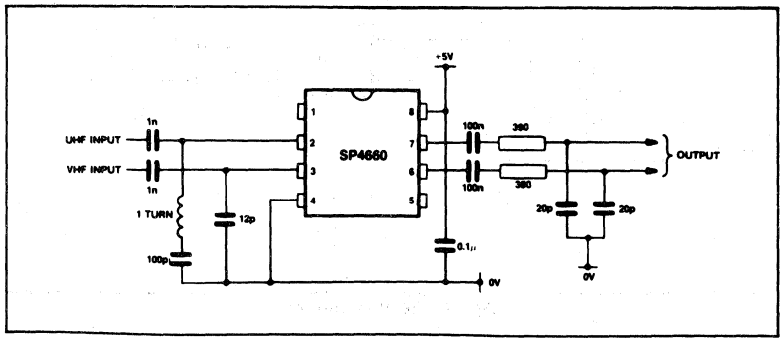


Fig.4 Application circuit

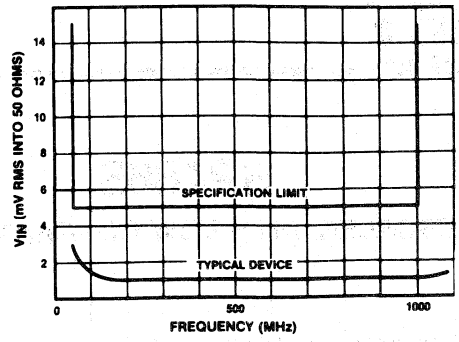


Fig.5 Typical input sensitivity

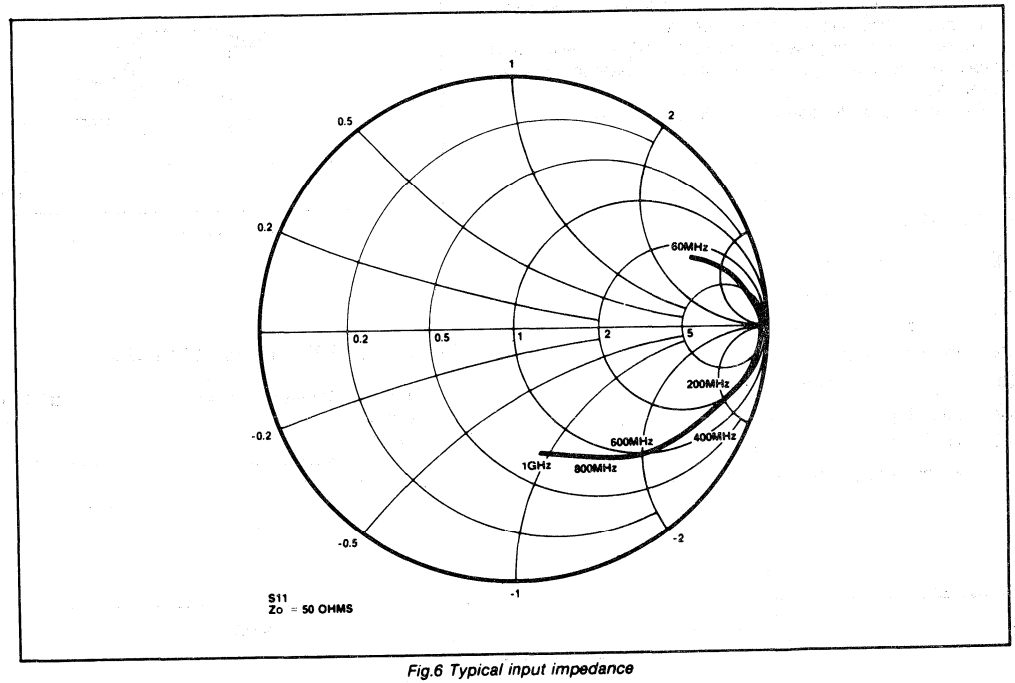


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4665

1GHz ÷ 64/256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4665 is a selectable division ratio high speed divider capable of replacing ECL output prescalers such as SP4632 and SP4653 with a single part in applications with alternative ÷ 64 and ÷ 256 division requirements.

An integrated low pass filter reduces radiation levels and saves the cost and space required by external filtering components.

Electrostatic protection is provided on all pins.

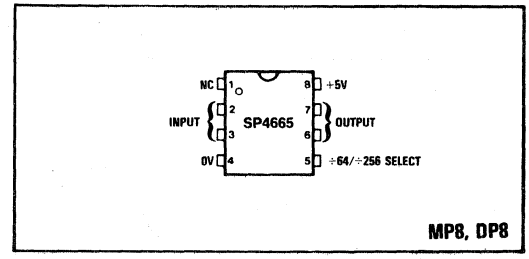


Fig.1 Pin connections - top view

FEATURES

- Ultra Low Radiation
- Active Output Filtering (3rd Order)
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**0°C to +80°C**
Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Junction temperature	+175°C

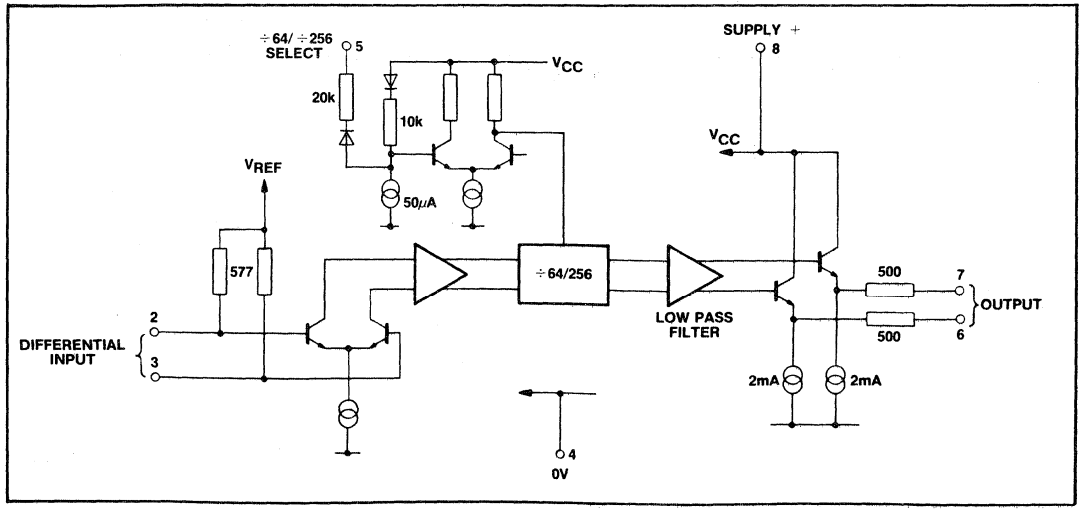


Fig.2 SP4665 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +80°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		36	42	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
70MHz			8	14	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	14	mV	
Input overload	2,3	300			mV	70MHz to 1050MHz operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage with 12p load	6,7	0.8	1		V p-p	÷64 mode, fin = 100MHz
		0.8	1		V p-p	÷256 mode, fin = 100MHz
		0.5	0.6		V p-p	÷64 mode, fin = 1GHz
		0.8	1		V p-p	÷256 mode, fin = 1GHz
Output impedance	6,7		500		ohms	
Output imbalance	6,7		0.1		V	
Voltage for ÷256 operation	5			1	V	
Voltage for ÷64 operation	5	3.5			V	See Note 1
Sink current for ÷256 operation	5			100	μA	V Pin 5 = 0V

NOTES

1. Pin 5 has an internal pull up and may be left open circuit for ÷64 operation.
2. The difference between the maximum input sensitivity and minimum input overload figures is the dynamic range of the device. For correct operation the input signal must be maintained within these limits at all frequencies.
3. The -3dB point of the output filter nominally corresponds to an input frequency of 1GHz, in ÷ 64 mode.

NOTE

The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

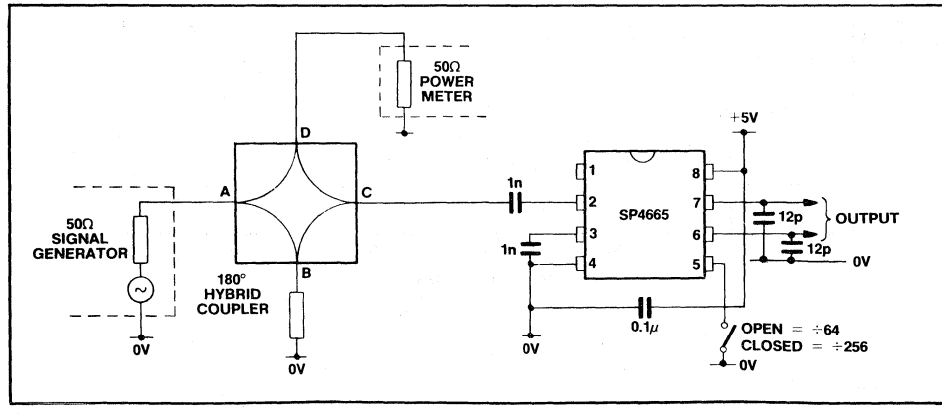


Fig.3 Test circuit

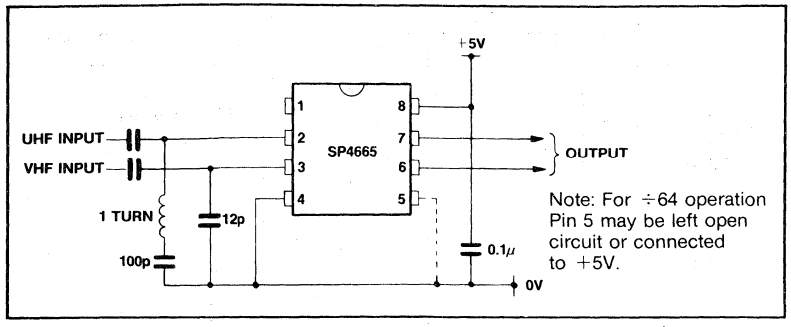


Fig.4 Application circuit

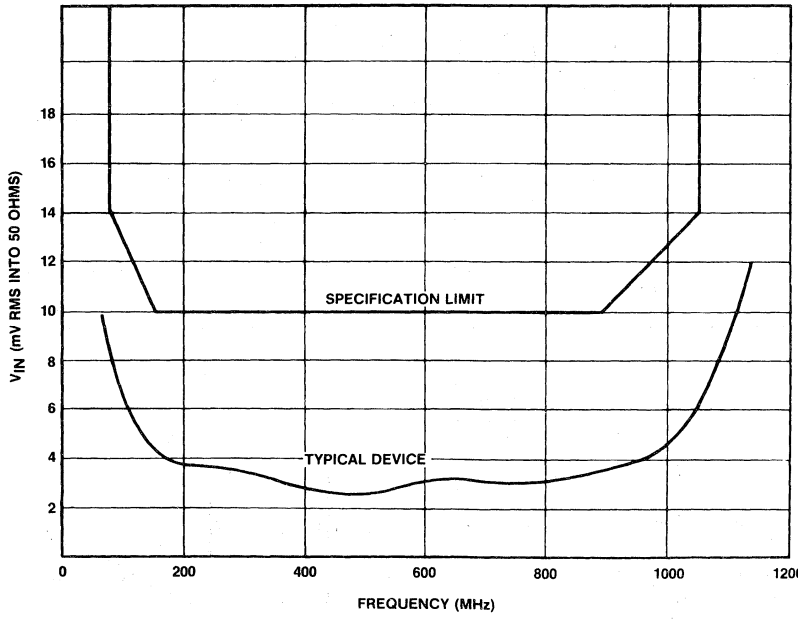


Fig.5 Typical input sensitivity

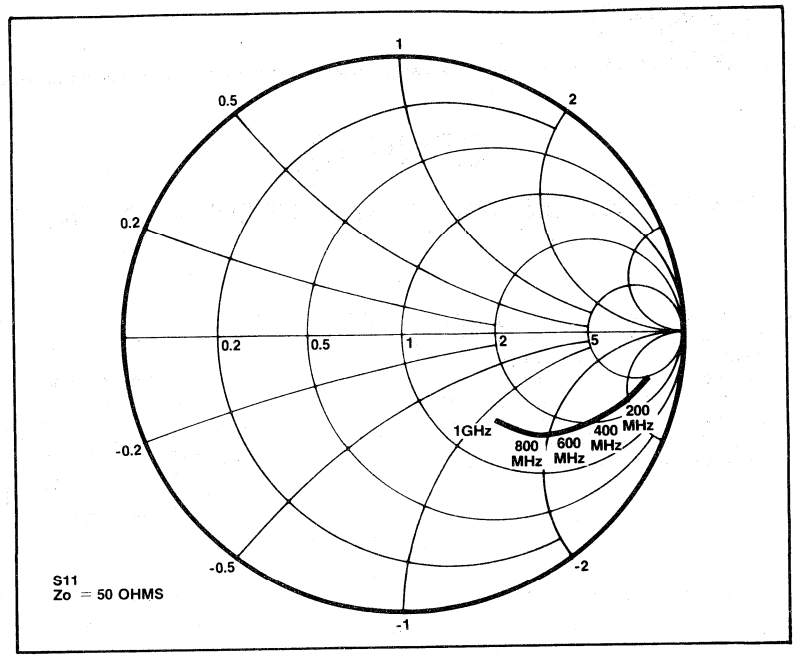


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4666

1.0GHz ÷ 64/256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4666 is a selectable division ratio high speed divider capable of replacing ECL prescalers such as SP4632 and SP4653 with a single part in applications with alternative ÷64 and ÷256 division requirements.

A switched low pass filter with -3dB points at 5.3MHz and 15.6MHz is connected before the output stage to reduce the harmonic content to very low levels.

Electrostatic protection is provided on all pins.

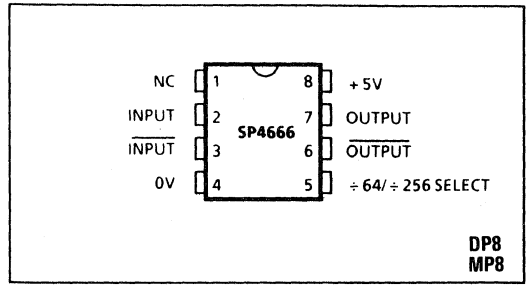


Fig 1 Pin Connections - top view

FEATURES

- Switched Low Pass Filter for Very Low Output Radiation
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	VCC + 7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to +125°C
Operating temperating range	0°C to +80°C

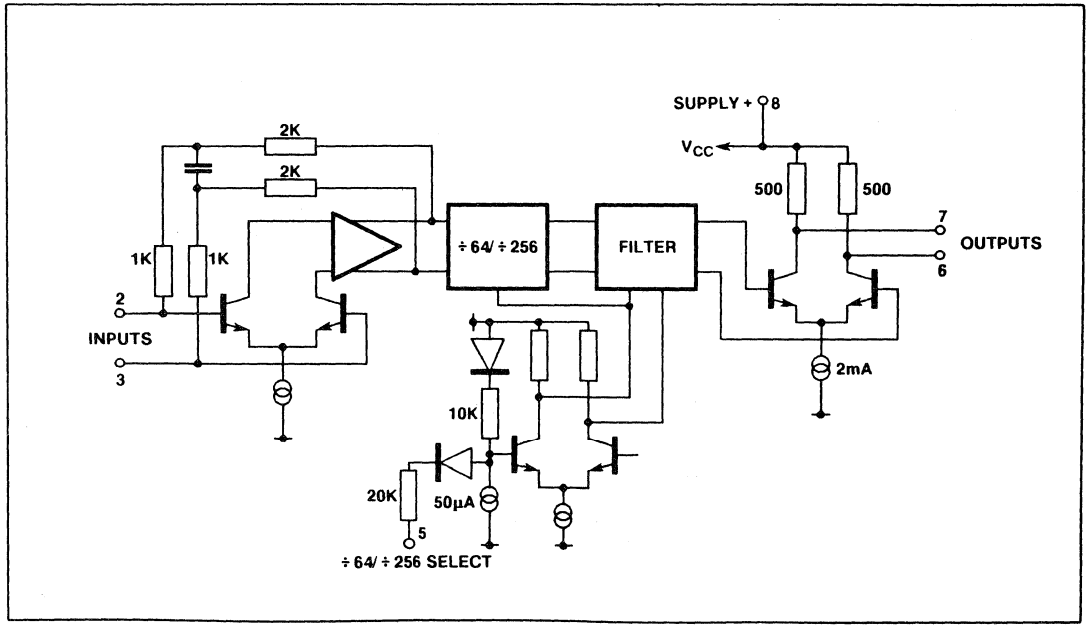


Fig. 2 SP4666 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +80°C, VCC = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	8		23	30	mA	VCC = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			2.5	10	mV	
200MHz to 1050MHz			0.5	5	mV	
Input overload	2,3	500			mV	
Input impedance	2,3		50		ohms	See fig.6
			2		pF	
Output voltage with 12pF load	6,7					
		0.8	1		Vp-p	÷64 mode fin = 100MHz
		0.8	1		Vp-p	÷256 mode
		0.4	0.5		Vp-p	÷64 mode fin = 1000MHz
		0.7	0.9		Vp-p	÷256 mode
Output impedance	6,7		500		ohms	
Output imbalance	6,7		0.1		V	
Voltage for ÷256 operation	5			0.5	V	
Voltage for ÷64 operation	5	3.5			V	See Note 1
Sink current for ÷256 operation	5			250	µA	V pin 5 = 0V

NOTES
1. Pin 5 has an internal pull up and may be left open circuit for ÷64 operation
2. The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device. For correct operation the input signal must be maintained between these limits at all frequencies

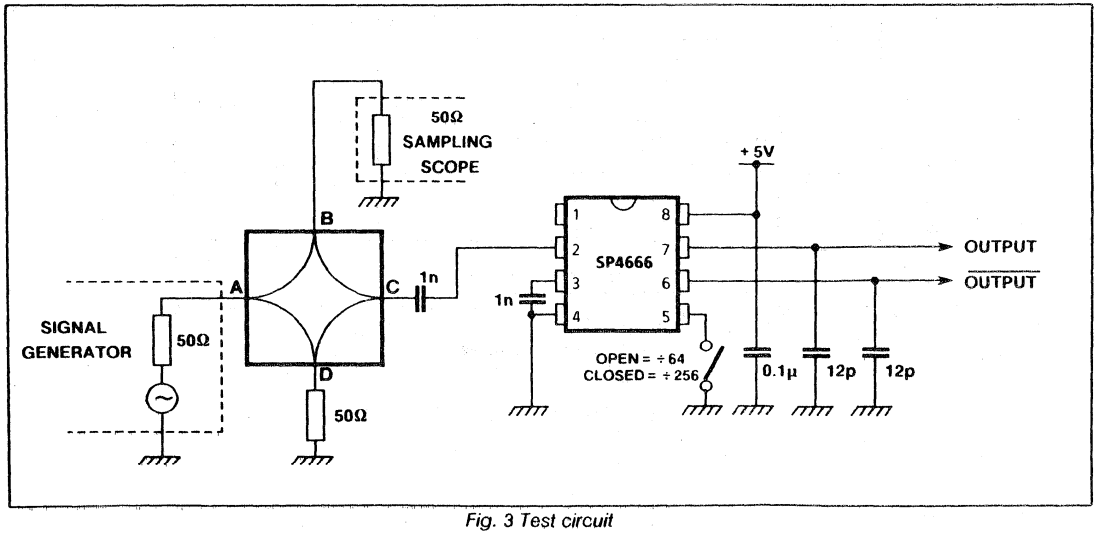


Fig. 3 Test circuit

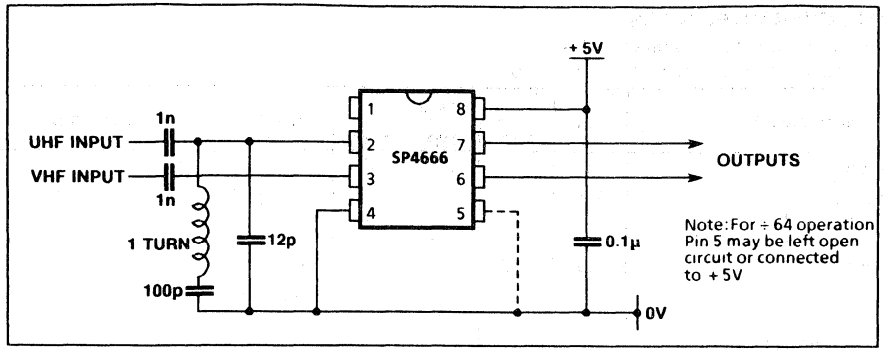


Fig.4 Application circuit

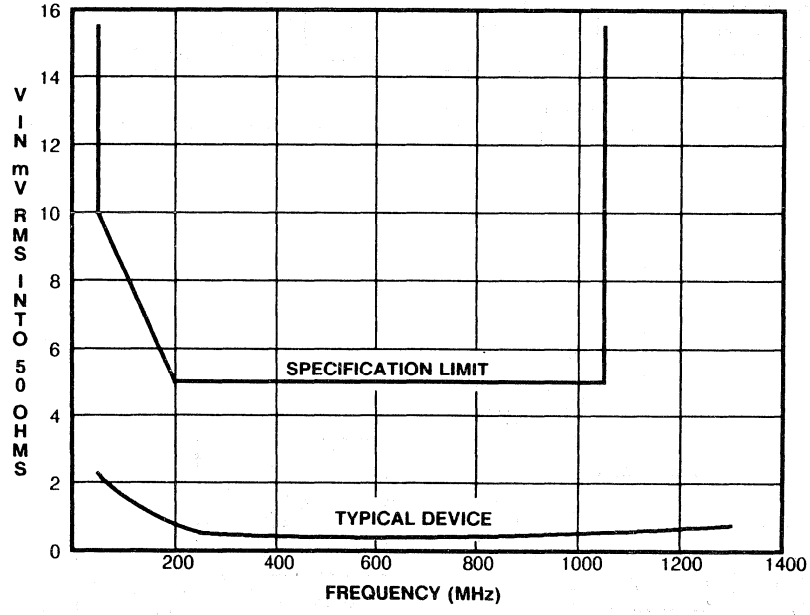


Fig.5 Typical input sensivity

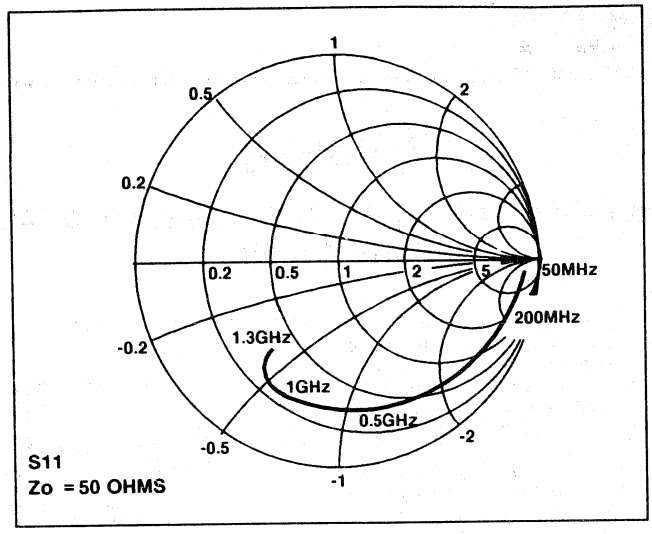


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4676

950MHz ÷ 128/136, ÷ 64/68 VERY LOW RADIATION DUAL MODULUS PRESCALER

The SP4676 ÷ 128/136, ÷64/68 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8 pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4676 incorporates an on chip preamplifier and has a single ECL output. The control input is latched and synchronised making the device highly tolerant to delays in the control loop.

Electrostatic protection is provided on all pins.

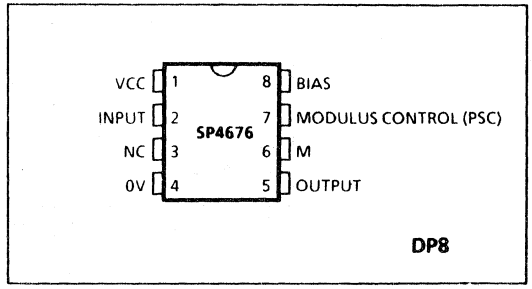


Fig 1 Pin Connections - top view

FEATURES

- Low Supply Current
- Very Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- Latched and Synchronised Modulus Control Input
- Single ECL Output
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC} + 7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to + 125°C
Control input voltage (PSC)	-0.5V to V_{CC}
Operating temperating range	0°C to + 70°C

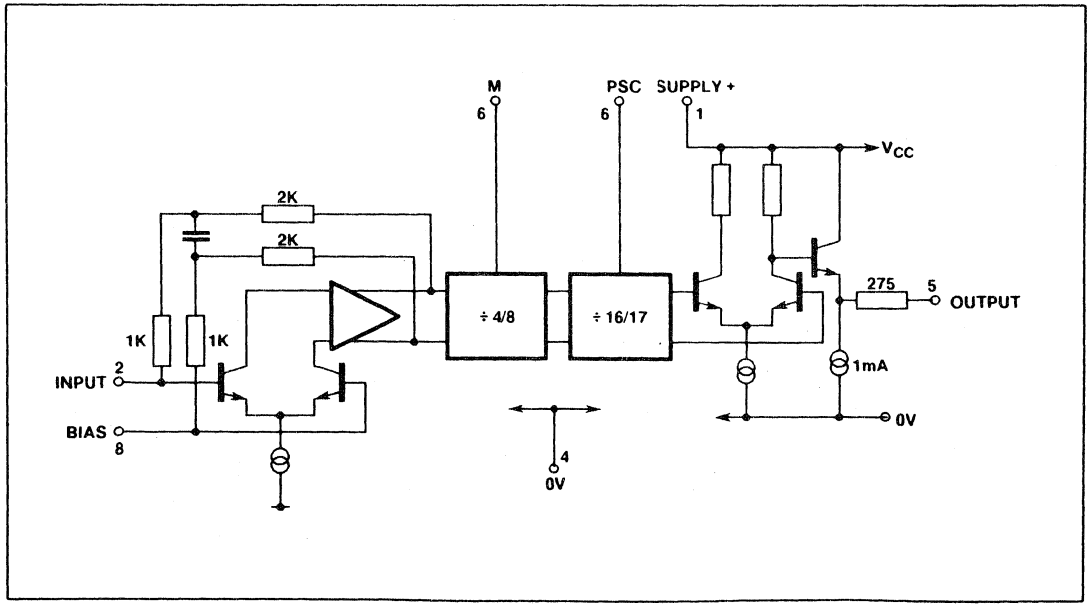


Fig. 2 SP4676 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +70°C, VCC = +4.5V to +5.5V with 10ns rise and fall time on PSC input.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		16	21	mA	VCC = 5V
Input sensitivity (see Fig. 3)	2					RMS sinewave
Input overload 50 to 950MHz (see note)	2	400			mV	
Input impedance	2		50 2		ohms pF	See fig.7
Output voltage	5		1.2		Vp-p	15pF load, fo ≤3.5MHz
		1.0			Vp-p	15pF load, fo ≤7.5MHz
High level input voltage	7	$0.7V_{CC}$			V	÷68/136 mode
Low level input voltage	7			$0.3V_{CC}$	V	÷64/128 mode
High level input current	7			10	µA	
High level input voltage	6	$0.6V_{CC}$			V	÷64/68 mode
Low level input voltage	6			$0.4V_{CC}$	V	÷128/136 mode
High level input current	6			10	µA	

NOTE
The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device.For correct operation the input signal must be maintained between these limits at all frequencies

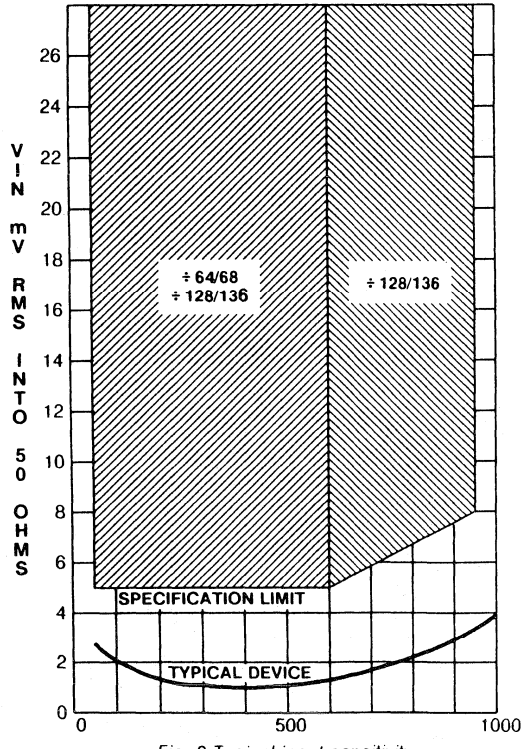


Fig. 3 Typical input sensitivity

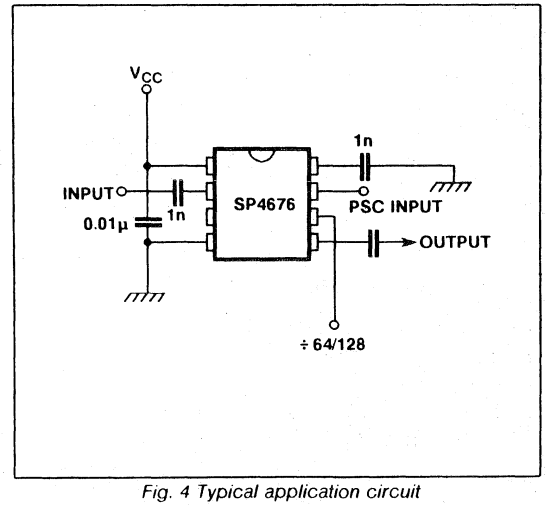


Fig. 4 Typical application circuit

NOTES(Refer to Fig. 6 opposite)

1. The PSC input is sampled at 2 points in each output half cycle, the sampling points being 25% and 50% of the high or low output period from the output transitions (see Fig. 6a).
2. The PSC input must be high for both sampling points in a high or low output period to increase the division ratio for that output period (see Fig. 6b).
3. The rising edge of the swallow pulse should occur at least 30ns before the 25% sampling point.
4. The division ratio may only be increased for either the positive or negative portion of any output cycle.

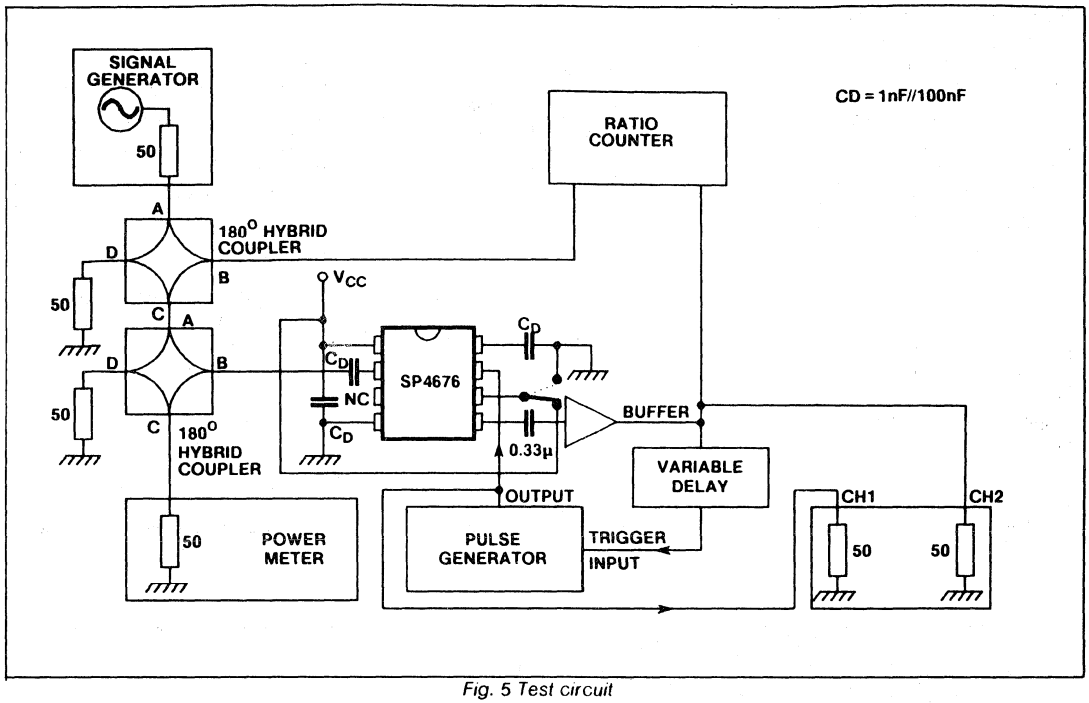


Fig. 5 Test circuit

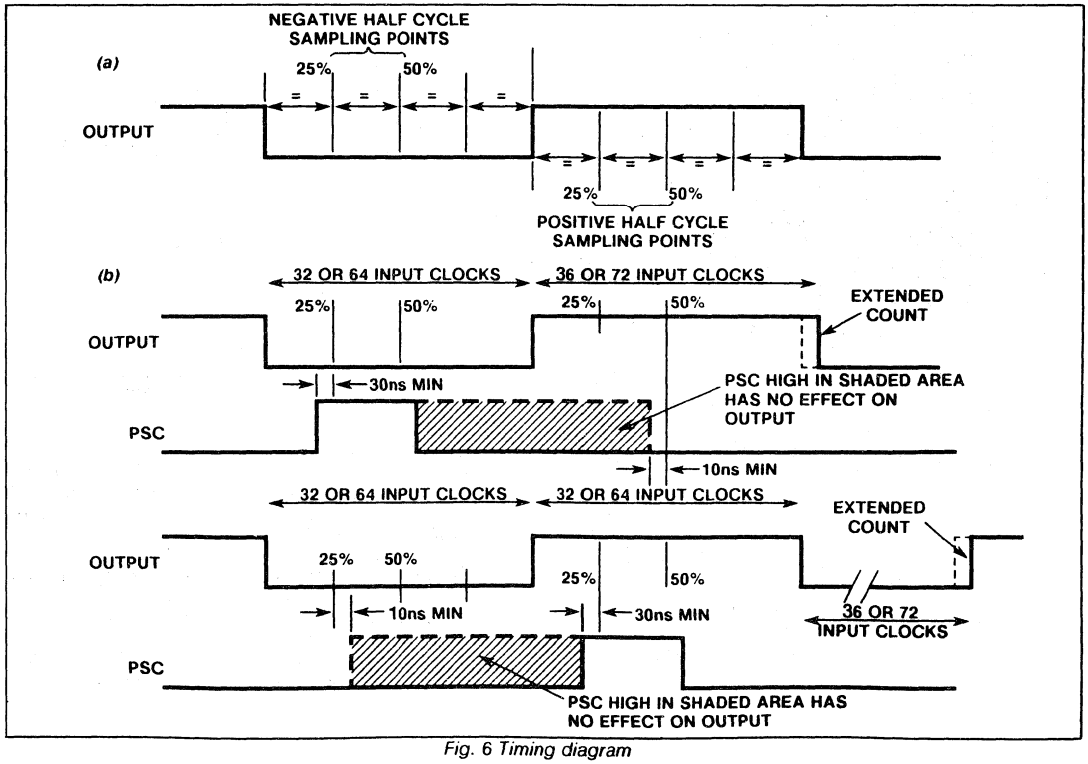


Fig. 6 Timing diagram

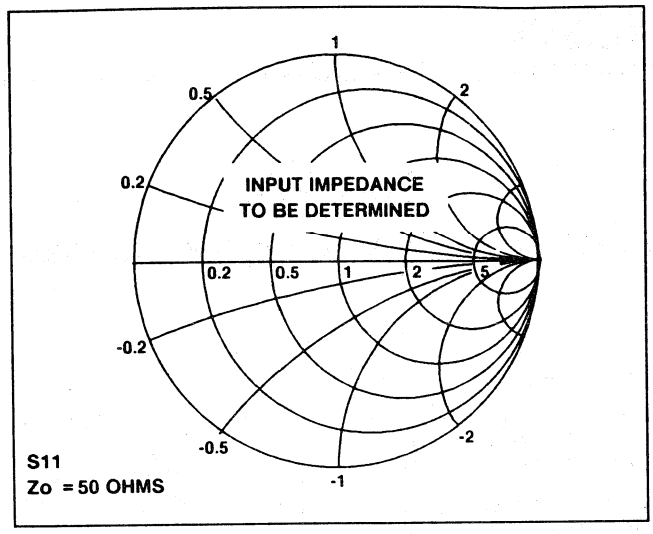


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4678

1.2GHz ÷ 128/136, ÷ 64/68 DUAL MODULUS PRESCALER

The SP4678 ÷ 128/136, ÷64/68 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8 pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4678 incorporates an on chip preamplifier and has a single ECL output. The control input is latched and synchronised making the device highly tolerant to delays in the control loop.

Electrostatic protection is provided on all pins.

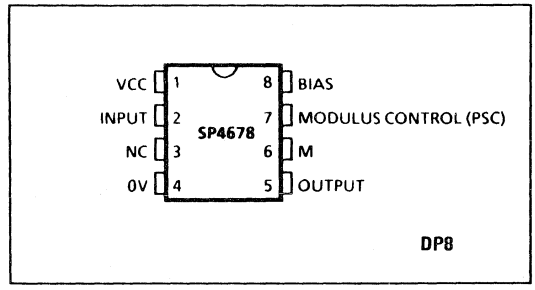


Fig 1 Pin Connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- Latched and Synchronised Modulus Control Input
- Single ECL Output
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC} + 7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to + 125°C
Control input voltage (PSC)	-0.5V to V_{CC}
Operating temperating range	0°C to + 70°C

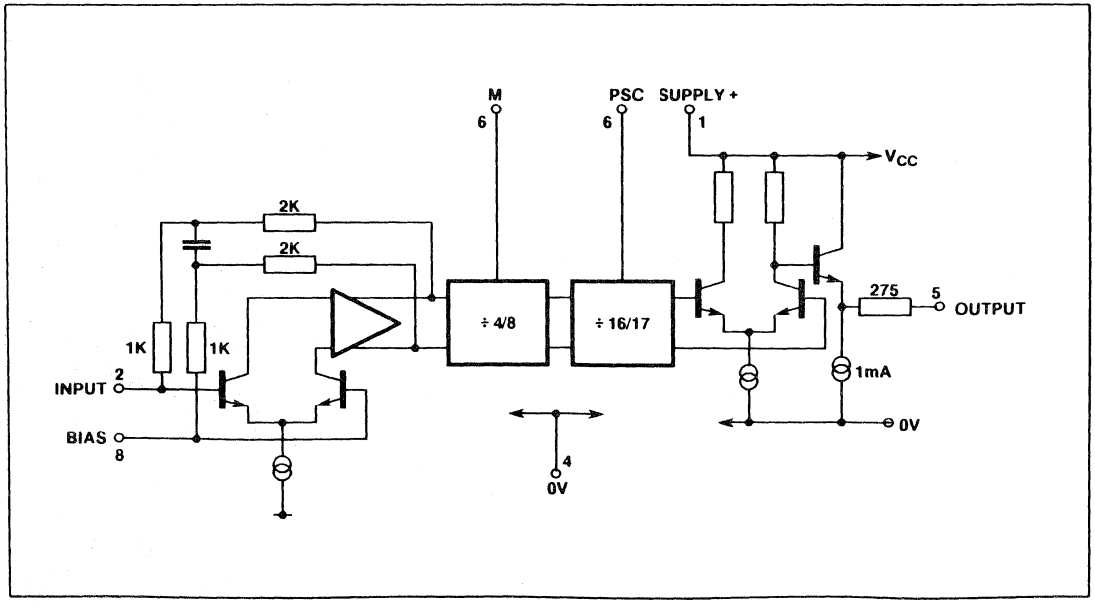


Fig. 2 SP4678 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +70°C, VCC = +4.5V to +5.5V with 10ns rise and fall time on PSC input.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		16	21	mA	VCC = 5V
Input sensitivity (see Fig. 3)	2					RMS sinewave
Input overload 50 to 1200MHz (see note)	2	400			mV	
Input impedance	2		50 2		ohms pF	See fig.7
Output voltage	5		1.2		Vp-p	15pF load, fo ≤ 10MHz
		1.0			Vp-p	15pF load, fo ≤ 17.2MHz
High level input voltage	7	$0.7V_{CC}$			V	÷68/136 mode
Low level input voltage	7			$0.3V_{CC}$	V	÷64/128 mode
High level input current	7			10	µA	
High level input voltage	6	$0.6V_{CC}$			V	÷64/68 mode
Low level input voltage	6			$0.4V_{CC}$	V	÷128/136 mode
High level input current	6			10	µA	

NOTE
The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device. For correct operation the input signal must be maintained between these limits at all frequencies

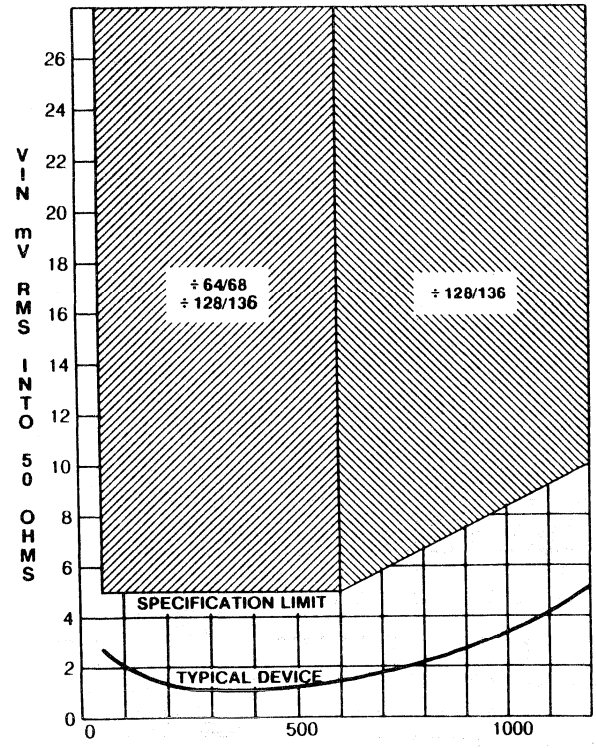


Fig. 3 Typical input sensitivity

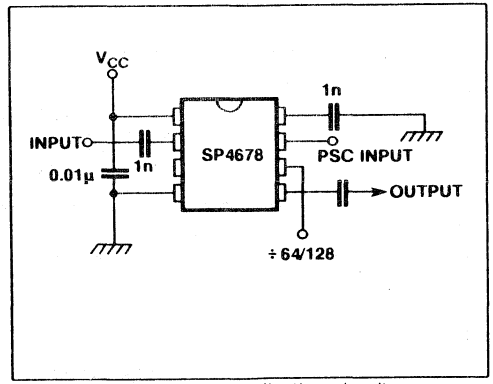


Fig. 4 Typical application circuit

NOTES(Refer to Fig. 6 opposite)

1. The PSC input is sampled at 2 points in each output half cycle, the sampling points being 25% and 50% of the high or low output period from the output transitions (see Fig. 6a).
2. The PSC input must be high for both sampling points in a high or low output period to increase the division ratio for that output period (see Fig. 6b).
3. The rising edge of the swallow pulse should occur at least 30ns before the 25% sampling point.
4. The division ratio may only be increased for either the positive or negative portion of any output cycle.

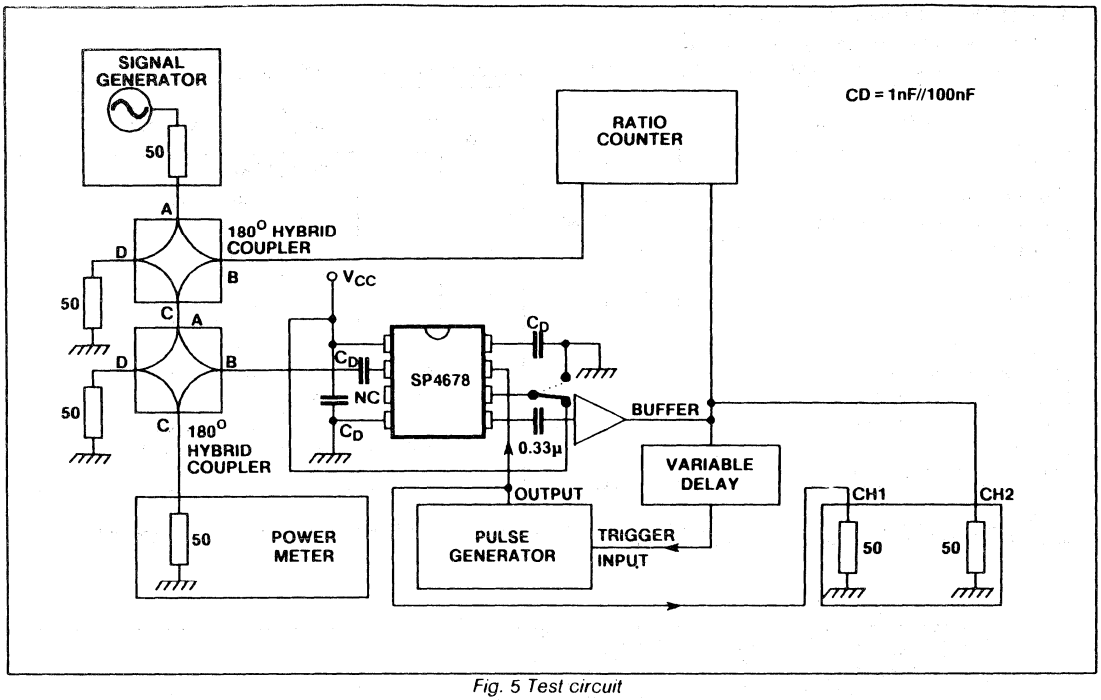


Fig. 5 Test circuit

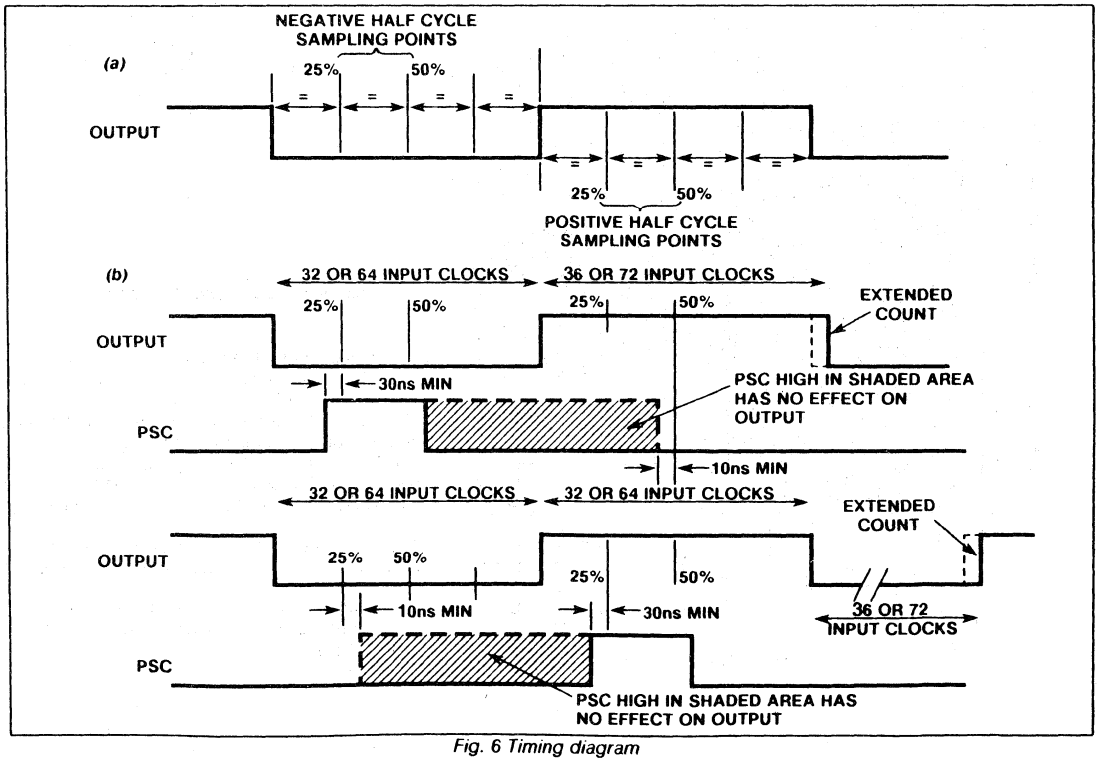


Fig. 6 Timing diagram

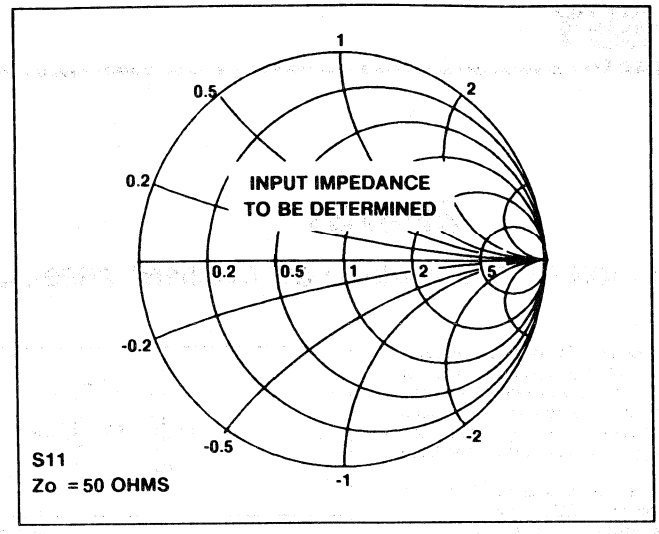


Fig.6 Typical input impedance

SP4731

1.3GHz ÷ 64 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4731 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4731 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

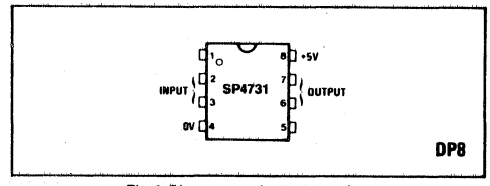


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

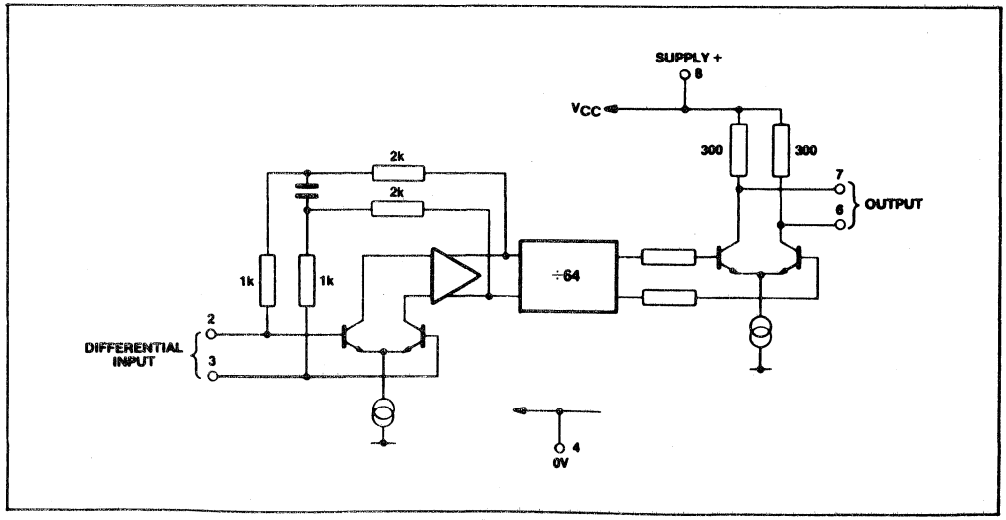


Fig.2 SP4731 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1.3GHz V_{CC} = 5V
	7	1.0			V p-p	
Output voltage load as Fig.3	6	0.8			V p-p	fin = 1.3GHz V_{CC} = 5V
	7	0.8			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

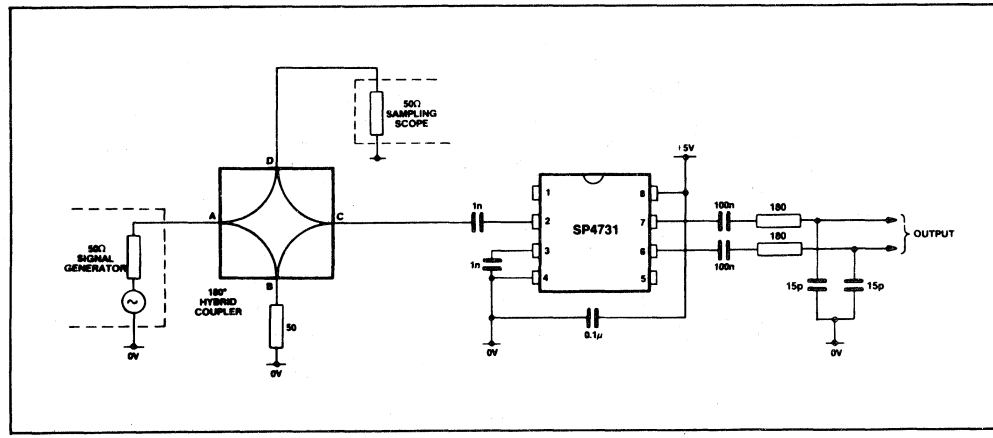


Fig.3 Test circuit

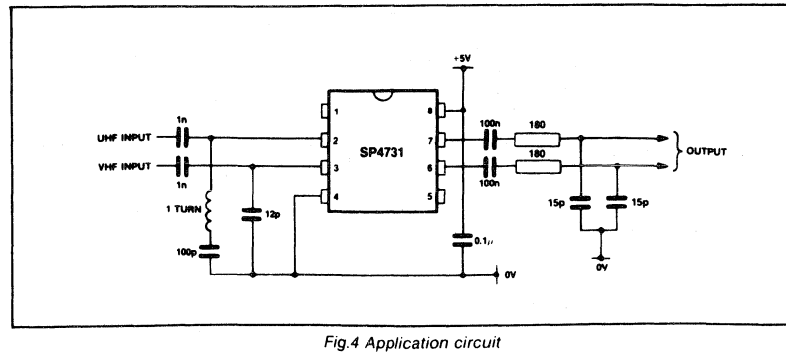


Fig.4 Application circuit

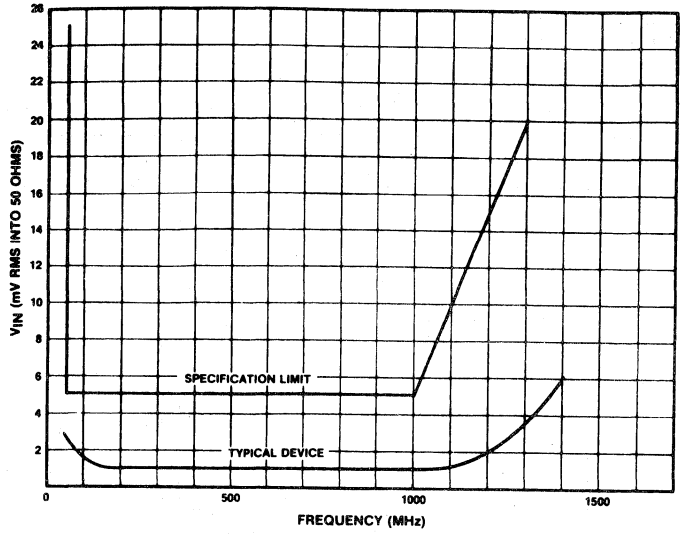


Fig.5 Typical input sensitivity

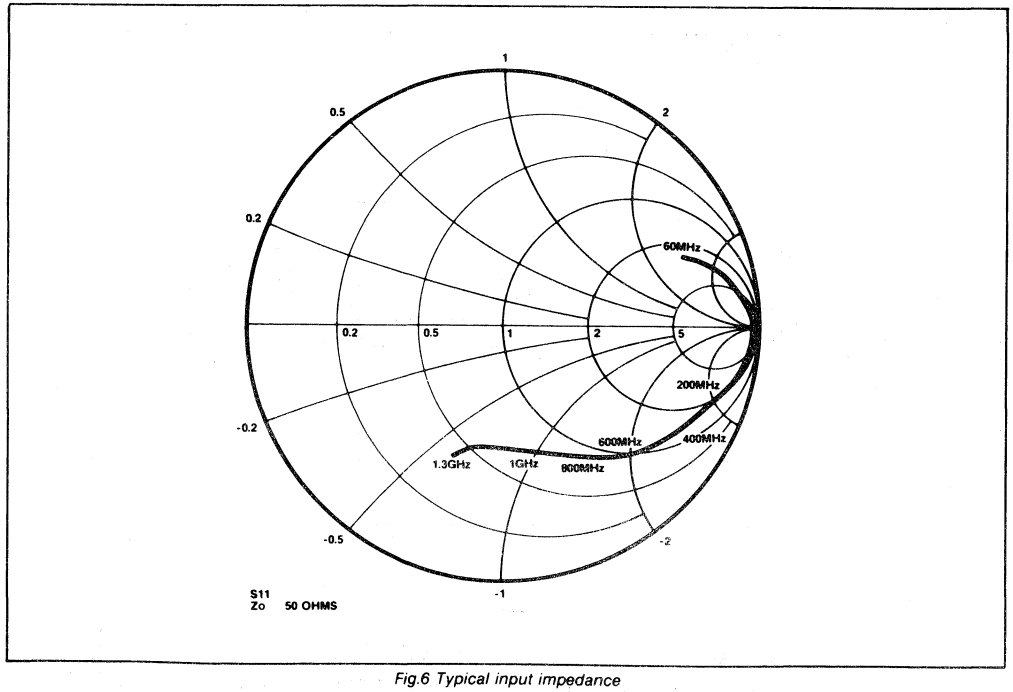


Fig.6 Typical input impedance

SP4740

1.3GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4740 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4740 incorporates an on-chip preamplifier with differential inputs, and has a single TTL output.

Electrostatic protection is provided on all pins.

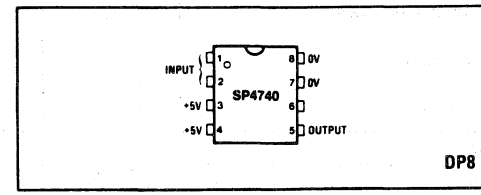


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- TTL Output
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

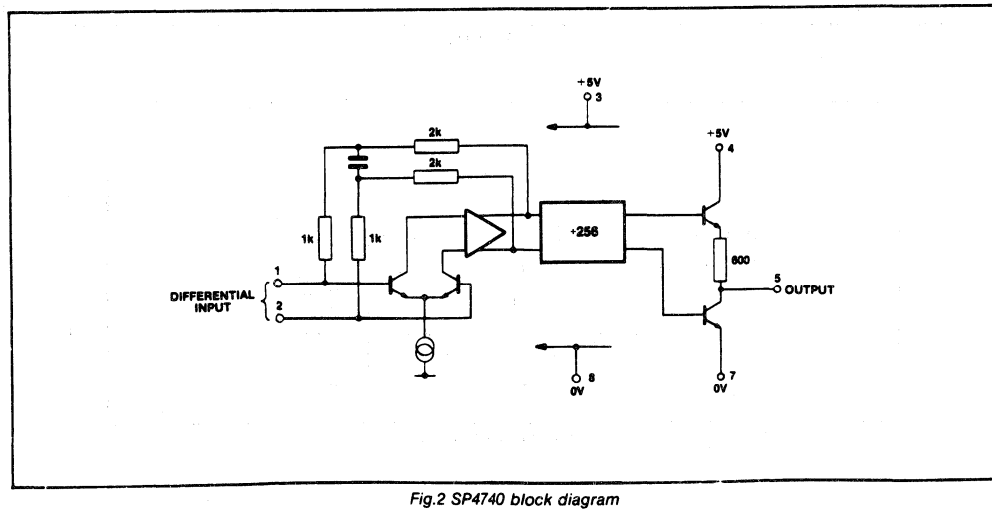


Fig.2 SP4740 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +70° C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage						
High	5	3.3			V	Sourcing 0.2mA
Low	5			0.4	V	Sinking 2mA

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

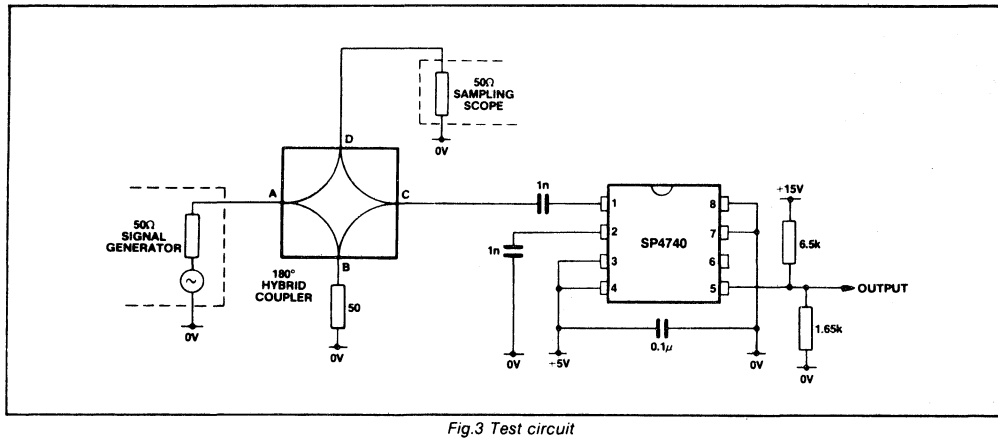


Fig.3 Test circuit

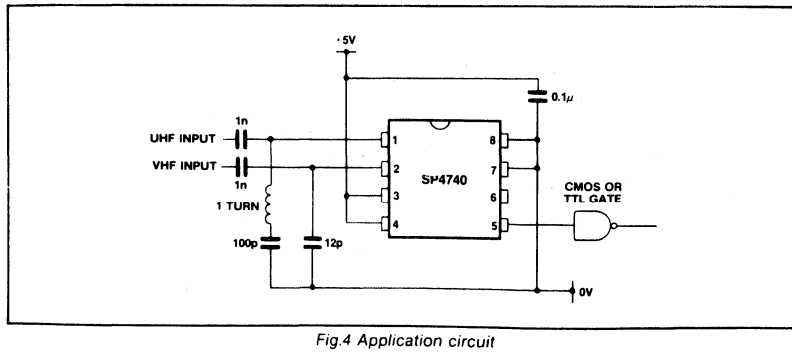


Fig.4 Application circuit

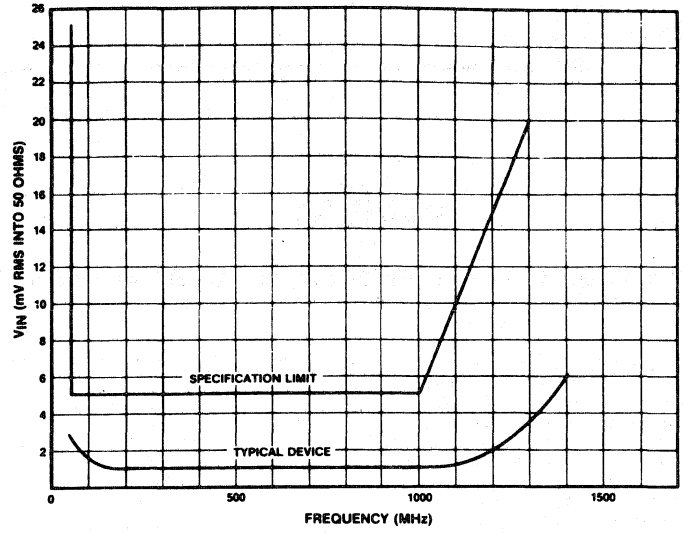


Fig.5 Typical input sensitivity

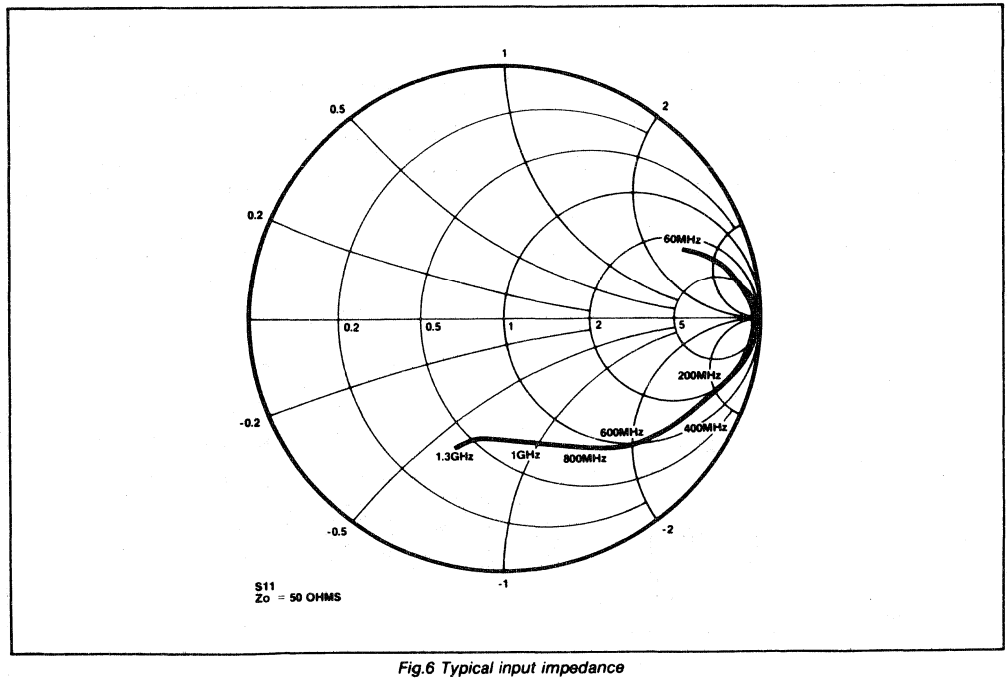


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4751

1.3GHz ÷ 256 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4751 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4751 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

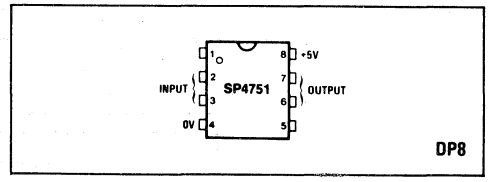


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

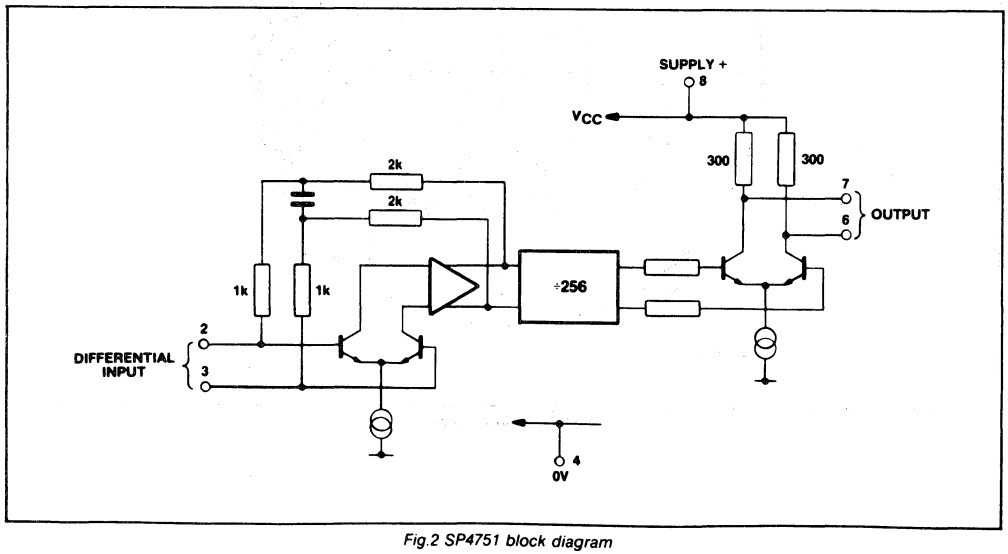


Fig.2 SP4751 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C Vcc = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1.3GHz Vcc = 5V
	7	1.0			V p-p	
Output voltage load as Fig.3	6	0.8			V p-p	fin = 1.3GHz Vcc = 5V
	7	0.8			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

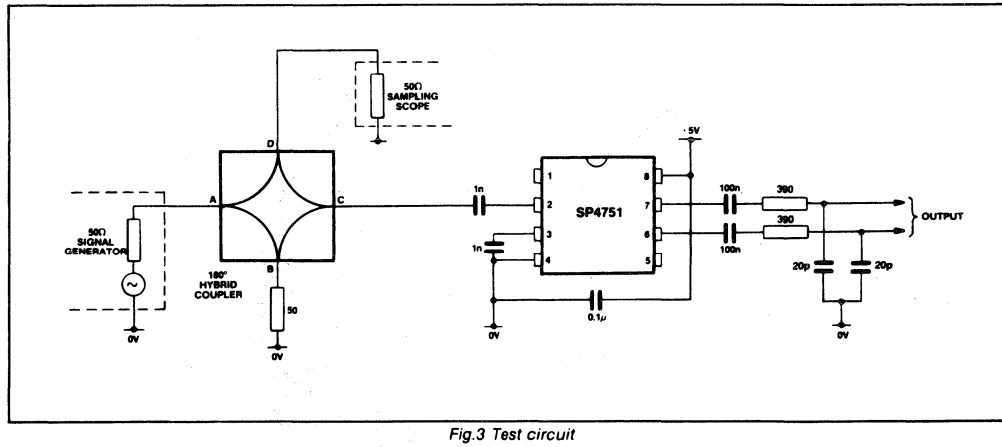


Fig.3 Test circuit

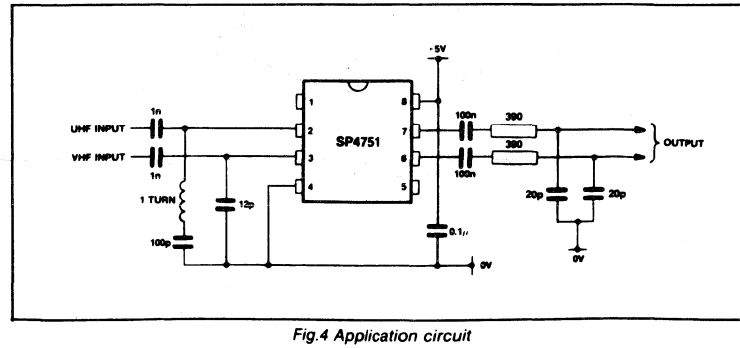


Fig.4 Application circuit

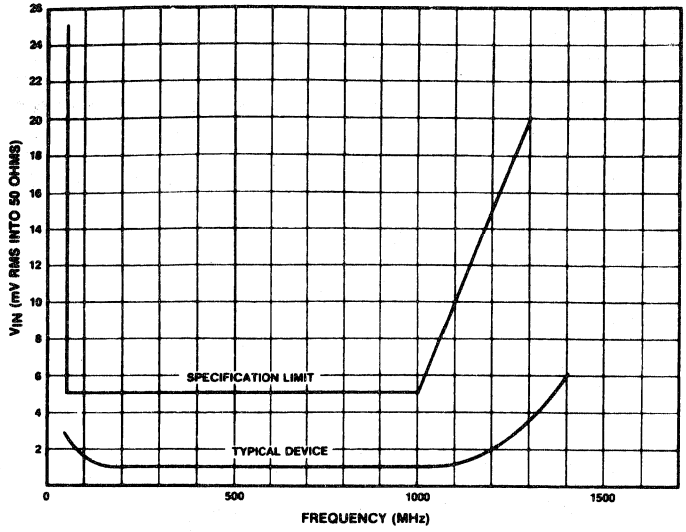


Fig.5 Typical input sensitivity

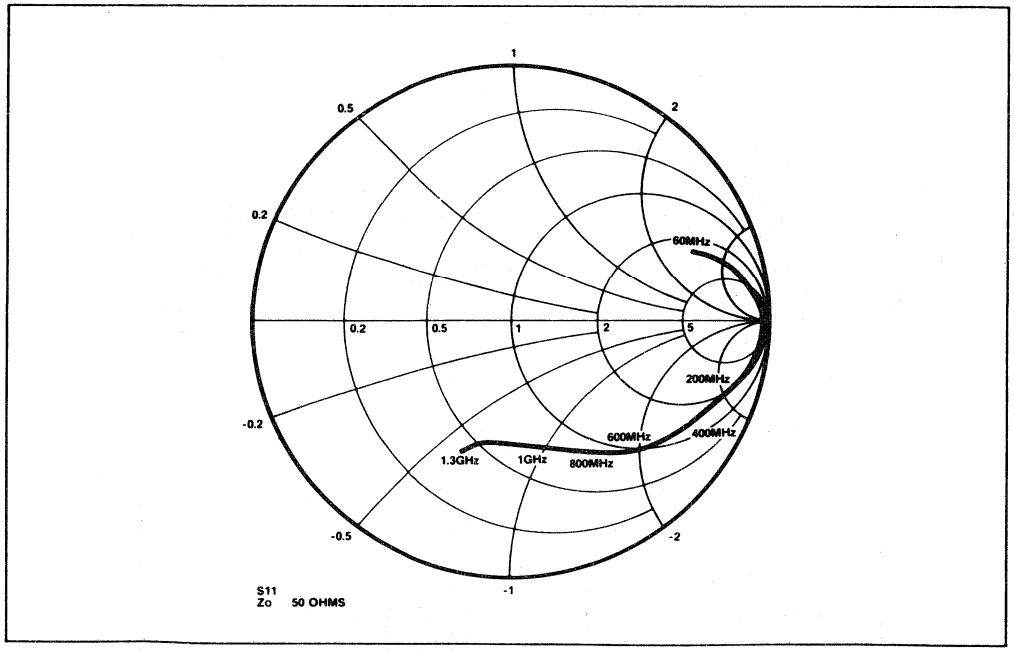


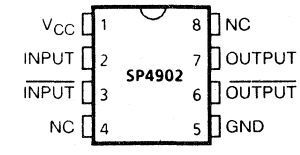
Fig.6 Typical input impedance

PLESSEY
Semiconductors

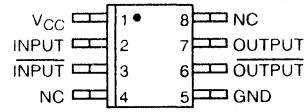
SP4902

2.5GHz ÷ 2 PRESCALER

The SP4902 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.



DP8



MP8

Fig 1 Pin Connections - top view

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

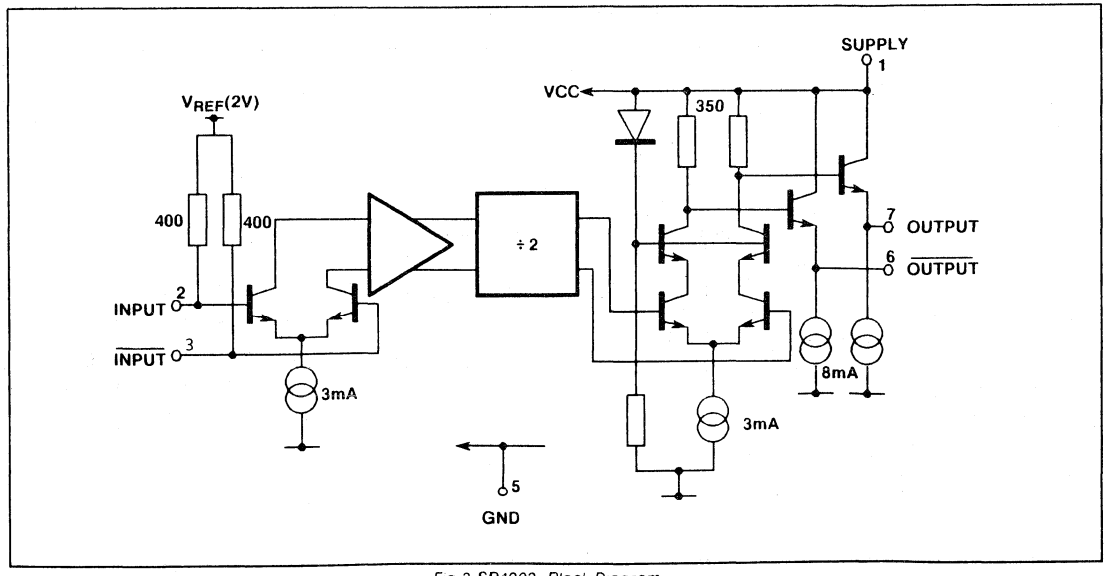


Fig 2 SP4902 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		51		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 2500MHz	6,7		0.3		Vp-p	V_{CC} = 5V Load as fig.4

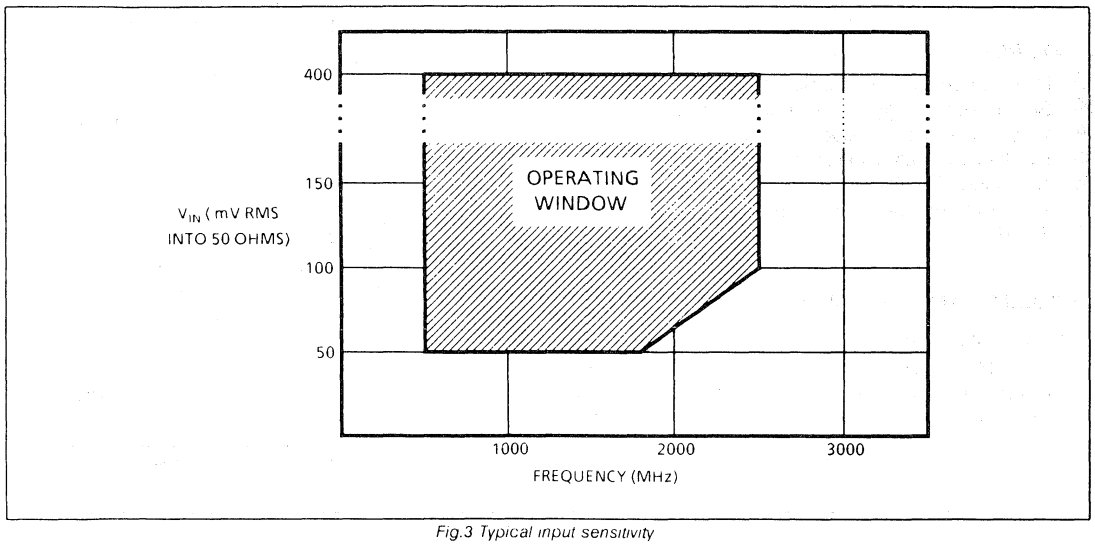


Fig.3 Typical input sensitivity

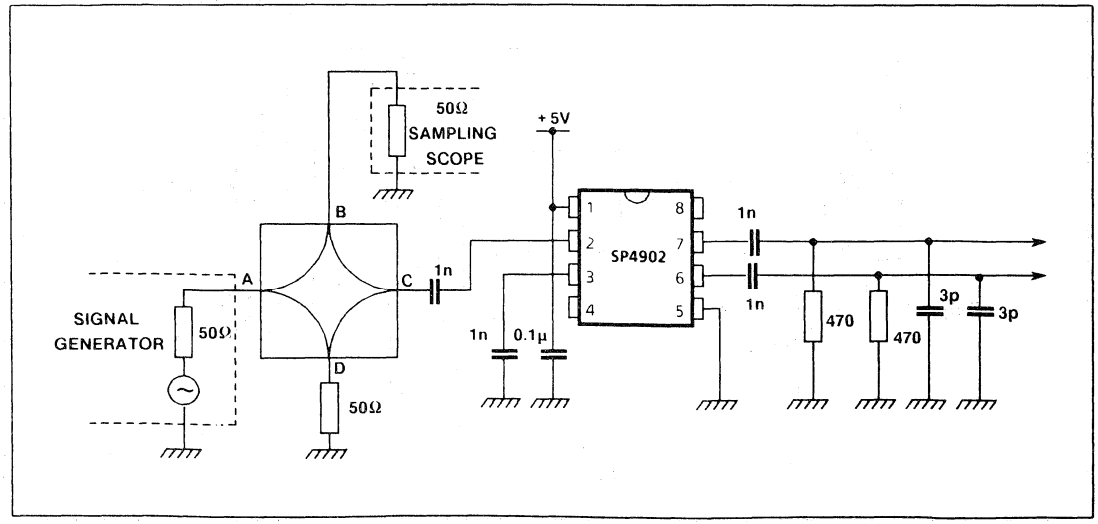


Fig.4 Test circuit

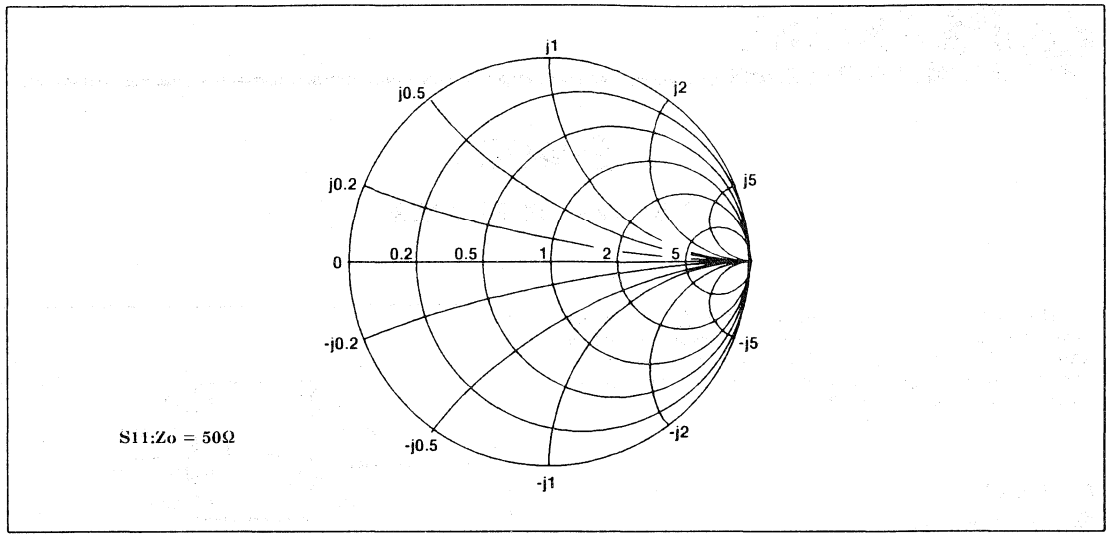


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP4904

2.5GHz ÷ 4 PRESCALER

The SP4904 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 220mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

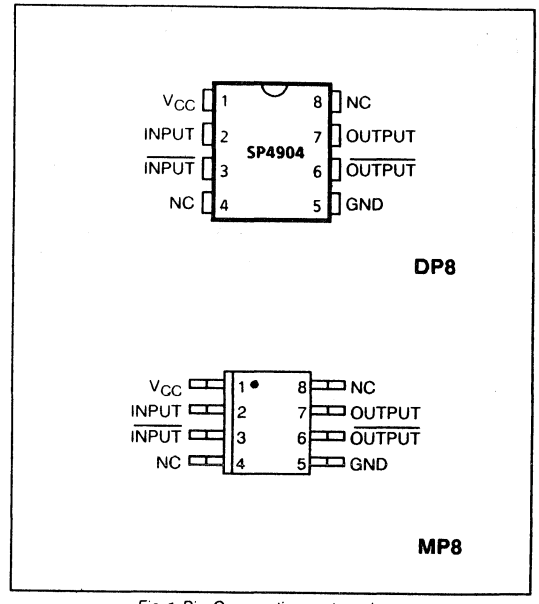


Fig 1 Pin Connections - top view

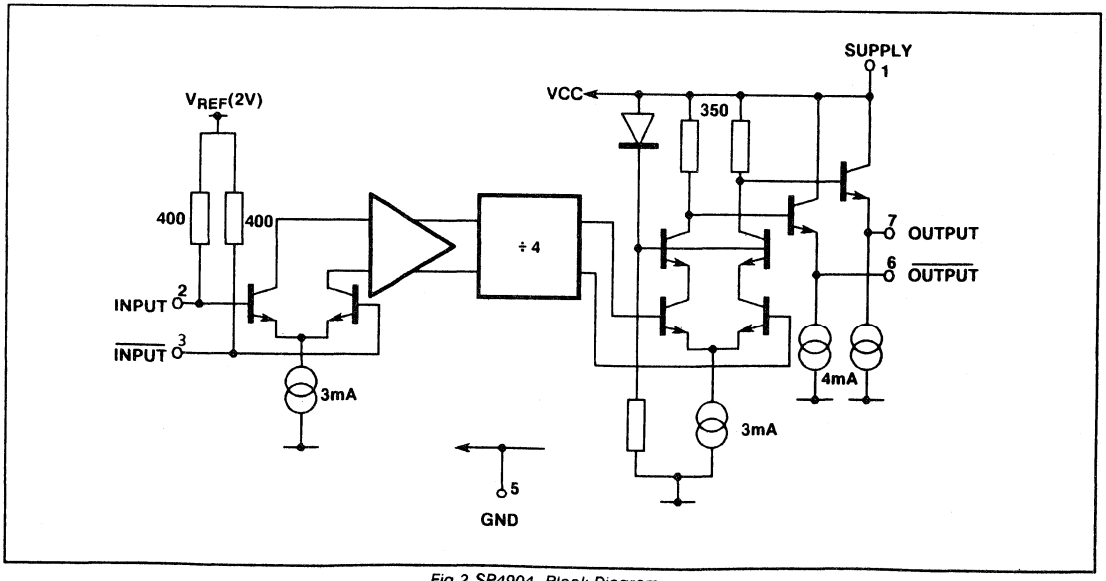


Fig 2 SP4904 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		46		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 2500MHz	6,7		0.3		Vp-p	V_{CC} = 5V Load as fig.4

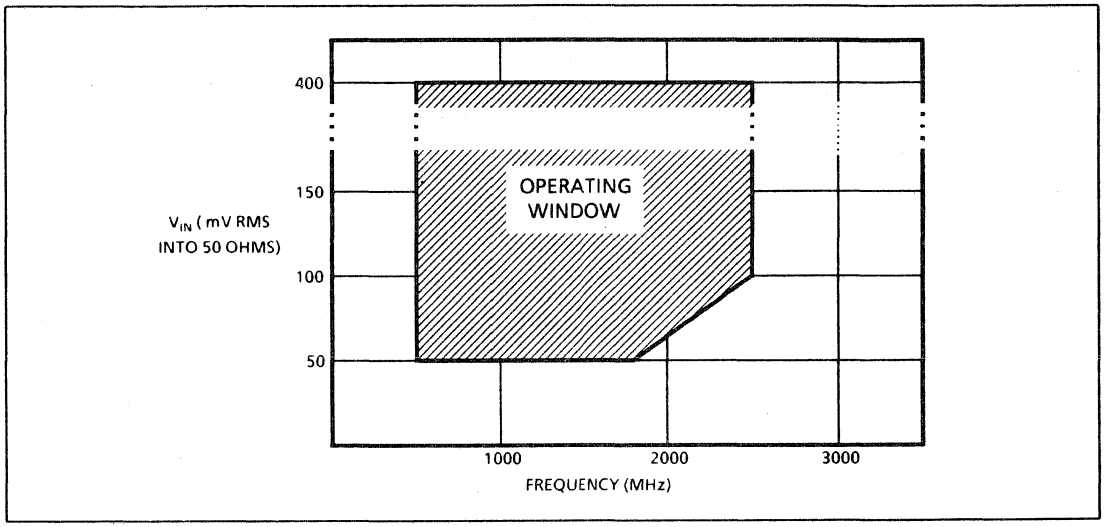


Fig.3 Typical input sensitivity

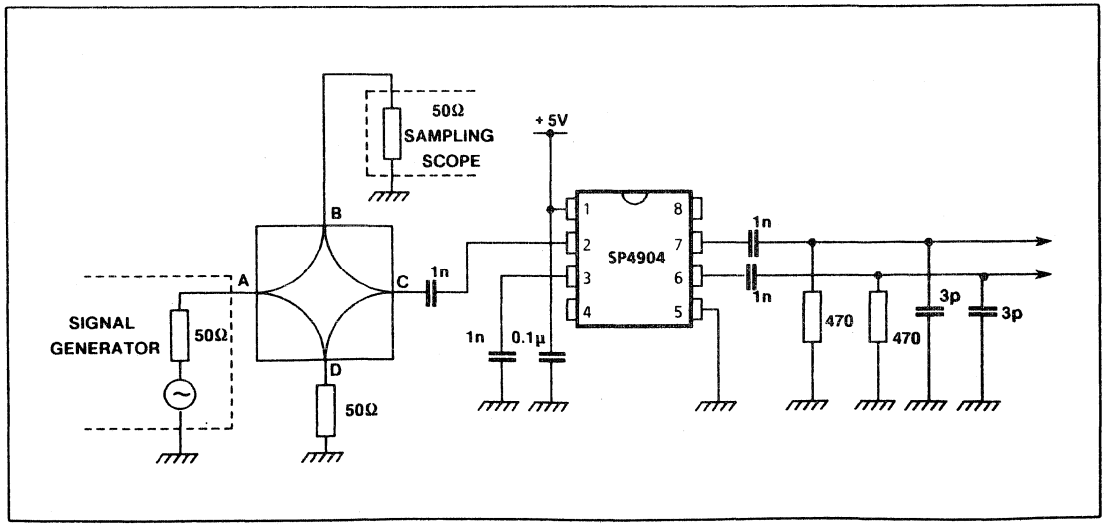


Fig.4 Test circuit

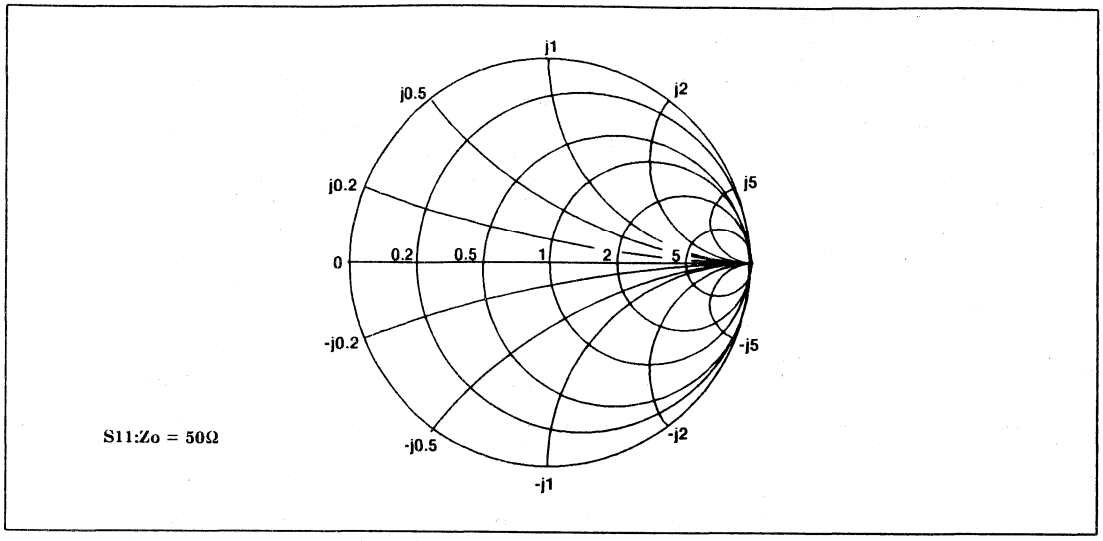


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP4914

2.5GHz ÷ 128 PRESCALER

The SP4914 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

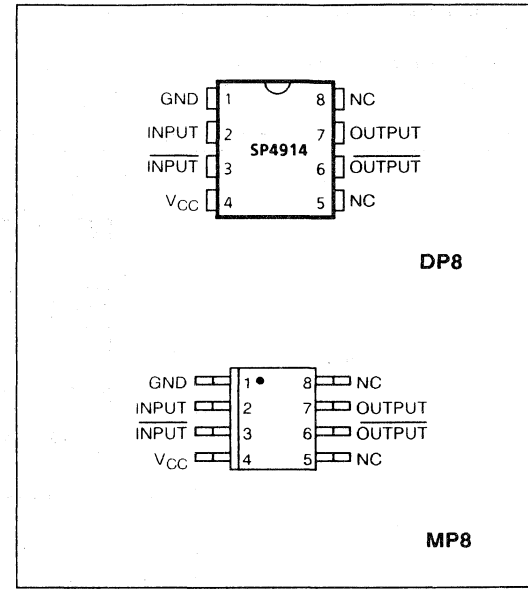


Fig 1 Pin Connections - top view

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

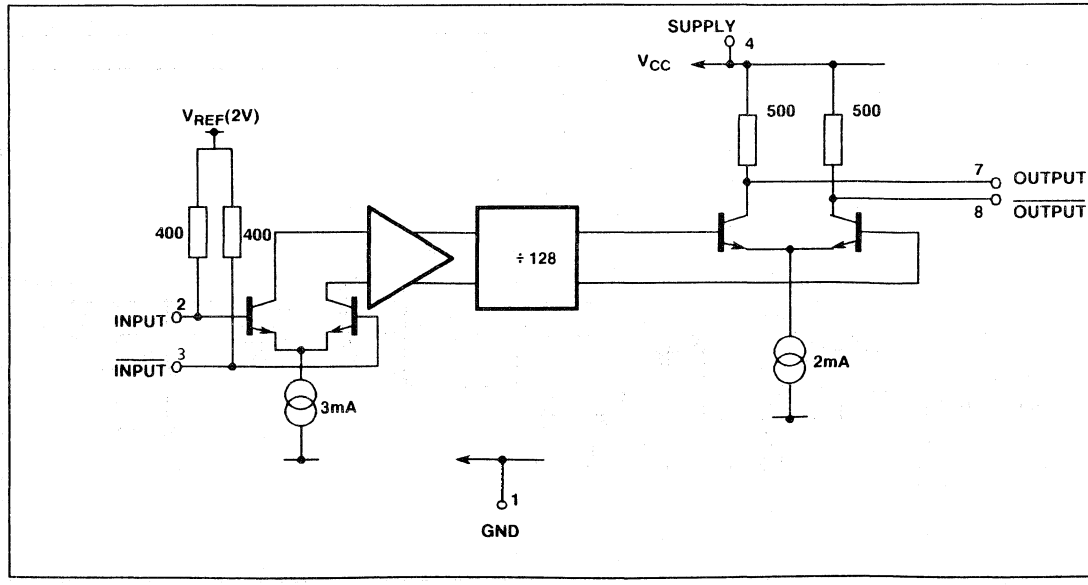


Fig 2 SP4914 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		44		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 2500MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V No Load
Output voltage with fin = 2500MHz	6,7	0.55	0.8		Vp-p	V_{CC} = 5V Load as fig.4

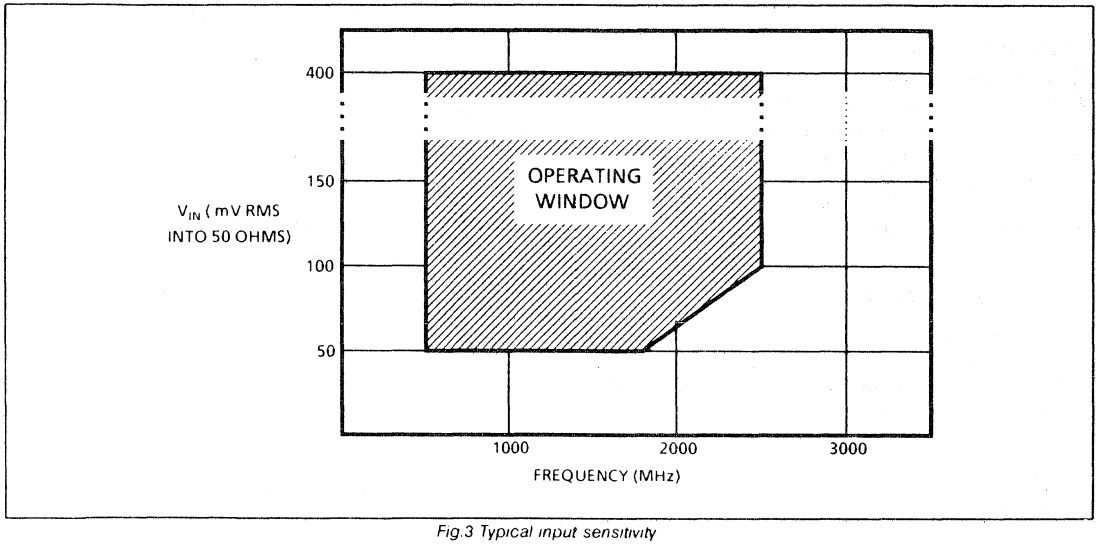


Fig.3 Typical input sensitivity

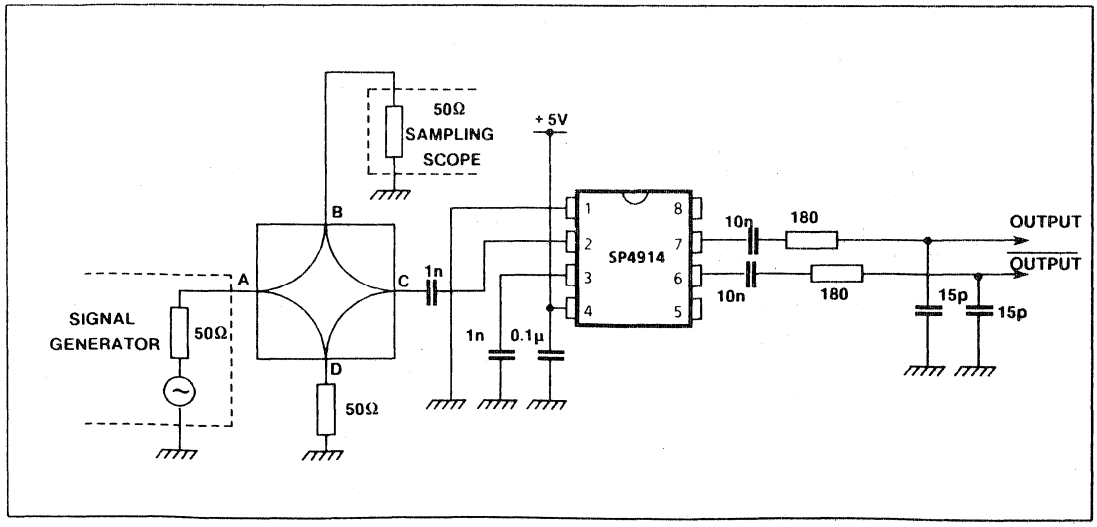


Fig.4 Test circuit

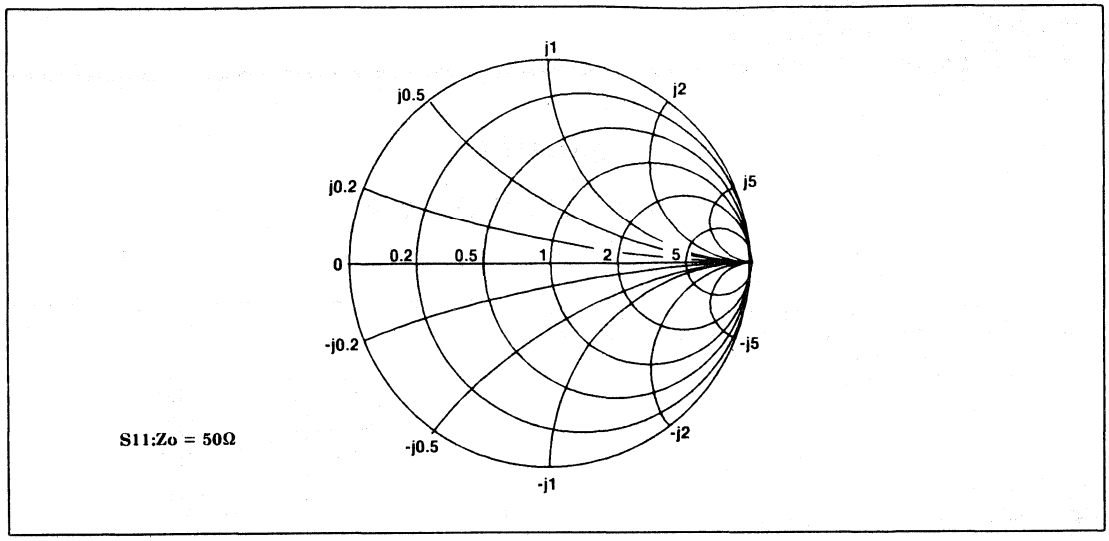


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP4916

2.5GHz ÷ 512 PRESCALER

The SP4916 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

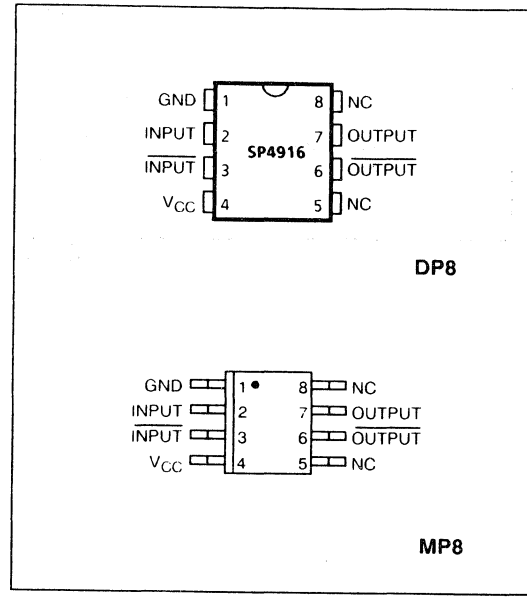


Fig 1 Pin Connections - top view

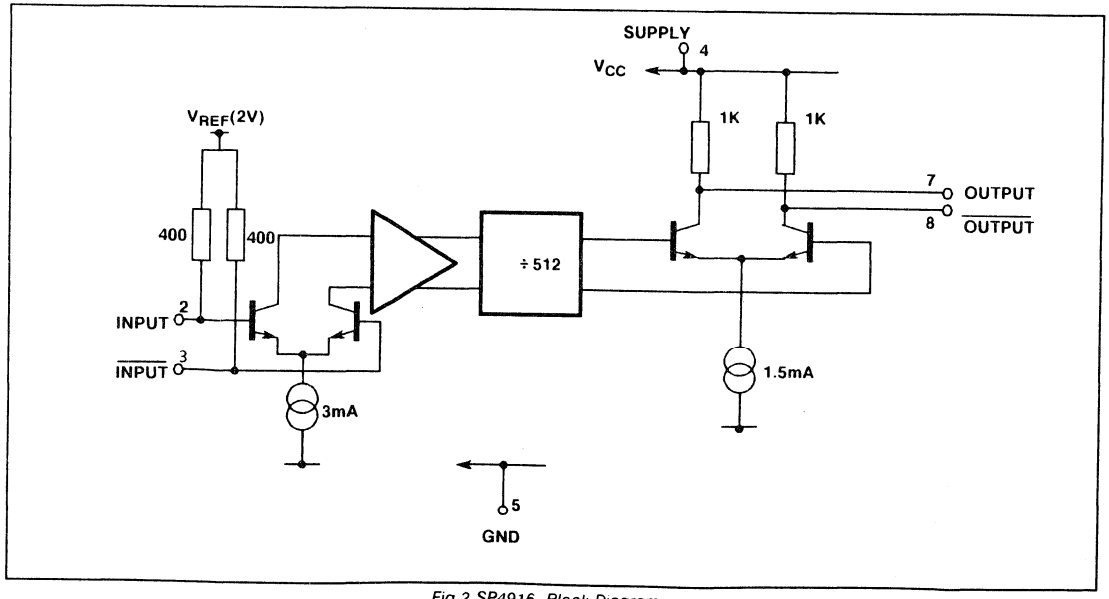


Fig 2 SP4916 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		44		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 2500MHz	6,7	1.3	1.5		Vp-p	V_{CC} = 5V No Load
Output voltage with fin = 2500MHz	6,7	1	1.3		Vp-p	V_{CC} = 5V Load as fig.4

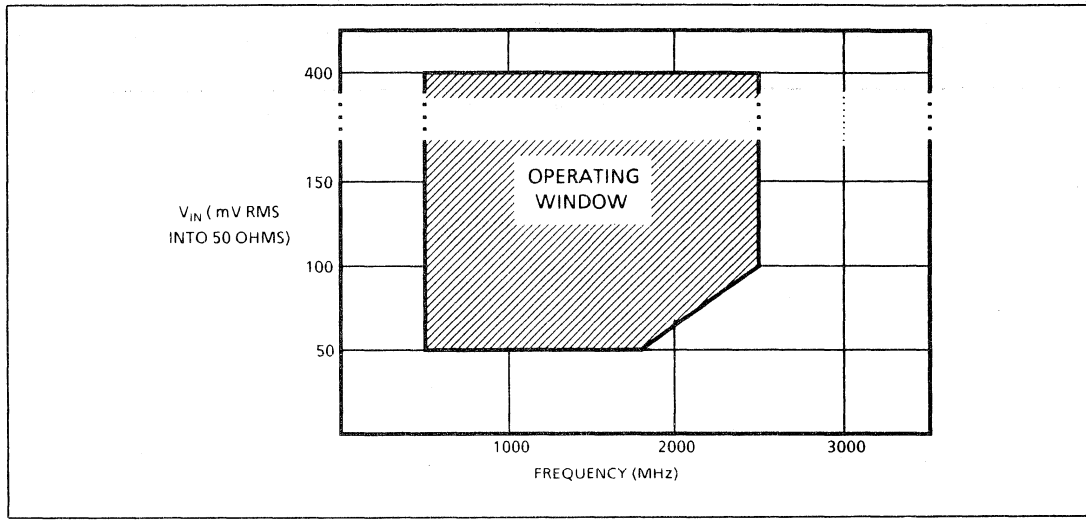


Fig.3 Typical input sensitivity

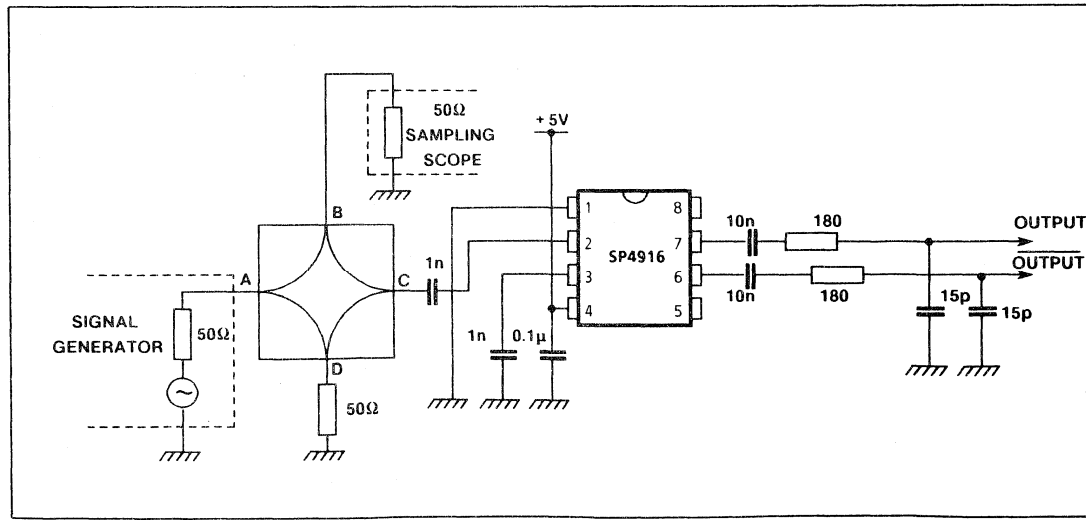


Fig.4 Test circuit

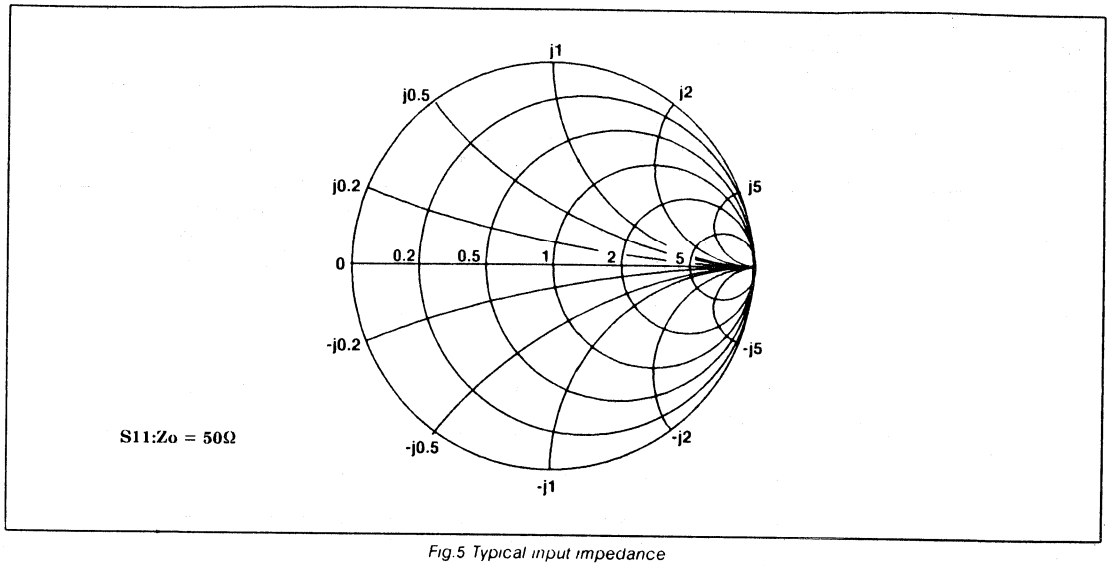


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP5000A

SINGLE CHIP FREQUENCY SYNTHESISER FOR TV TUNING

The SP5000A used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Band selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

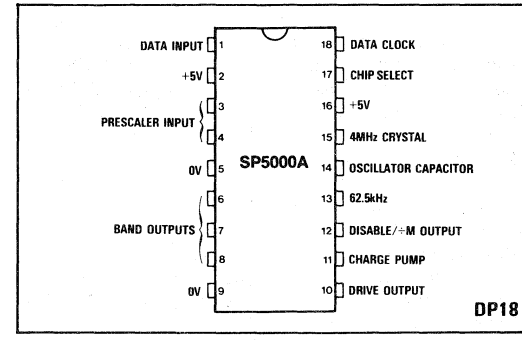


Fig.1 Pin connections - top view

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 60mA
- Prescaler and Preamplifier Included
- Single Port 16-bit Serial Data Entry
- Frequencies up to 1024MHz in 62.5kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- Frequency Band Select Outputs
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

Band select data		Band outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Band select decoding

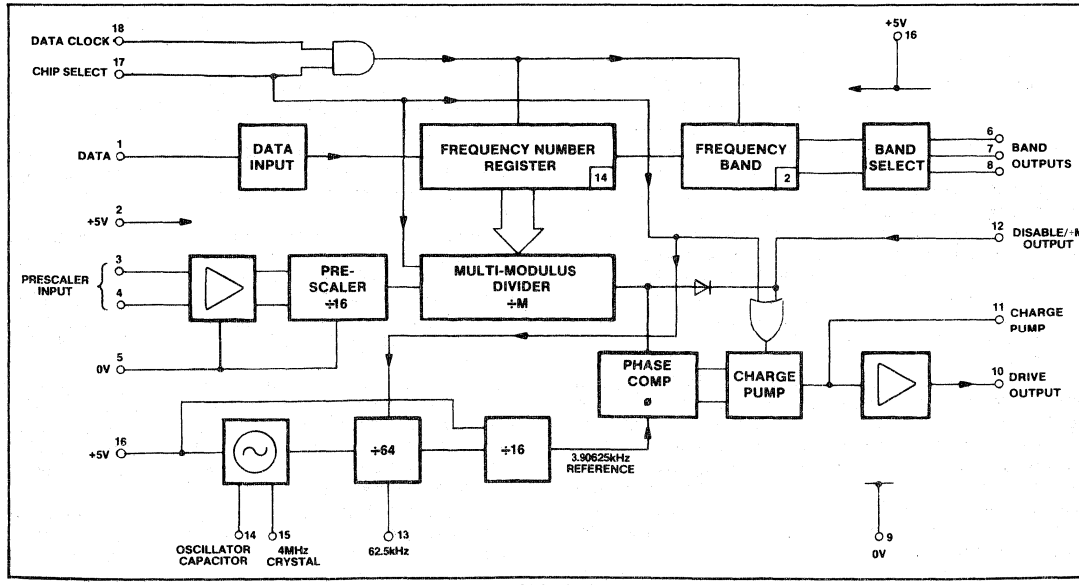


Fig.2 SP5000A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	$I_{CC}(2)$	2		50	65	mA	
Supply current	$I_{CC}(16)$	16		1		mA	
Prescaler input voltage		3,4	17.5		200	mV	80MHz to 1GHz sinewave. See Fig.4
Prescaler input impedance		3,4		50		Ω	See Fig.5
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider		12		350		mV	6.8k to 0V. Provided for test purposes only.
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/°C	Over 0 °C to 65 °C temperature range. IC variation only
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Band output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Band output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An output at 62.5kHz for driving the SP5010 in cable TV applications is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-sixteen prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. A simple filter arrangement is necessary at the inputs to prevent loading by the unused oscillator output when operation at both UHF and VHF frequencies is required.

The divide-by-sixteen prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies required for both off air and cable TV reception is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data, applied as a 16 bit serial word, is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider, and the remaining bits the band select outputs on Pins 6, 7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the tuner varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

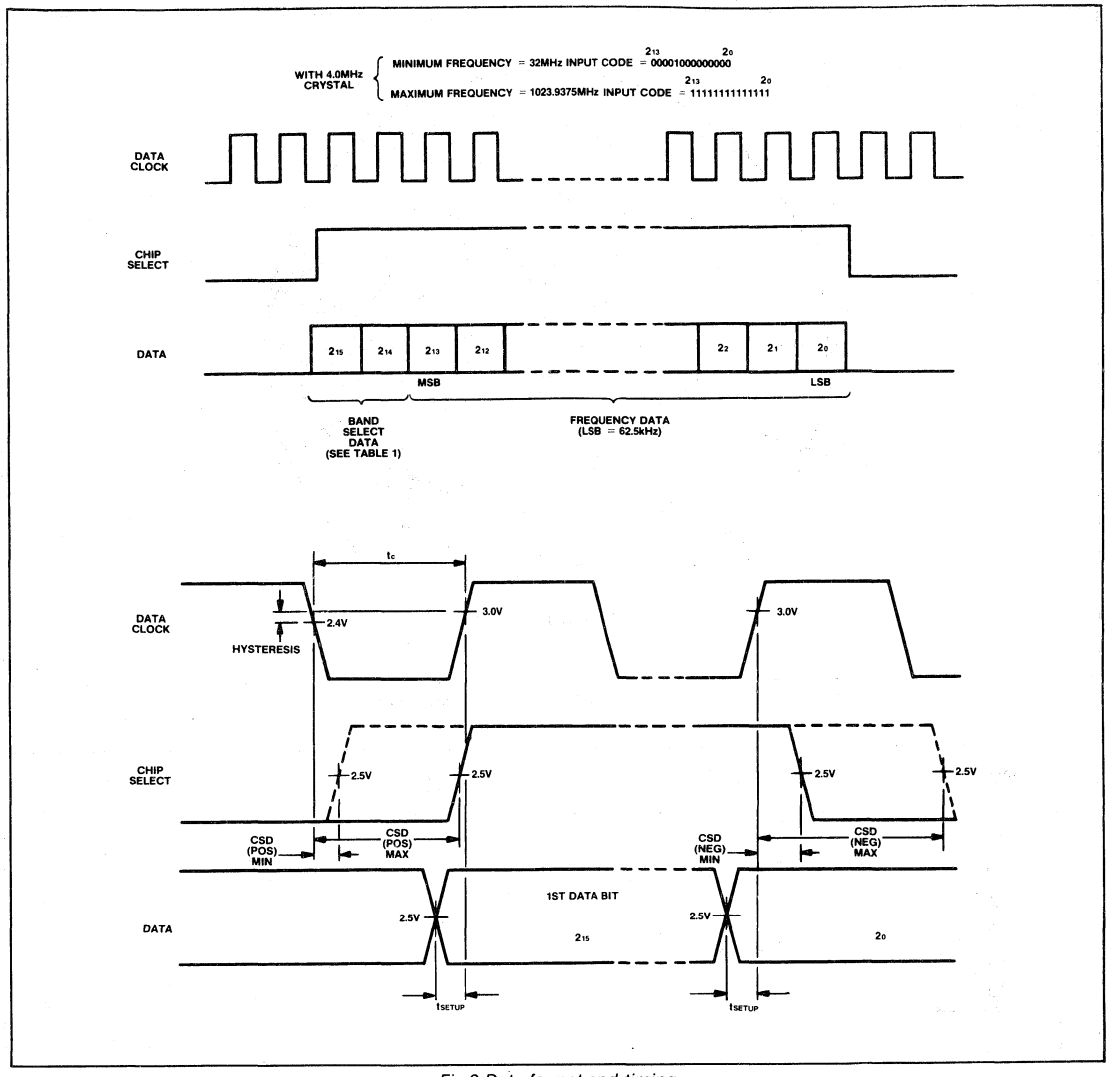


Fig.3 Data format and timing

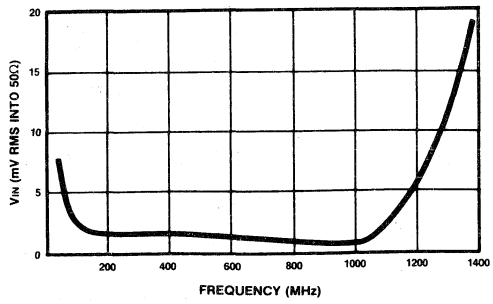


Fig.4 Typical input sensitivity of prescaler

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature: -10° C to +65° C
Storage temperature: -55° C to +125° C
Supply voltage Pin 2 and 16: 7V
Band select output voltage Pins 6,7,8: 14V
Prescaler input voltage: 2.5V p-p

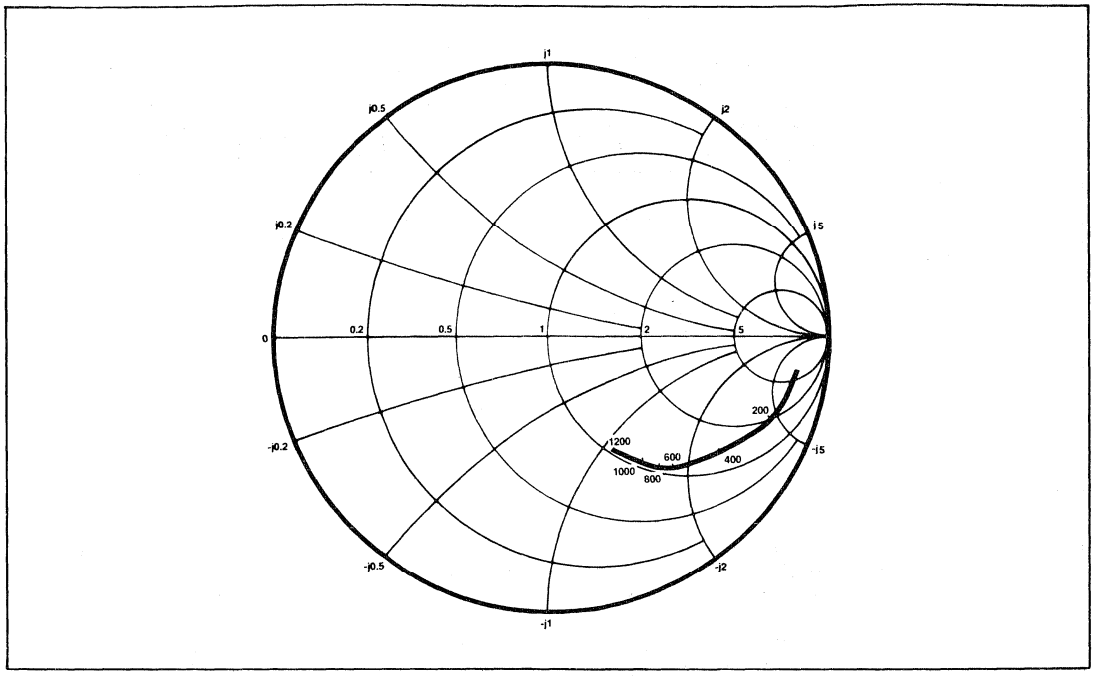


Fig.5 Typical input impedance frequencies in MHz. Normalised to 50 Ω

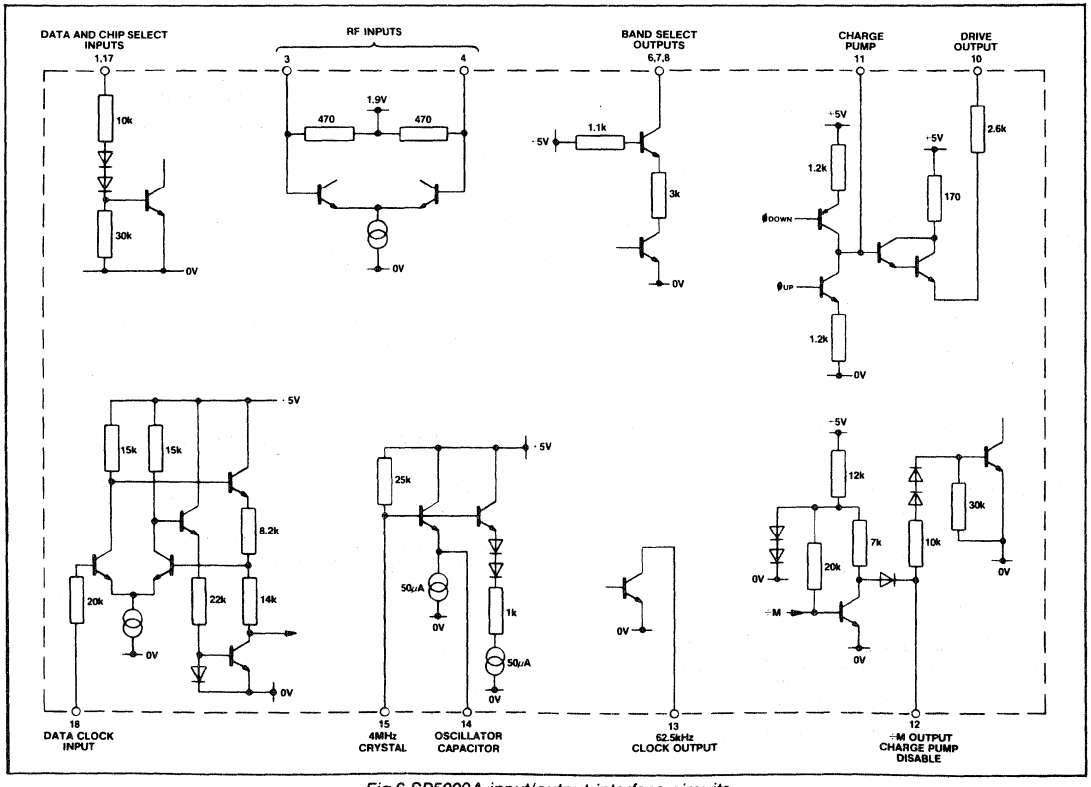


Fig.6 SP5000A input/output interface circuits

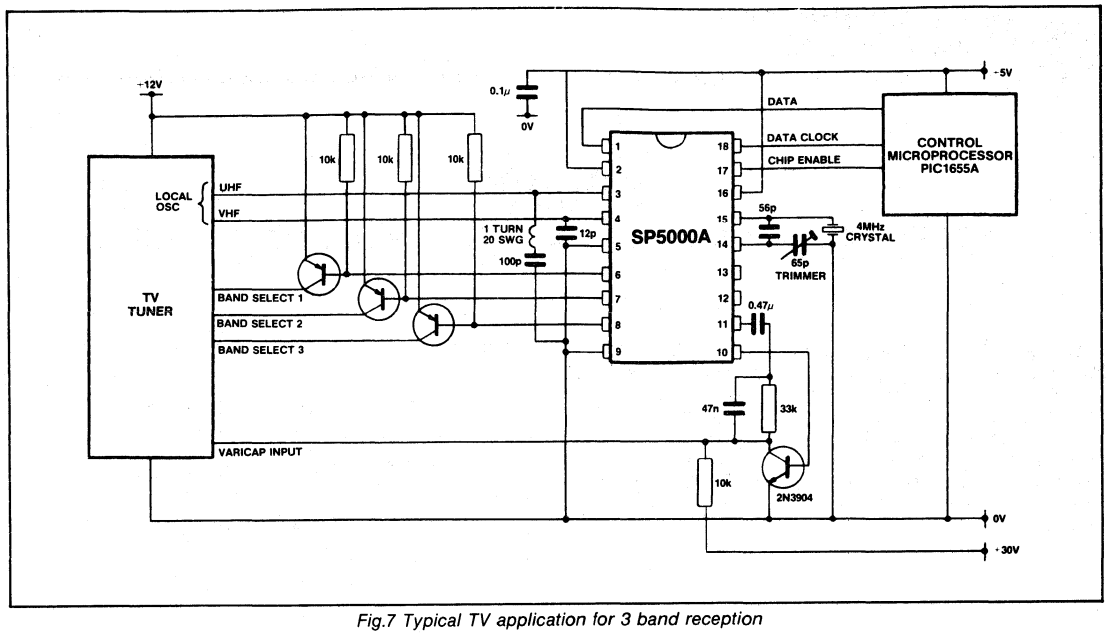


Fig.7 Typical TV application for 3 band reception

PLESSEY
Semiconductors

SP5003

1.3GHz I²C BUS CONTROLLED FREQUENCY SYNTHESISER

The SP5003 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered via the I²C bus; five eight-bit serial bytes are required to address the device, select the tuned frequency, program the five control outputs and set the charge pump current. The frequency/phase comparator operates at 7.8125kHz when a 4MHz reference crystal is used. The SP5003 requires external transistors for the varicap drive and band select outputs.

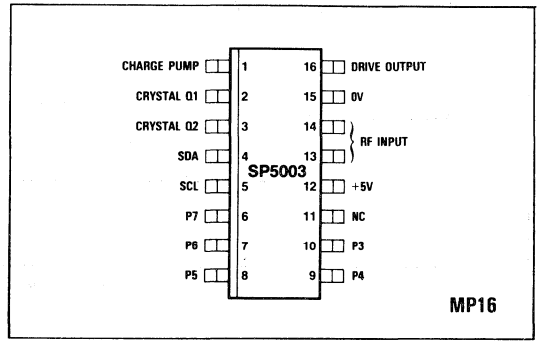


Fig.1 Pin connections - top view

FEATURES

- Complete Single Chip System
- I²C Bus Programming
- 5V 42mA Supply
- Charge Pump Current Programmable From I²C Bus
- Five Control Outputs
- 7.8125kHz Comparator Frequency with 4MHz Crystal
- 62.5kHz Minimum Step Size with 4MHz Crystal
- 1.3GHz Operating Frequency
- Non Self-Oscillating Prescaler
- Full ESD Protection

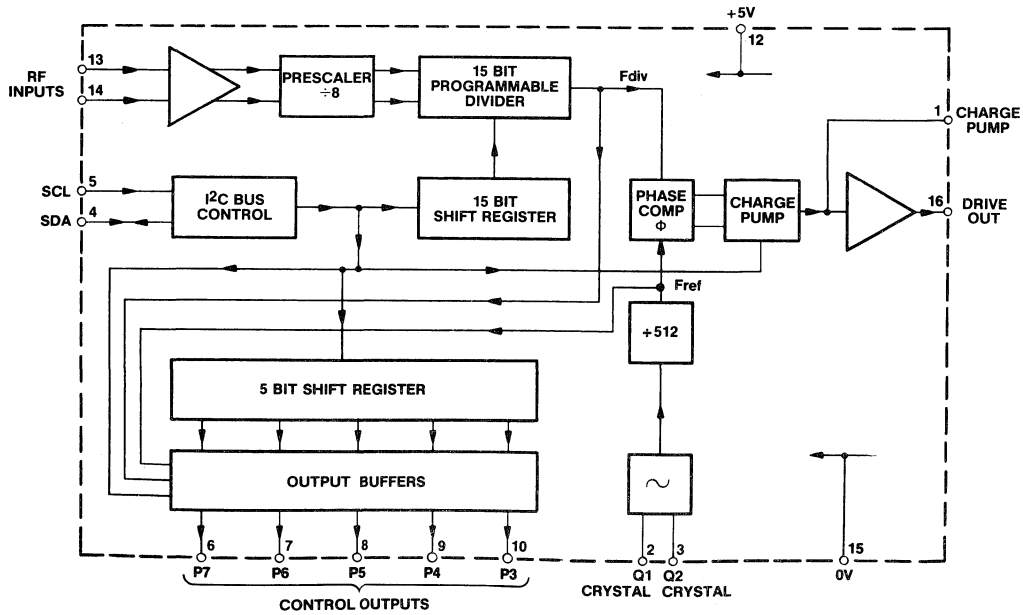


Fig.2 SP5003 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		42		mA	V_{CC} = 5V
Prescaler input voltage	12.5		300	mV	50MHz to 1GHz
Prescaler input impedance		50		Ω	
		2		pF	
Crystal frequency	2	4	8	MHz	
SDA,SCL Input high voltage	3			V	
Input low voltage			1.5	V	
Input high current			3	μA	
SDA output voltage			0.4	V	I_{sink} = 2mA
Charge pump current low		±50		μA	Byte 4 Bit 2 = 0 }
Charge pump current high		±250		μA	Byte 4 Bit 2 = 1 } V pin 1 = 2V
Charge pump output leakage			±1	μA	Byte 4 Bit 4 = 1 }
Charge pump drive output current	1			mA	V Pin 18 = 0.7V
P4 - P7 control output sink current			10	mA	
P4 - P7 control output leakage current			10	μA	V_{OUT} = 12V
P3 control output leakage current			5	μA	V_{OUT} = 12V
P3 control output sink current	1	1.3		mA	V_{OUT} = 12V on impedance = 12k

FUNCTIONAL DESCRIPTION

The SP5003 is programmed by data from a microprocessor fed via the I²C bus according to Table 1. To fully program the device, 5 bytes (each of 8 bits) are required on the SDA line together with 8 clocks on the SCL input. At the conclusion of each byte, the microprocessor must leave the SDA input high and generate an additional clock on SCL. In accordance with the I²C bus specification, the SP5003 will generate an Acknowledge signal by taking the SDA input low during the high period of the 9th clock pulse.

The I²C bus interface is designed to allow programming of frequency data using bytes 2 and 3, or charge pump and band select information using bytes 4 and 5 independently. Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or byte 4, a logic 0 indicating frequency data and a logic 1 charge pump and band information. Until an I²C Bus Stop condition is recognised, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give a high sensitivity at the local oscillator input. The amplifier is designed to be non self-oscillating, preventing a lock-up condition which can occur if the tuner local oscillator stops when varicap voltages outside the normal operating extremes are applied.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the 7.8125kHz reference obtained by dividing the output of the 4MHz crystal oscillator by 512.

Bit 2 of byte 4 of the programming data is used to control the current in the charge pump circuit, a logic '1' increasing the current from 50μA to 250μA allowing compensation for the variable tuning slope of tuners over the frequency range.

The five control outputs can be programmed from byte 5 of the input data. The current source on P3 is an output suitable for driving tuner band selection via external PNP transistors or other auxiliary functions. The outputs P4 - P7 are provided by open collector NPN transistors.

When using the standard 4MHz reference frequency, the phase comparator reference frequency is 7.8125kHz and the minimum step size 62.5kHz.

I²C BUS ADDRESS AND DATA ALLOCATION

	MSB								LSB	
ADDRESS	1	1	0	0	0	0	1	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	0	A	**BYTE 4**
CONTROL AND BAND OUTPUTS	P7	P6	P5	P4	P3	X	X	X	A	**BYTE 5**

MSB is transmitted first; A = Acknowledge bit (generated by SP5003), X = Don't Care

Table 1

The programmable divider ratio is set by bytes 2 and 3 according to the binary weighting shown in the table. An input of

0	1	0	0	1	1	0	1	A	**BYTE 2**
0	0	0	1	0	1	1	1	A	**BYTE 3**

will give a programmable divider ratio of 19735 and synthesised frequency of 1233.4375MHz with a 4MHz crystal reference.

BYTE4 CP: Sets charge pump current: logic 1 = high current.
BYTE4 T1: Selects test modes where the phase comparator inputs are available on control outputs P6 and P7. A logic 1 on T1 connects P6 to F_{ref} and P7 to F_{div}.
BYTE4 T0: A logic 1 disables the charge pump.
BYTE5 P7 - P4: A logic 1 turns on the NPN output transistors.
BYTE5 P3: A logic 1 activates the current sink.

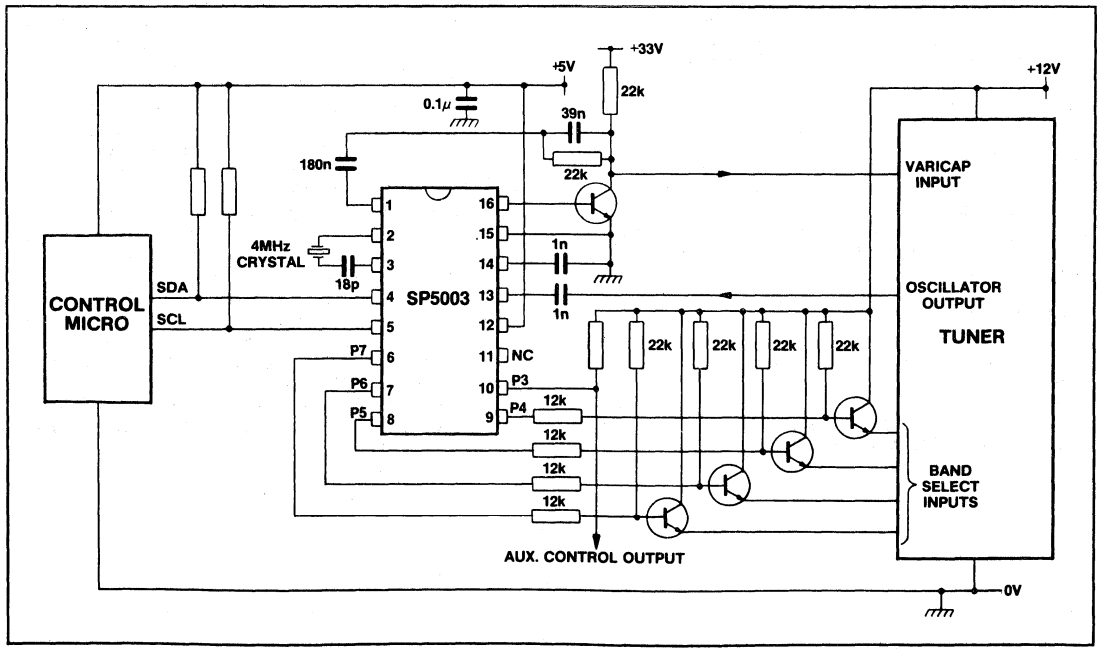


Fig.3 SP5003 typical application

PLESSEY
Semiconductors

SP5004

1.3GHz I²C BUS CONTROLLED FREQUENCY SYNTHESISER

The SP5004 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered via the I²C bus; five eight-bit serial bytes are required to address the device, select the tuned frequency, program the four band select and four auxiliary outputs and set the charge pump current. The frequency/phase comparator operates at 7.8125kHz when a 4MHz reference crystal is used. The SP5004 requires external transistors for the varicap drive and band select outputs.

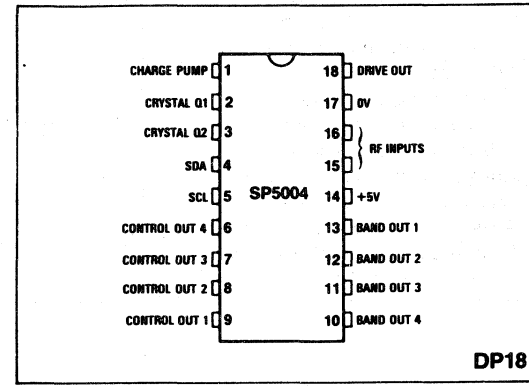


Fig.1 Pin connections - top view

FEATURES

- Complete Single Chip System
- I²C Bus Programming
- 5V 42mA Supply
- Charge Pump Current Programmable From I²C Bus
- Four Band Select Outputs
- Four Auxiliary Control Outputs
- 7.8125kHz Comparator Frequency with 4MHz Crystal
- 62.5kHz Minimum Step Size with 4MHz Crystal
- 1.3GHz Operating Frequency
- Non Self-Oscillating Prescaler
- Full ESD Protection

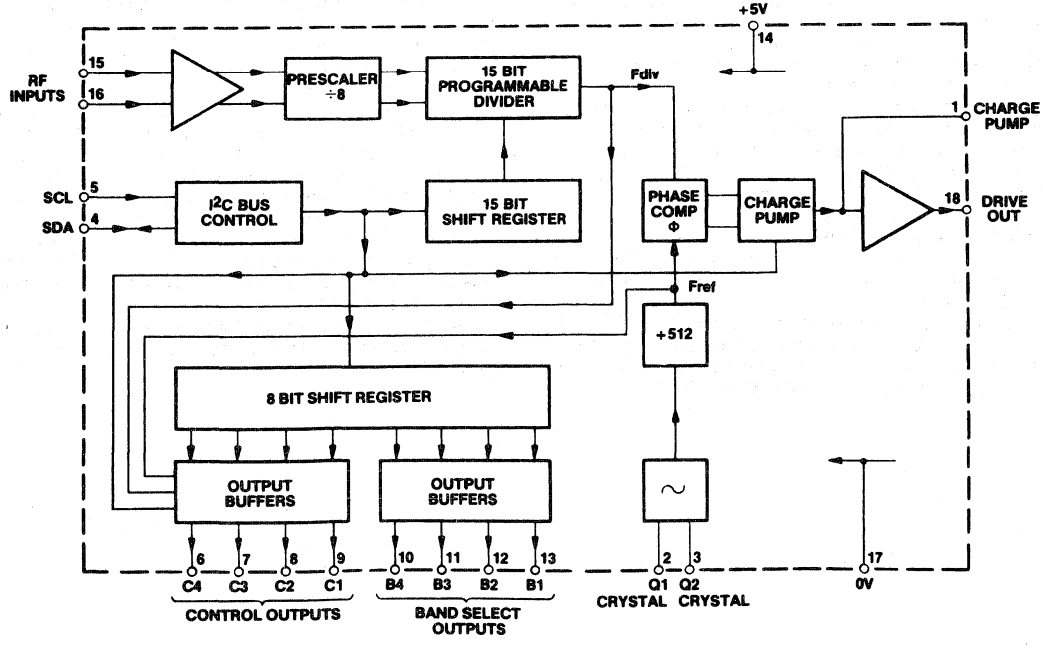


Fig.2 SP5004 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		42		mA	V_{CC} = 5V
Prescaler input voltage	12.5		300	mV	50MHz to 1GHz
Prescaler input impedance		50		Ω	
		2		pF	
Crystal frequency	2	4	8	MHz	
SDA,SCL Input high voltage	3			V	
Input low voltage			1.5	V	
Input high current			3	μA	
SDA output voltage			0.4	V	I_{sink} = 2mA
Charge pump current low		±50		μA	Byte 4 Bit 2 = 0 }
Charge pump current high		±250		μA	Byte 4 Bit 2 = 1 } V pin 1 = 2V
Charge pump output leakage			±1	μA	Byte 4 Bit 4 = 1 }
Charge pump drive output current	1			mA	V Pin 18 = 0.7V
Auxiliary control output sink current			10	mA	
Auxiliary control output leakage current			10	μA	V_{OUT} = 12V
Band select output leakage current			5	μA	V_{OUT} = 12V
Band select output sink current	1	1.3		mA	V_{OUT} = 12V on impedance = 12k

FUNCTIONAL DESCRIPTION

The SP5004 is programmed by data from a microprocessor fed via the I²C bus according to Table 1. To fully program the device, 5 bytes (each of 8 bits) are required on the SDA line together with 8 clocks on the SCL input. At the conclusion of each byte, the microprocessor must leave the SDA input high and generate an additional clock on SCL. In accordance with the I²C bus specification, the SP5004 will generate an Acknowledge signal by taking the SDA input low during the high period of the 9th clock pulse.

The I²C bus interface is designed to allow programming of frequency data using bytes 2 and 3, or charge pump and band select information using bytes 4 and 5 independently. Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or byte 4, a logic 0 indicating frequency data and a logic 1 charge pump and band information. Until an I²C Bus Stop condition is recognised, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give a high sensitivity at the local oscillator input. The amplifier is designed to be non self-oscillating, preventing a lock-up condition which can occur if the tuner local oscillator stops when varicap voltages outside the normal operating extremes are applied.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the 7.8125kHz reference obtained by dividing the output of the 4MHz crystal oscillator by 512.

Bit 2 of byte 4 of the programming data is used to control the current in the charge pump circuit, a logic '1' increasing the current from 50μA to 250μA allowing compensation for the variable tuning slope of tuners over the frequency range.

Four band select and four general purpose control outputs can be programmed from byte 5 of the input data. The current sources on the band select outputs are suitable for driving tuner band selection via external PNP transistors. The auxiliary control outputs are provided by open collector NPN transistors.

When using the standard 4MHz reference frequency, the phase comparator reference frequency is 7.8125kHz and the minimum step size 62.5kHz.

I²C BUS ADDRESS AND DATA ALLOCATION

	MSB								LSB	
ADDRESS	1	1	0	0	0	0	1	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	0	A	**BYTE 4**
CONTROL AND BAND OUTPUTS	C4	C3	C2	C1	B4	B3	B2	B1	A	**BYTE 5**

MSB is transmitted first; A = Acknowledge bit (generated by SP5004).

Table 1

The programmable divider ratio is set by bytes 2 and 3 according to the binary weighting shown in the table. An input of

0	1	0	0	1	1	0	1	A	**BYTE 2**
0	0	0	1	0	1	1	1	A	**BYTE 3**

will give a programmable divider ratio of 19735 and synthesised frequency of 1233.4375MHz with a 4MHz crystal reference.

BYTE4 CP: Sets charge pump current: logic 1 = high current.
BYTE4 T1: Selects test modes where the phase comparator inputs are available on control outputs 3 and 4. A logic 1 on T1 connects C4 to F_{ref} and C3 to F_{div}.
BYTE4 T0: A logic 1 disables the charge pump.
BYTE5 C4 - C1: A logic 1 turns on the NPN output transistors.
BYTE5 B4 - B1: A logic 1 activates the current sink.

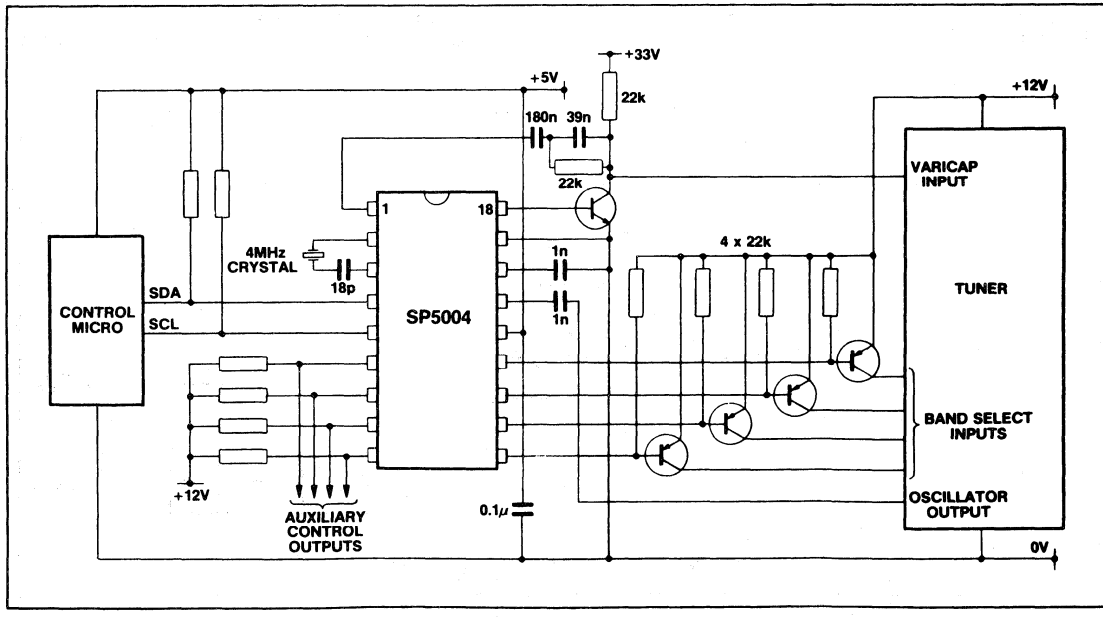


Fig.3 SP5004 typical application

PLESSEY
Semiconductors

SP5011 AND SP5012

CABLE TV PLL CONVERTERS

The SP5011/2 together with an appropriate voltage controlled oscillator (VCO), form a complete phase locked loop (PLL) synthesiser with 8-channel frequency selection. They consist of a prescaler with preamplifier and a divider programmable by means of link options on 3 pins. The frequency standard is derived from a 4MHz crystal controlled oscillator on-chip. A frequency/phase comparator working at 3.90625kHz feeds a charge pump output with an output amplifier stage around which a feedback filter may be applied.

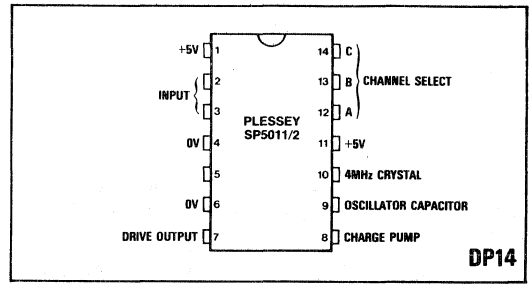


Fig.1 Pin connections - top view

FEATURES

- Complete 8-Channel System with Control
- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- Frequencies Selected by Wire Links
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- 4MHz Crystal

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10° C to +65° C
Storage Temperature	-55° C to +125° C
Supply Voltage Pin 1 and Pin 12	7V
Prescaler Input Voltage	2.5V p-p

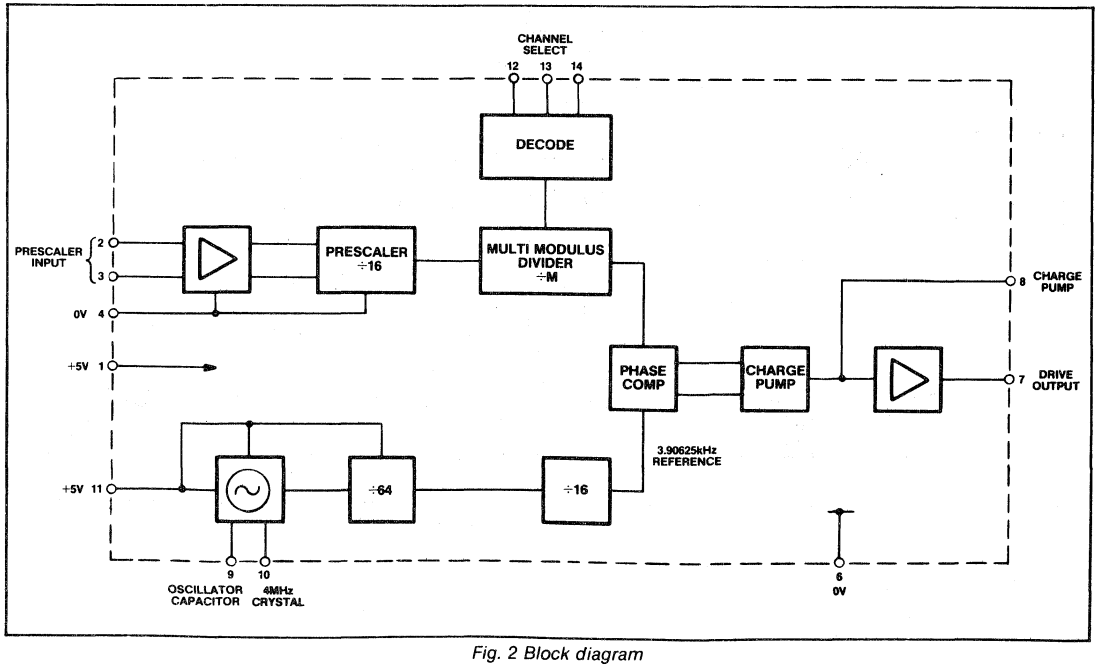


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
T_{amb} = +25° C; V_{CC} = +5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	1,11	4.5		5.5	V	
Supply current	I_{CC} (1)	1		50	60	mA	
Supply current	I_{CC} (11)	11		1		mA	
Prescaler input voltage		2,3	17.5		200	mV	RMS into 50Ω SP5011
Prescaler input voltage		2,3	10		200	mV	RMS into 50Ω SP5012
Prescaler input impedance		2,3		50		Ohms	
High level input voltage		12,13,14	3.5V		V_{CC}	V	
Low level input voltage		12,13,14	0		1.5	V	
High level input current		12,13,14			0.4	mA	V_{in} = 5V
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/° C	Over 0 to 65° C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	V_{CC} = 4.5V to 5.5V

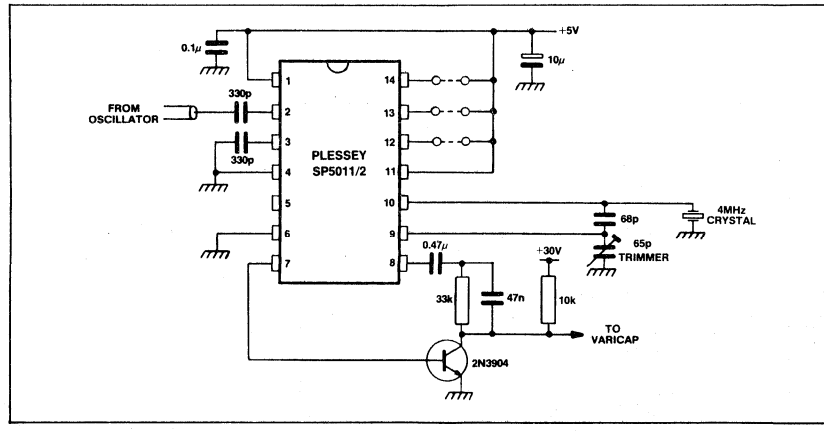


Fig.3 Typical application and test circuit

DESCRIPTION

The SP5011/2 when used with a voltage controlled oscillator form complete phase locked loop frequency synthesisers. Eight possible output frequencies are selectable by three wire links on each device. The SP5011 is intended to synthesise the 2nd LO frequency in American cable TV convertors using an IF frequency of 612.75MHz. The SP5012 will synthesise the vision carrier frequencies for European UHF channels as shown in Table 1.

A phase comparator reference frequency of 3.90625kHz is obtained by division of a 4MHz reference frequency which may be generated on chip or applied externally from the SP5000 reference oscillator where this is used.

In order to achieve a high sensitivity at the local oscillator pick off point the divide by sixteen prescaler is preceded by a differential amplifier with inputs on pins 2 and 3. The prescaler output is further divided by the multi-modulus divider, producing an output which is phase locked to the 3.90625kHz reference.

By changing the code on the channel select inputs on pins 12, 13 and 14 the division ratio of the multi-modulus divider can be changed to allow synthesis of eight local oscillator frequencies.

A single external transistor driven from the charge pump output provides the output swing necessary for the local oscillator varicap control line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all supply pins for the device to operate.

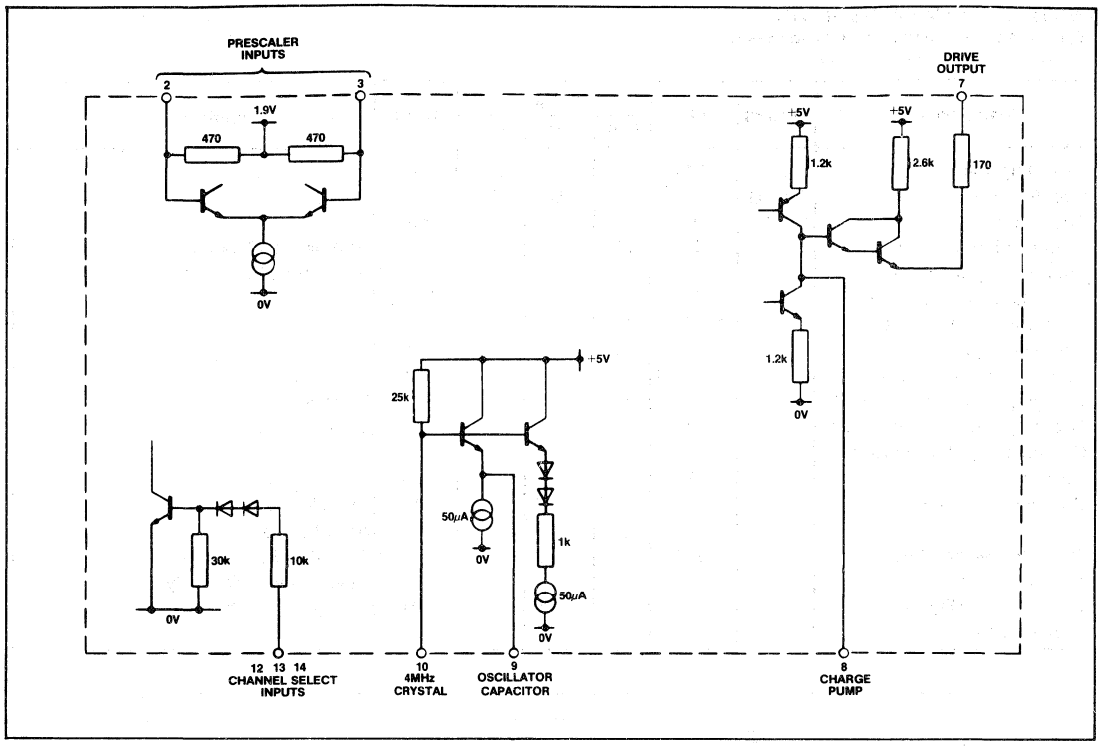


Fig.4 SP5011/2 input/output interface circuits

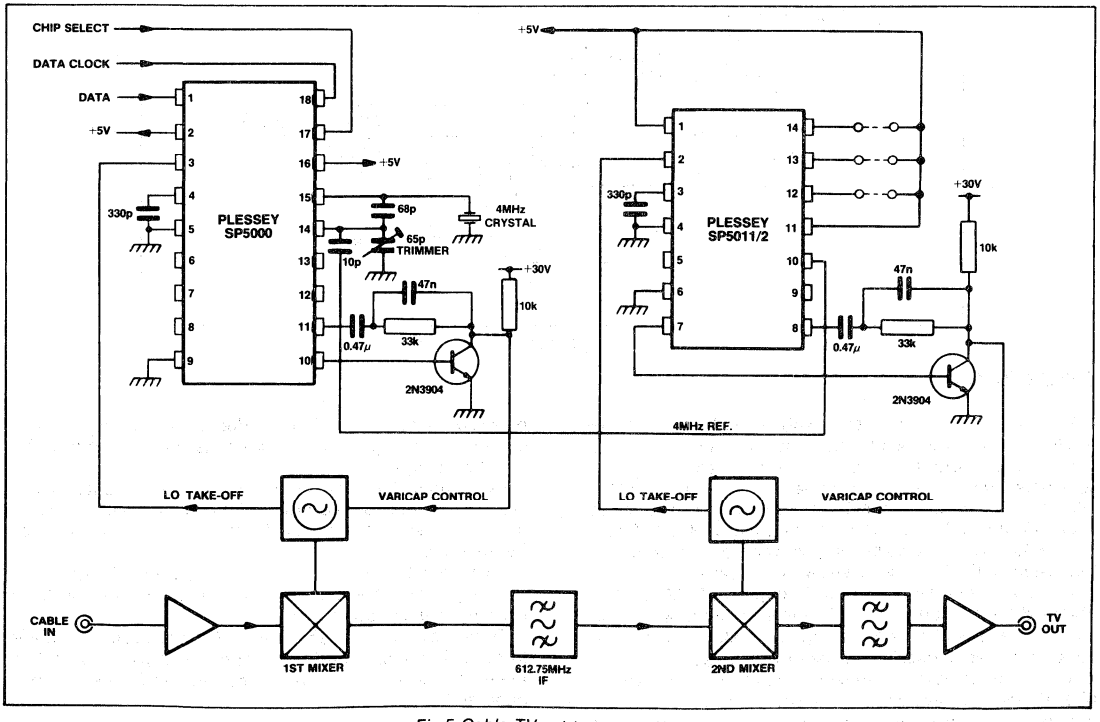


Fig.5 Cable TV set top converter

A Pin 12	B Pin 13	C Pin 14	SP5011 (2nd IF frequency = 612.75MHz)			SP5012	
			USA channel	Synthesised frequency	Mixer output frequency	European UHF channel	Vision carrier frequency
0	0	0	5	690MHz	77.25MHz	24	495.25MHz
0	0	1	6	696MHz	83.25MHz	25	503.25MHz
0	1	0	3 vision carrier	61.25MHz	-	32	559.25MHz
0	1	1	4 vision carrier	67.25MHz	-	33	567.25MHz
1	0	0	3	674MHz	61.25MHz	34	575.25MHz
1	0	1	2	668MHz	55.25MHz	35	583.25MHz
1	1	0	4	680MHz	67.25MHz	36	591.25MHz
1	1	1	TV IF	567MHz	45.75MHz	37	599.25MHz

Table 1 Channel selection coding for SP5011 and SP5012

PLESSEY
Semiconductors

SP5050/1

1.8/2GHz SINGLE CHIP FREQUENCY SYNTHESISER

The SP5050/1, used with a voltage controlled oscillator, forms a complete phase locked loop system. The circuit consists of a divide-by-32 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Control selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4 MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

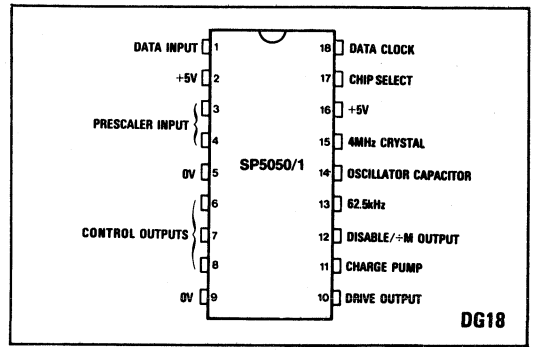


Fig.1 Pin connections - top view

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 90mA/70mA
- Prescaler and Preamplifier Included
- Single Port 16-Bit Serial Data Entry
- Frequencies up to 2048MHz in 125kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- 3 Selectable Control Outputs Are Available
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

Control select data		Control outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Control select decoding

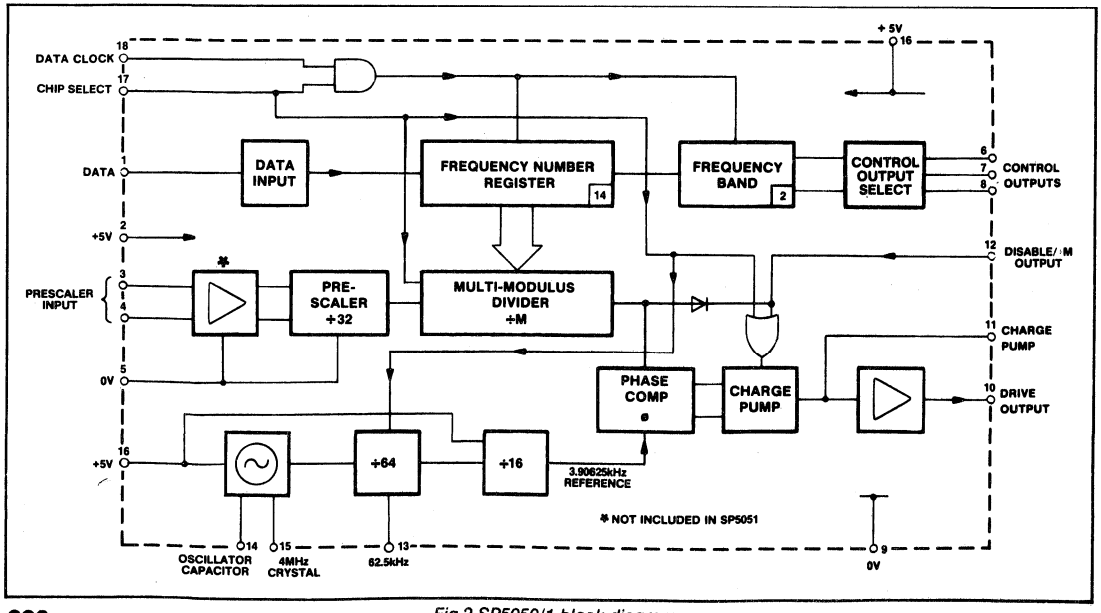


Fig.2 SP5050/1 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	I_{CC}	2		85		mA	SP5051
Supply current	I_{CC}	2		70		mA	SP5050
Prescaler input voltage		3,4		50		mV	300MHz to 1.8GHz sinewave - SP5050
		3,4	100			mV	See Fig.4,5 - SP5051
Prescaler input impedance		3,4	50			Ω	See Fig.6
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider output swing		12		350		mV	6.8k to 0V. Provided for test purposes only
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/°C	Over 0°C to 65°C temperature range. IC variation only.
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Control output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Control output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An outpt at 62.5kHz is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-32 prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. The SP5051 does not contain this preamp as it limits the frequency range. But as a consequence the SP5051 is not as sensitive as the SP5050 in the lower frequency region.

The divide-by-32 prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies from 64 MHz to 2048MHz is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data,applied as a 16-bit serial word,is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider,while the remaining bits determine the control outputs on Pins 6,7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the oscillator varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

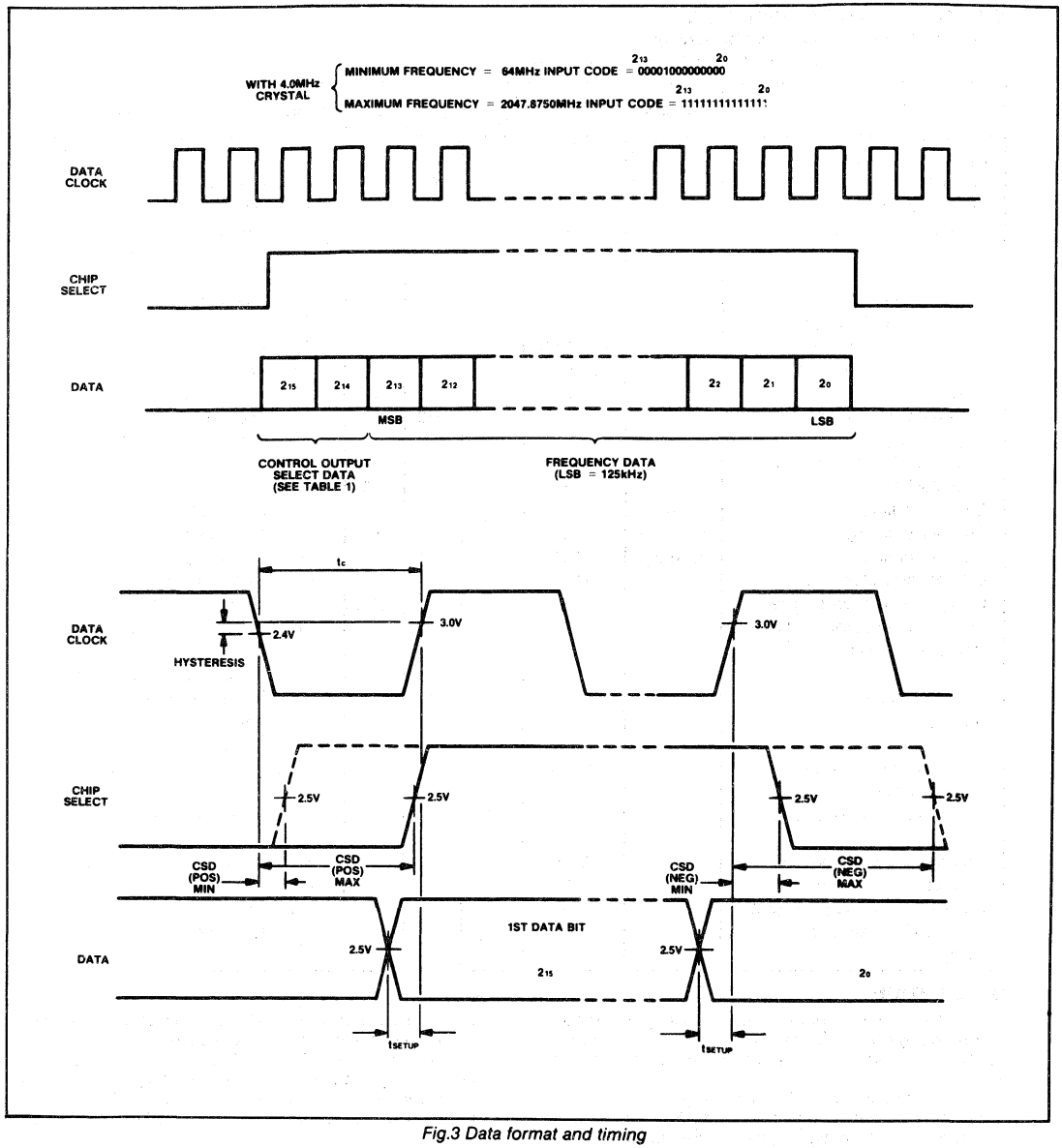


Fig.3 Data format and timing

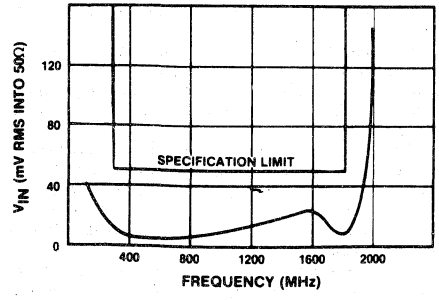


Fig.4 SP5050 typical input sensitivity

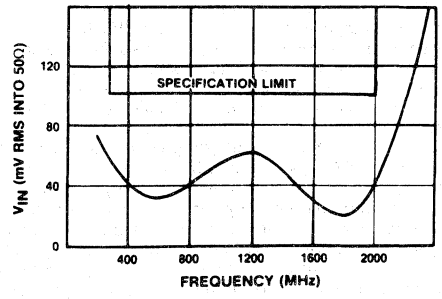


Fig.5 SP5051 typical input sensitivity

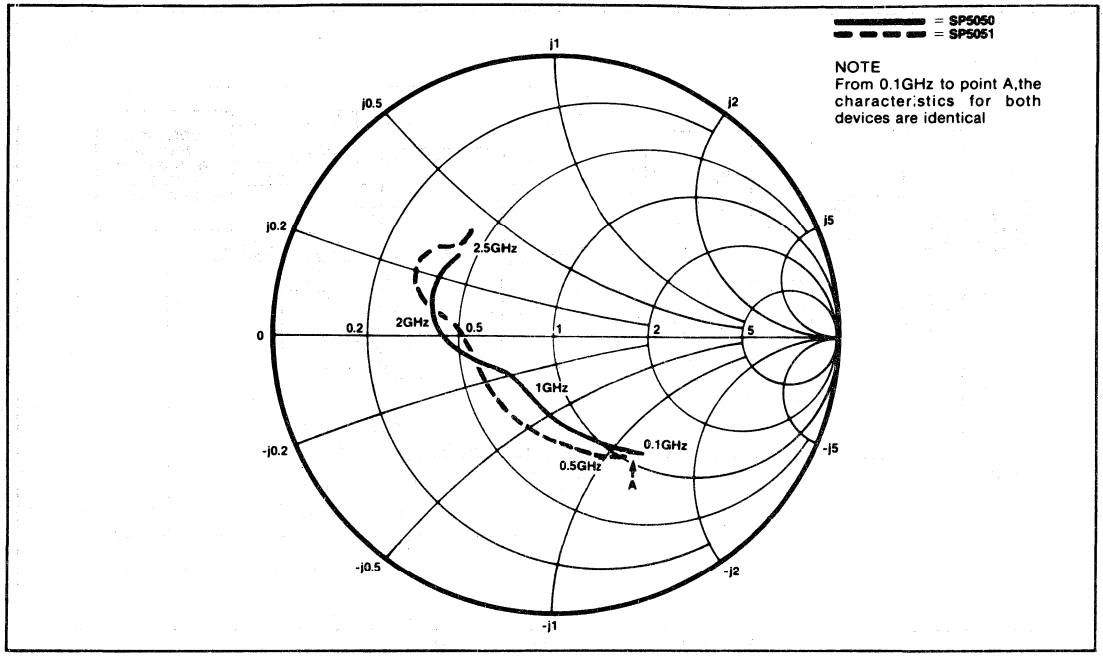


Fig.6 Typical input impedance frequencies in MHz. Normalised to 50Ω

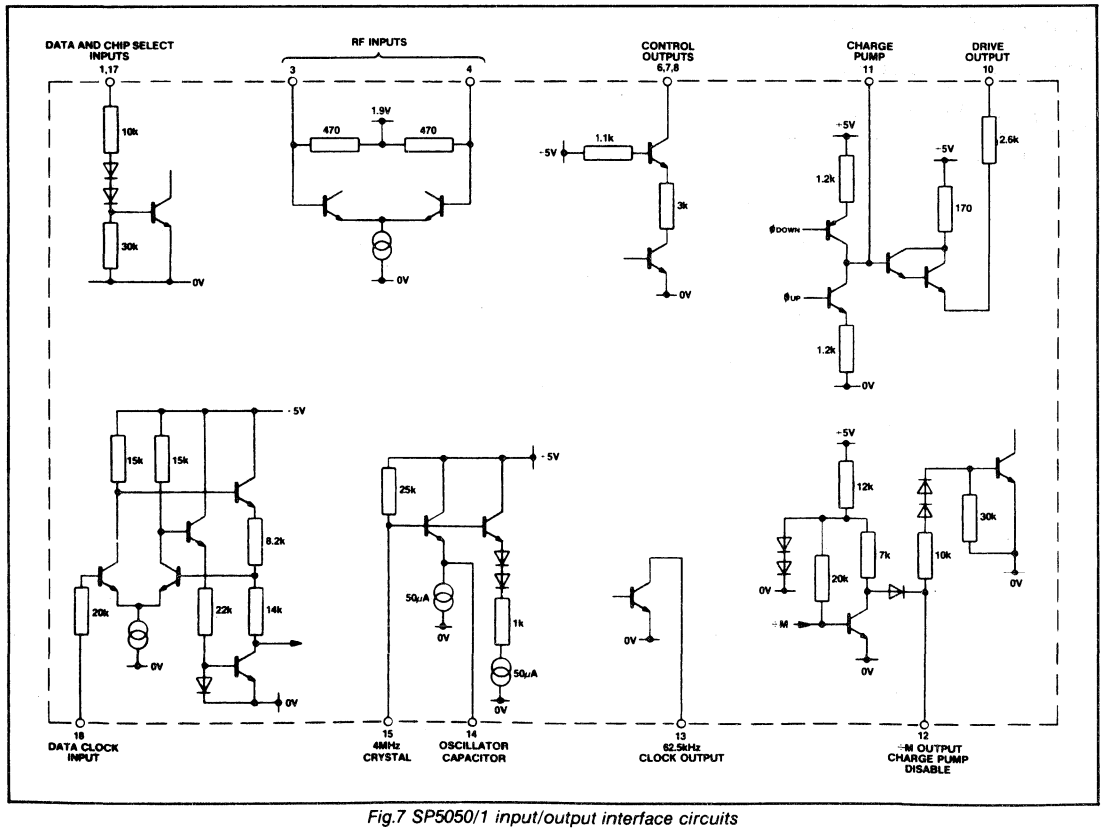


Fig.7 SP5050/1 input/output interface circuits

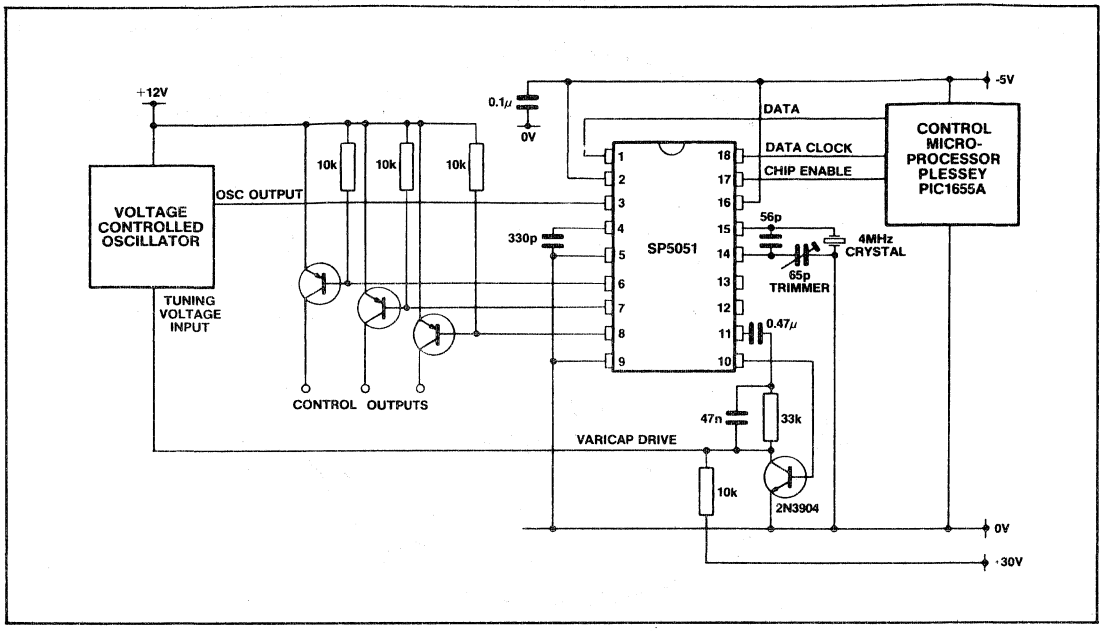


Fig.8 Application for controlling a 2GHz oscillator

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-55° C to +125° C
Supply voltage Pin 2 and 16	7V
Band select output voltage Pins 6,7,8	14V
Prescaler input voltage	2.5V p-p

PLESSEY
Semiconductors

SP5052

2.3GHz SINGLE CHIP FREQUENCY SYNTHESISER

The SP5052, used with a voltage controlled oscillator forms a complete phase locked loop capable of synthesising up to 2.3GHz. This enables the device to be incorporated in a satellite receiver designed to tune to input signals of between 0.95GHz and 1.75GHz by using a high side local oscillator to produce an IF of 480MHz. Frequency information is programmed into the device using 14 bits from a 16 bit serial data word. The remaining 2 bits set the control line outputs which may be used to switch sound sub-carrier frequencies or the dish polarisation.

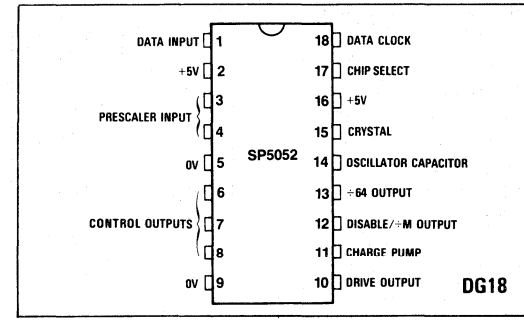


Fig.1 Pin connections (top view)

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 85mA
- Prescaler Included
- Single Port 16-Bit Serial Data Entry
- Frequencies up to 2.3GHz
- High Comparator Frequency Simplifies Charge Pump Filter
- 3 Selectable Control Outputs Are Available
- Charge Pump Amplifier with Feedback and Disable

Control select data		Control outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

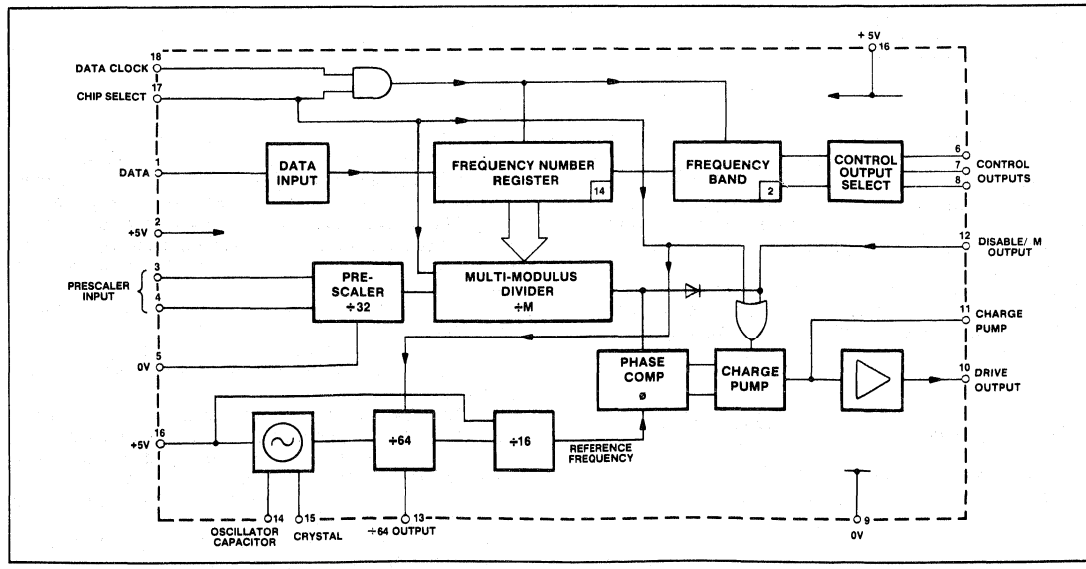


Fig.2 SP5052 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	I_{CC}	2		85		mA	SP5051
Prescaler input voltage		3,4				mV	See Fig.4
Prescaler input impedance		3,4		50		Ω	See Fig.6
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider output swing		12		350		mV	6.8k to 0V. Provided for test purposes only
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/° C	Over 0° C to 65° C temperature range. IC variation only.
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Control output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Control output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The synthesiser consists of a ÷32 prescaler followed by a 14 bit programmable divider, the resultant frequency is compared in phase with a set reference frequency. The reference frequency is generated by dividing the output of a crystal oscillator by 1024. The output from the phase detector takes the form of a charge pump, Pin 11, and an output drive, Pin 10, which with the aid of one external transistor can control the voltage controlled oscillator, (see Fig.7). This forms a complete phase locked loop system in which the frequency is determined by the data programmed into the divider.

$$\text{Synthesised frequency} = \frac{\text{crystal frequency x M}}{32}$$

M is any integer in the range 512 to 16383.

$$\text{Minimum step size} = \frac{\text{crystal frequency}}{32}$$

=change in synthesised frequency for a change of 1 bit of data programmed into the divider.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Fig.3 and Table 1 show the data format and timing requirements.

When the data is being entered the charge pump is disabled to prevent unwanted frequency variation of the oscillator.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

Fig.4 shows the input level operating window versus frequency, the oscillator coupling circuit should be designed to produce an output within these boundries over the full frequency range required for the synthesiser.

Example of crystal choice:

For a synthesiser that will synthesise from 1.5GHz to 2.3GHz in 200kHz steps a 6.4MHz crystal can be used -

M data for 1.5GHz = 7500
M data for 2.3GHz = 1500

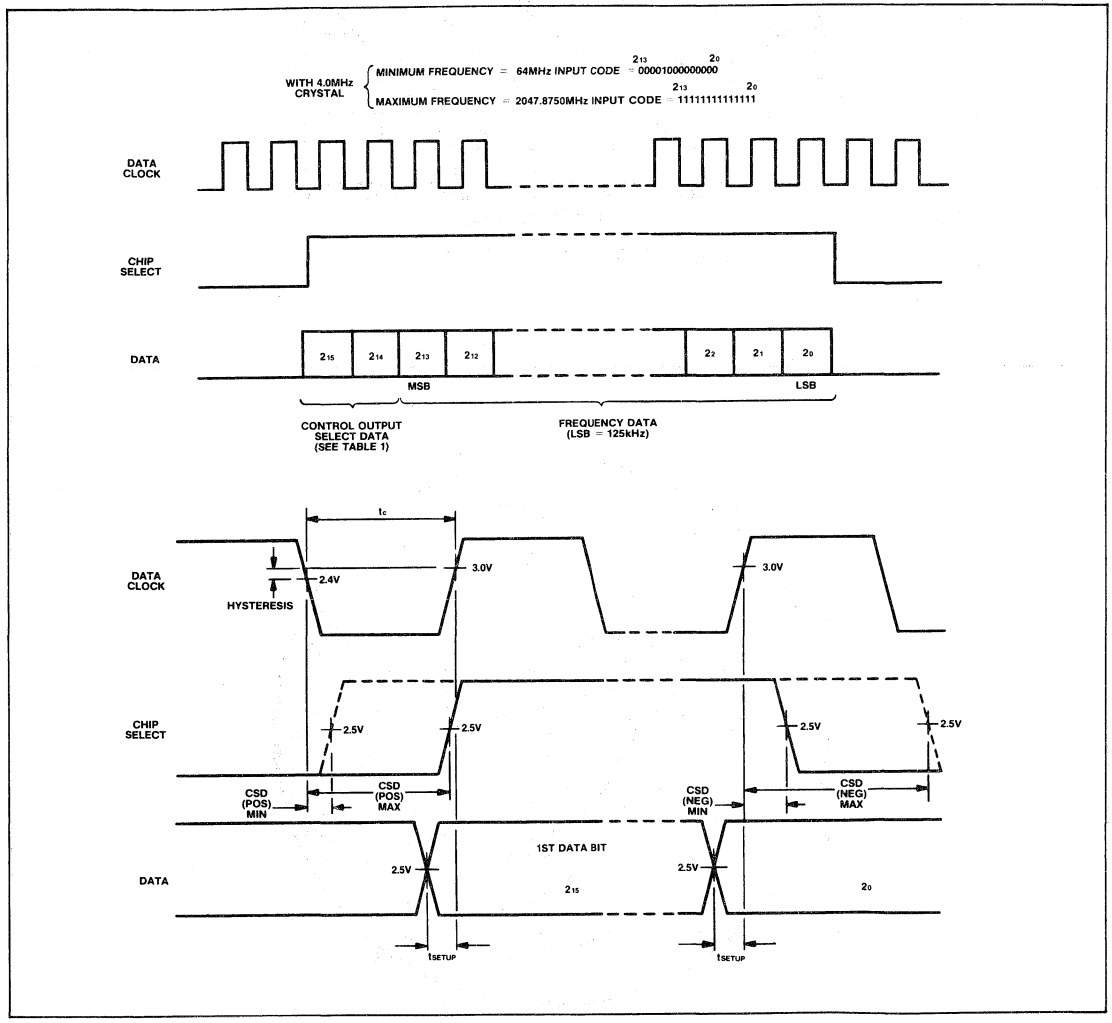


Fig.3 Data format and timing

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-55° C to +125° C
Supply voltage Pin 2 and 16	7V
Band select output voltage Pins 6,7,8	14V
Prescaler input voltage	2.5V p-p

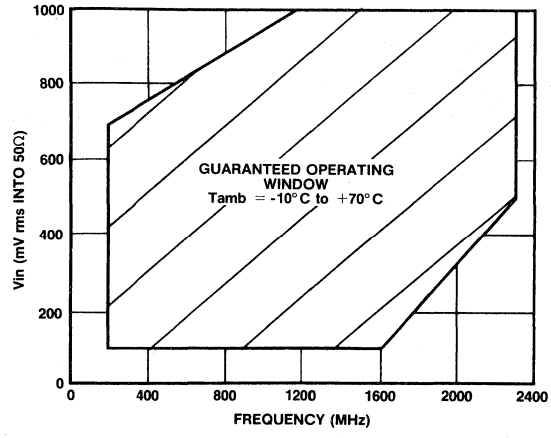


Fig.4 SP5052 typical input sensitivity

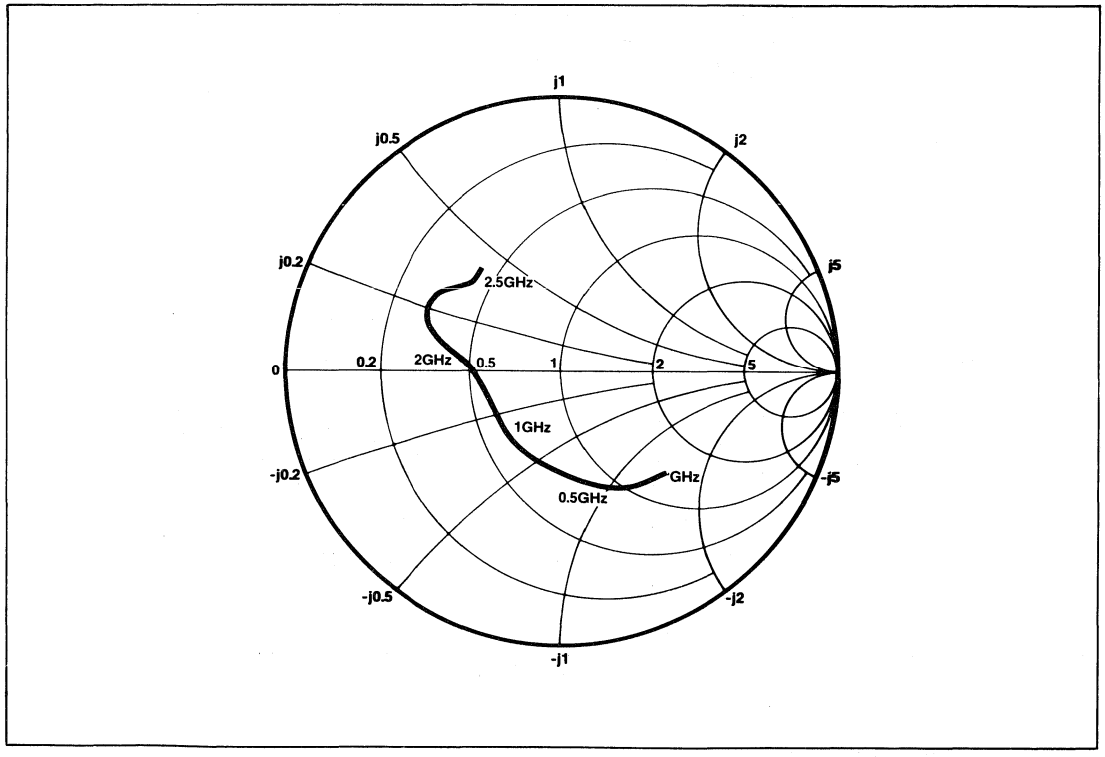


Fig.5 Typical input impedance frequencies in MHz. Normalised to 50Ω

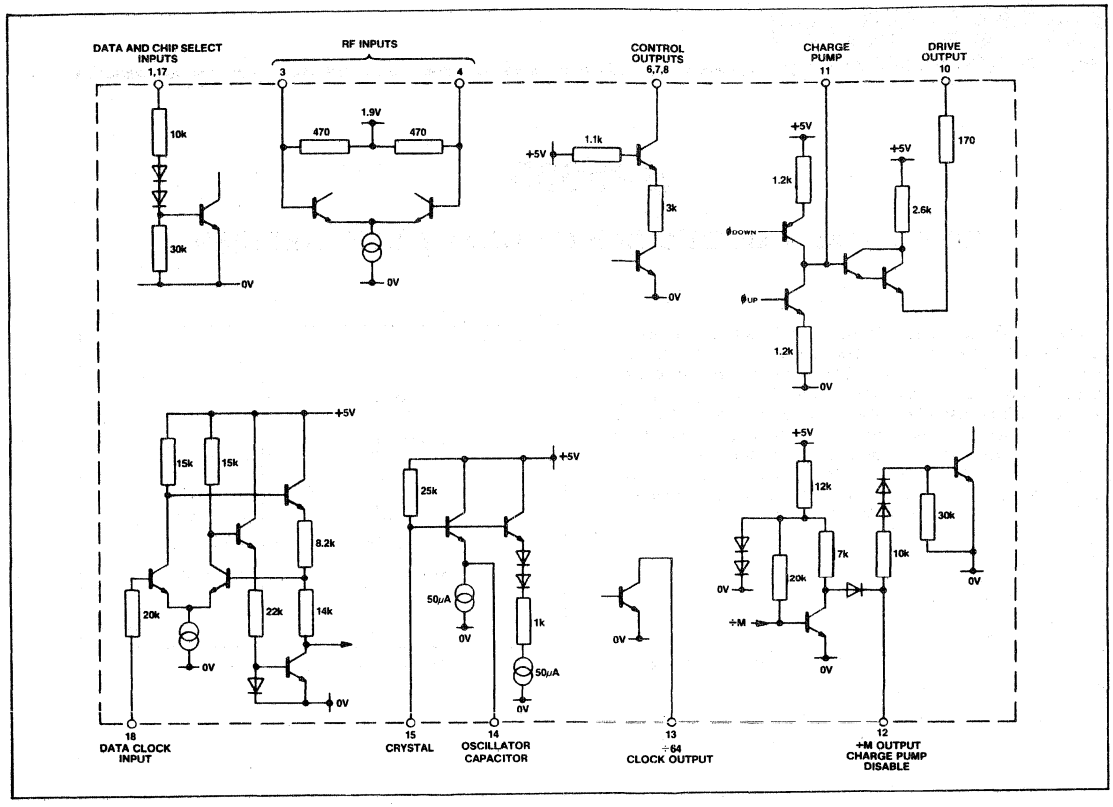


Fig.6 SP5052 input/output interface circuits

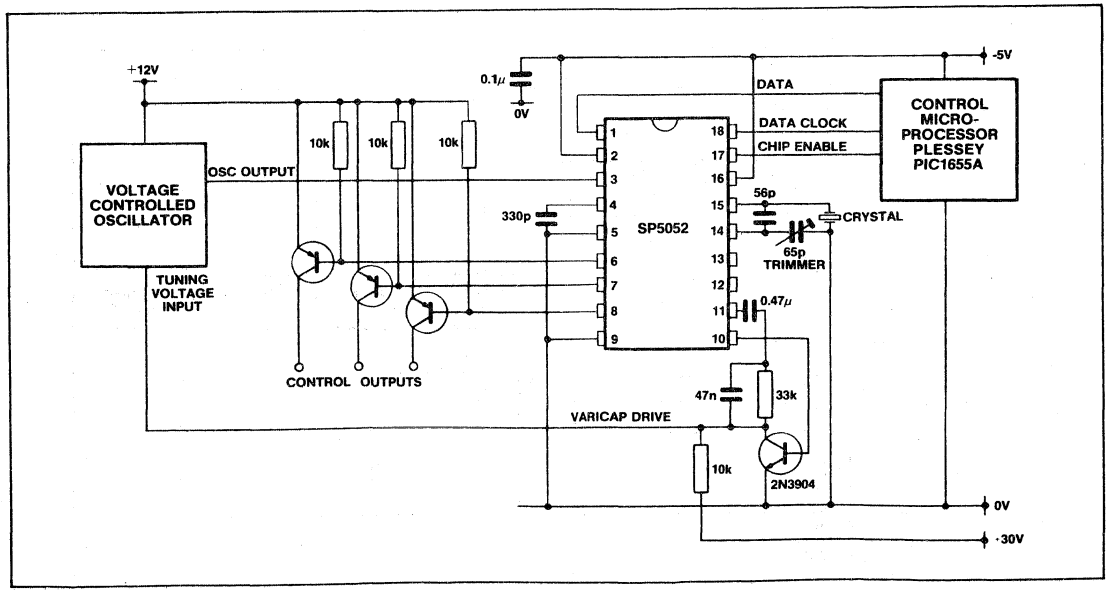


Fig.7 Application for controlling a 2.3GHz synthesiser

SP5060

2.0GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5060 is for use in outdoor (head end) units of satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

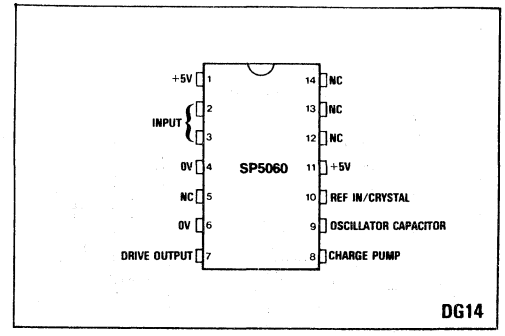


Fig.1 Pin connections - top view

FEATURES

- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- Synthesises Frequencies up to 2.0GHz
- For use at C-Band with Frequency Doubling Mixer

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +70°C**
Maximum junction temperature	175°C
Storage temperature	-55°C to +125°C
Supply voltage Pin 1 and Pin 11	7V
Prescaler input voltage	2.5V p-p

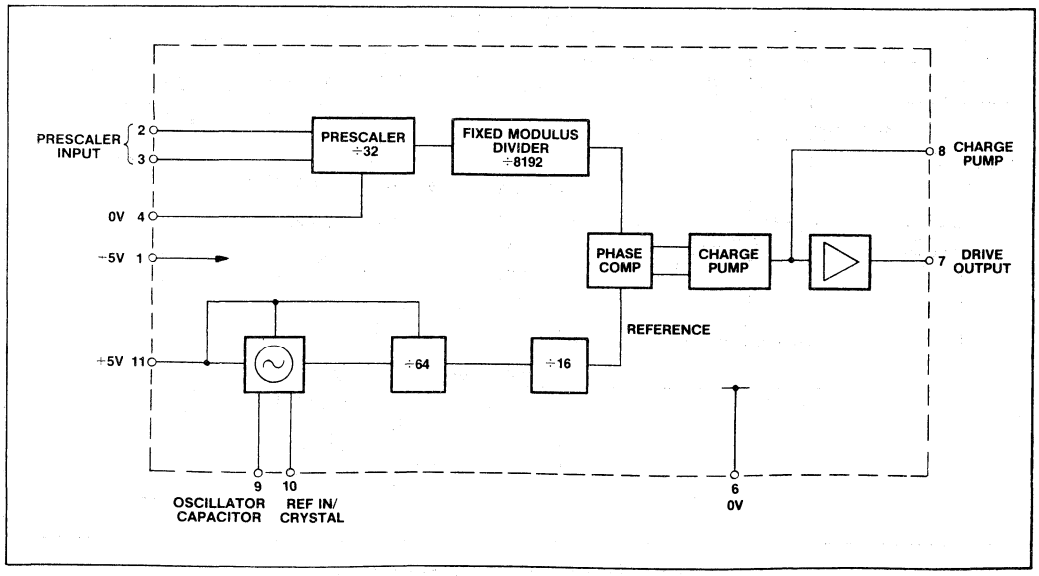


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = +4.5V to 5.5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	Vcc	1,11	4.5		5.5	V	
Supply current	Icc(1)	1		50	60	mA	
Supply current	Icc(11)	11		1		mA	
Prescaler input voltage		2,3	100			mV	300MHz to 2.0GHz sinewave
Prescaler input impedance		2,3		50		Ohms	
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/°C	Over 0 to 65°C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	Vcc = 4.5V to 5.5V
Reference clock frequency		10	2		8.0	MHz	
External reference amplitude		10	100		500	mV rms	
Reference input impedance		10		25		kohms	

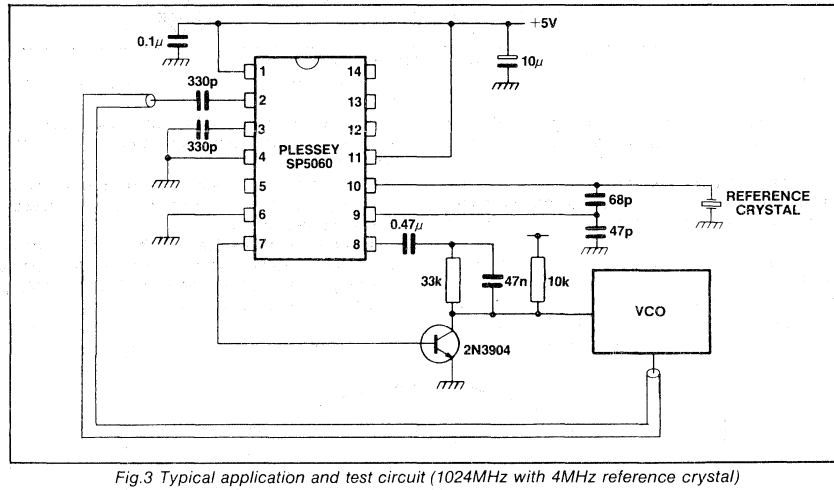


Fig.3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

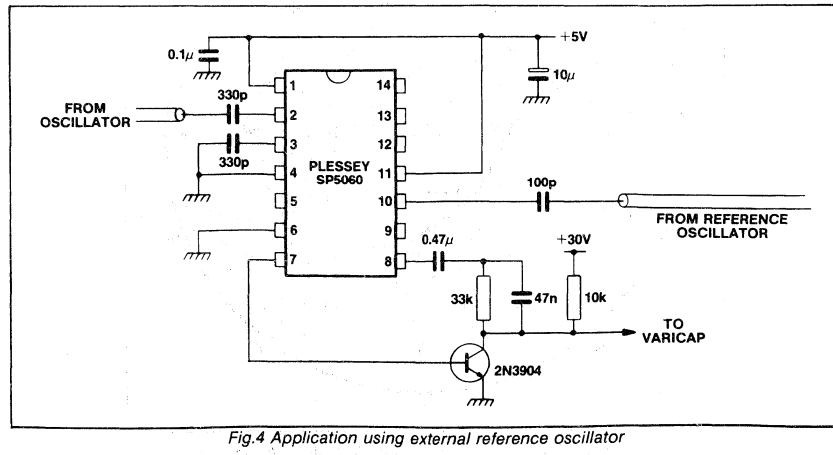


Fig.4 Application using external reference oscillator

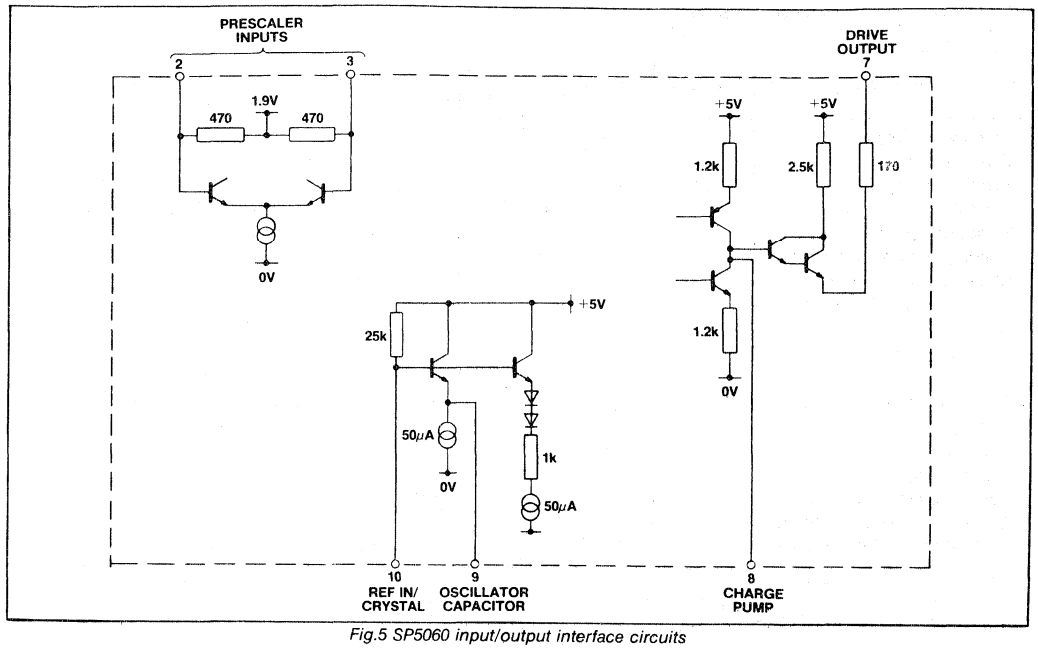


Fig.5 SP5060 input/output interface circuits

DESCRIPTION

The SP5060, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator reference frequency is obtained by dividing the reference frequency. This may be generated on chip, by means of a crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phase locked to the reference frequency.

The divider stages are arranged to give a fixed ratio, between the synthesised frequency and the reference, of 256:1.

Any frequency within the range 300MHz to 2.0GHz may be achieved using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output swing necessary for the oscillator varicap line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all the supply pins for the device to operate correctly.

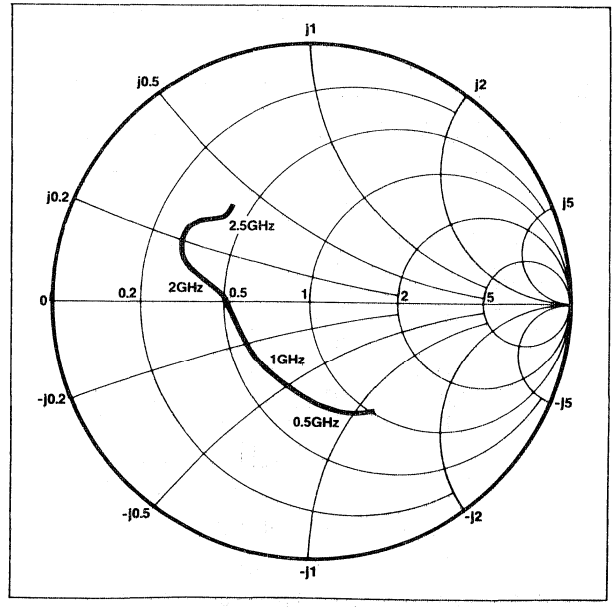


Fig.6 Typical input impedance Normalised to 50Ω

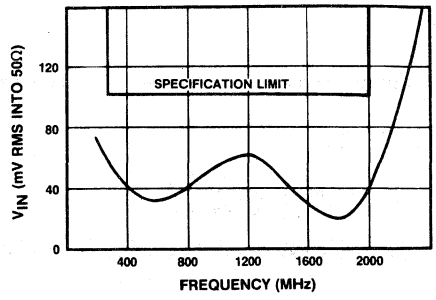


Fig.7 SP5060 typical input sensitivity

SP5062

2.3GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5062 is for use in outdoor (head end) units of satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- Synthesises Frequencies up to 2.3GHz

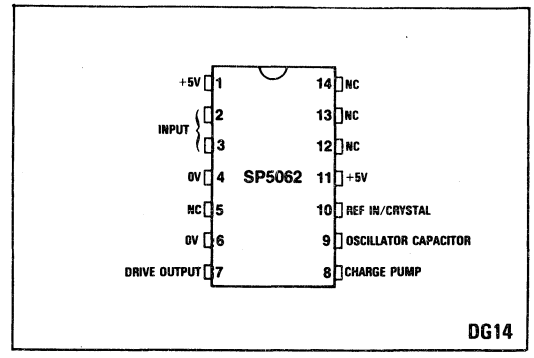


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	-10°C to +70°C
Maximum junction temperature	175°C
Storage temperature	-55°C to +125°C
Supply voltage Pin 1 and Pin 11	7V
Prescaler input voltage	2.5V p-p

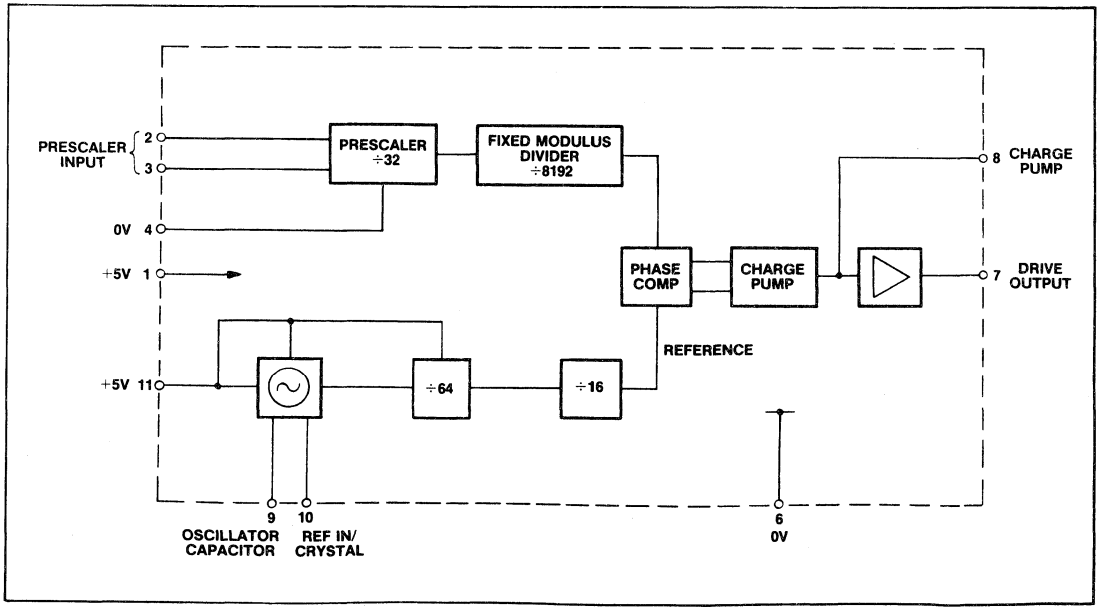


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = +4.5V to 5.5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	1,11	4.5		5.5	V	
Supply current	$I_{CC}(1)$	1		50	60	mA	
Supply current	$I_{CC}(11)$	11		1		mA	
Prescaler input voltage		2,3	See Fig.7				
Prescaler input impedance		2,3		50		Ohms	
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/°C	Over 0 to 65°C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	V_{CC} = 4.5V to 5.5V
Reference clock frequency		10	2		10	MHz	
External reference amplitude		10	100		500	mV rms	
Reference input impedance		10		25		kohms	

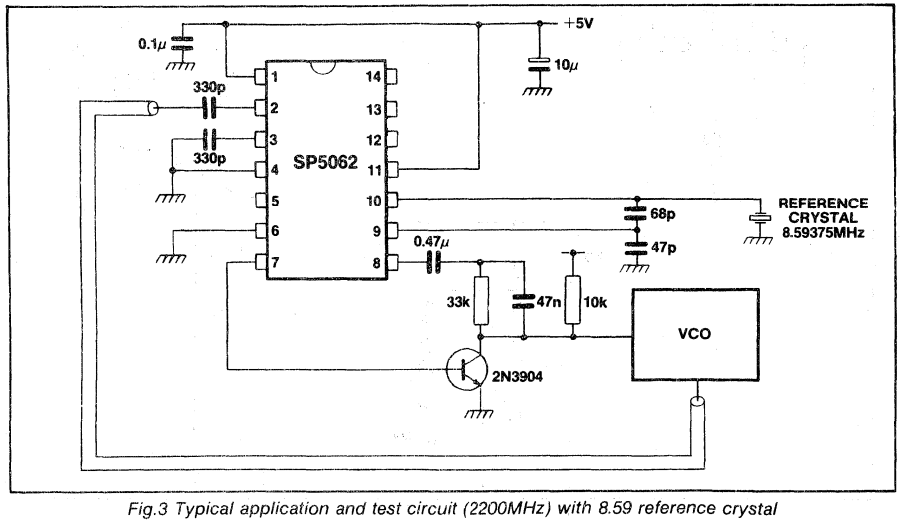


Fig.3 Typical application and test circuit (2200MHz) with 8.59 reference crystal

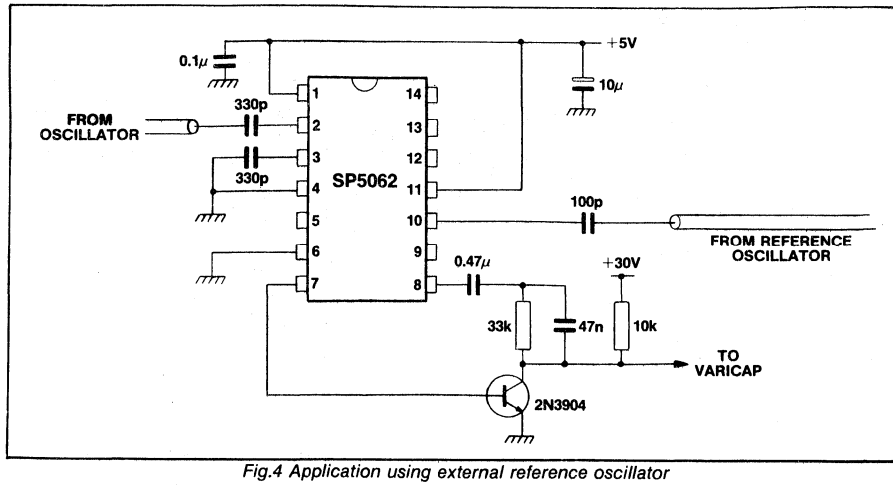


Fig.4 Application using external reference oscillator

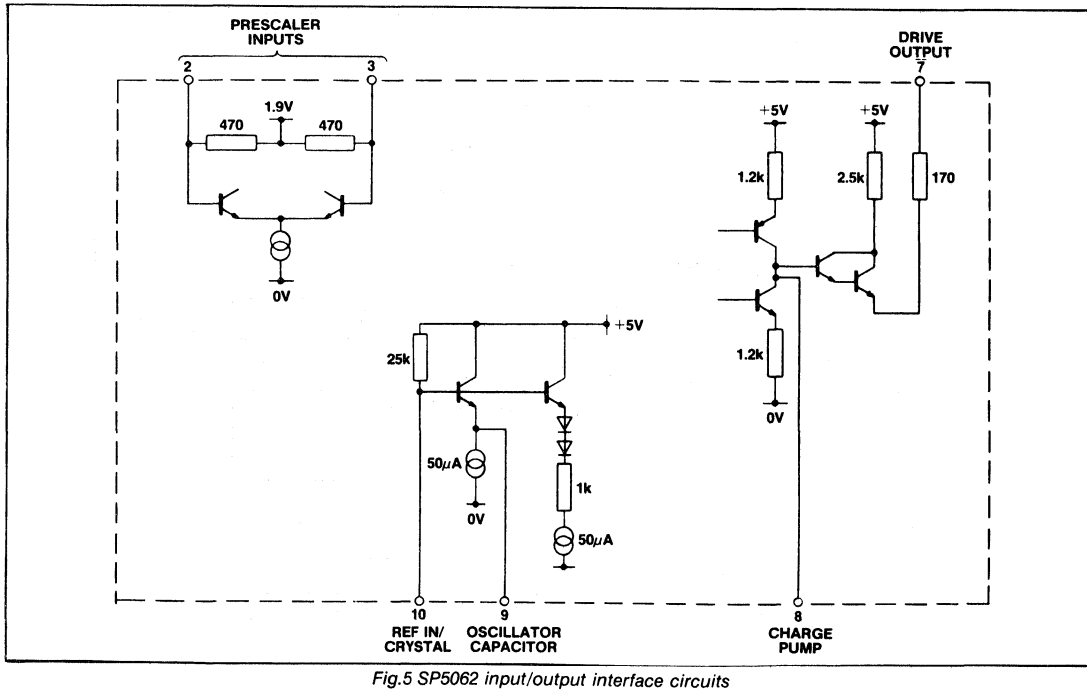


Fig.5 SP5062 input/output interface circuits

DESCRIPTION

The SP5062, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator reference frequency is obtained by dividing the reference frequency. This may be generated on chip, by means of a crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phase locked to the reference frequency.

The divider stages are arranged to give a fixed ratio, between the synthesised frequency and the reference, of 256:1.

Any frequency within the range 300MHz to 2.3GHz may be achieved using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output swing necessary for the oscillator varicap line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all the supply pins for the device to operate correctly.

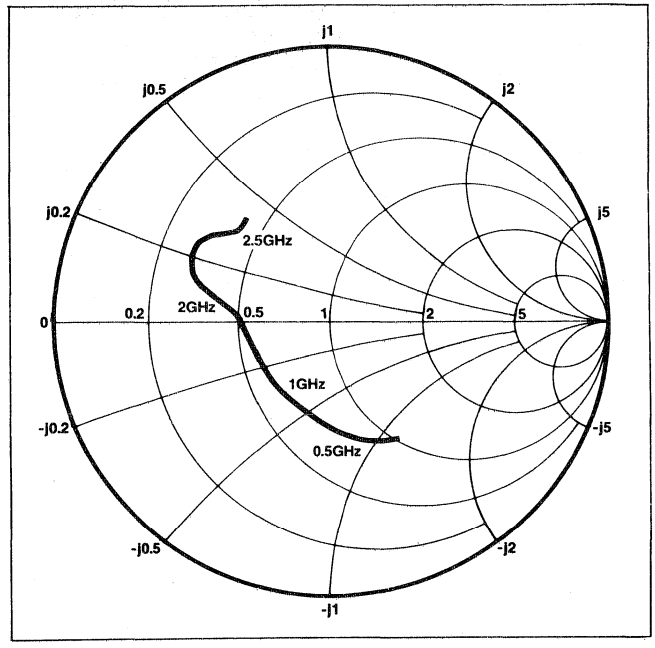


Fig.6 Typical input impedance Normalised to 50Ω

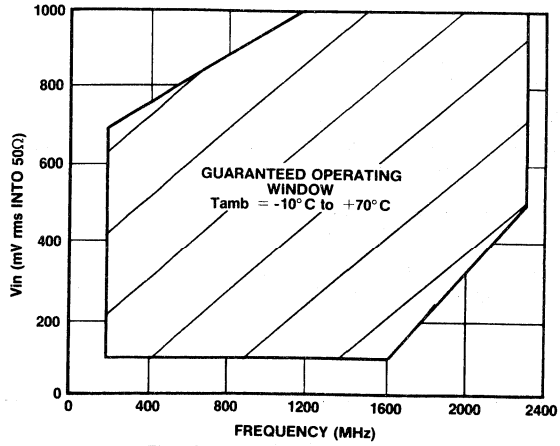


Fig.7 SP5062 typical input sensitivity

SP5510

1.3 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5510 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device also contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 Bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system. The comparison frequency is 7.8125kHz derived from a 4MHz Crystal.

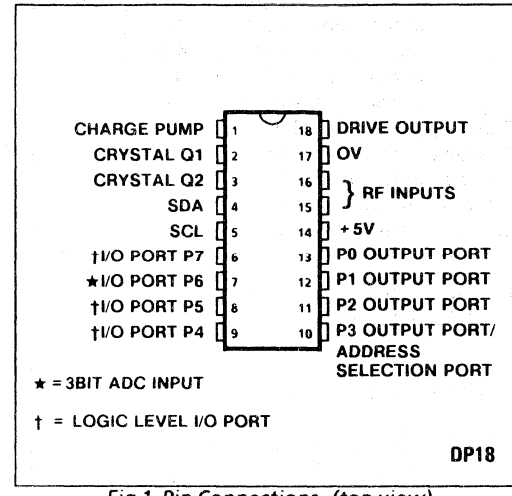


Fig 1 Pin Connections (top view)

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 43mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I²C BUS Address For Picture in Picture TV
- Full ESD Protection

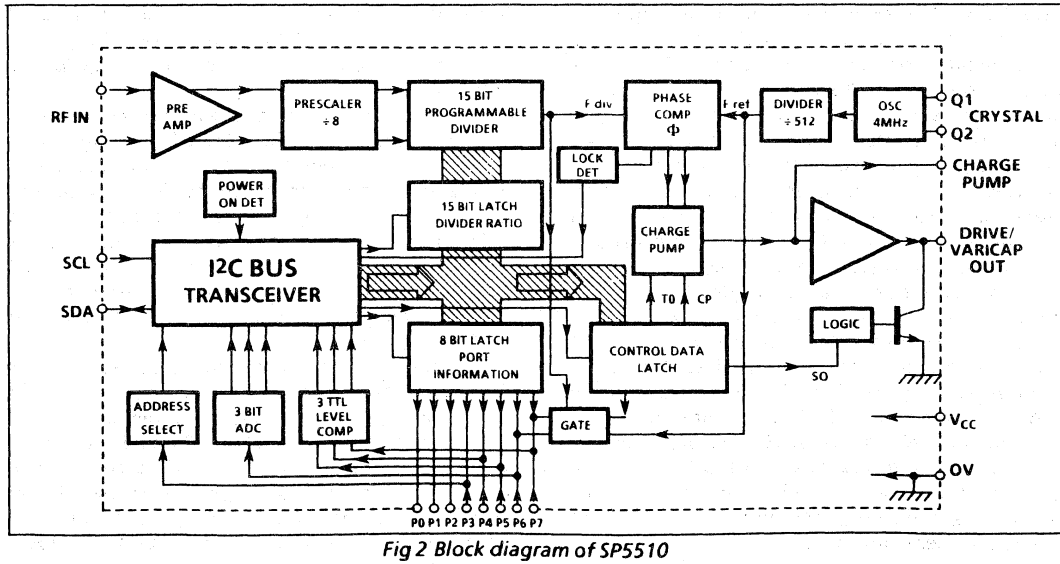


Fig 2 Block diagram of SP5510

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C, V_{CC} = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		43	50	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12.5		300	mV_{RMS}	50MHz to 1GHz
Prescaler input voltage	15,16	30		300	mV_{RMS}	1.3GHz
Prescaler input impedance	15,16		50		Ω	
input capacitance			2		pF	
SDA,SCL Input high voltage	4,5	3		5.5	V	
Input low voltage	4,5	0		1.5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			-10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte4 Bit2 = 0 V pin 1 = 2V
Charge pump current high	1		±250		µA	Byte4 Bit2 = 1 V pin 1 = 2V
Charge pump output leakage current	1			±1	µA	Byte4 Bit4 = 1 V pin 1 = 2V
Charge pump drive output current	18	500			µA	V pin 18 = 0.7V
Output ports						
P0 - P3 sink current	10 - 13	0.7	1	1.5	mA	V_{OUT} = 12V
P0 - P3 leakage current	10 - 13			10	µA	V_{OUT} = 13.5V
P4 - P7 sink current	6 - 9	10			mA	V_{OUT} = 0.7V
P4 - P7 leakage current	6 - 9			10	µA	V_{OUT} = 13.5V
Input ports						
P3 Input current high	10			+10	µA	V pin10 = 13.5V
P3 Input current low	10			-10	µA	V pin10 = 0V
P4,P6,P7Input voltage low	6,7,9			0.8	V	
P4,P6,P7Input voltage high	6,7,9	2.7			V	
P6 Input current high	7			+10	µA	See Table 3 for ADC levels
P6 Input current low	7			-10	µA	

FUNCTIONAL DESCRIPTION

The SP5510 is programmed from an I²C BUS.The data is fed in on the SDA line and clock on the SCL line as dictated by the I²C BUS format. The device can be programmed to accept new data (write mode) or to send data, derived from the input ports, and device status information (read mode). The Tables in Fig 3 illustate the format of the data. The device can be programmed to respond to several addresses This enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last Bit of the address Byte (R/W) sets the device into read mode if it is high and a write mode if it is low. When the SP5510 recieves a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5510 is programmed into the read mode the controlling device accepting the data can pull down the SDA line during the following acknowledge period to recieve another status Byte.

WRITE MODE-FREQUENCY SYNTHESIS

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while Bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is recieved and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Until an I²C BUS stop condition is recognised, additional data Bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmittion of data is stopped mid byte (i.e. by another device on the bus) then the previously programmed byte is maitained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15 Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	BYTE 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	BYTE 3
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	BYTE 4
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	P2	P1	P0	A	BYTE 5

Table 1 *write data format* MSB is transmitted first

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	BYTE 2

Table 2 *read data format*

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see table 4)
CP : Charge Pump Current Select
T1 : Test Mode Selection
T0 : Charge Pump Disable
OS : Varactor Drive Output Disable Switch
P7, P6, P5, P4, P3, P2, P1, P0 : Control Output States
POR : Power On Reset Indicator
FL : Phase Lock Detect Flag
I2, I1, I0 : Digital Information From Ports P7, P5 and P4 Respectively
A2, A1, A0 : 5 Level ADC Data From P6 (see table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to V_{CC}
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 *ADC levels*

MA1	MA0	Voltage input to P3
0	0	0
0	1	ALWAYS VALID
1	0	$0.5V_{CC}$
1	1	V_{CC}

Table 4 *Address selection*

Fig3 Data formats

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the 7.8125KHz reference obtained by dividing the output of the 4MHz crystal oscillator by 512.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit a logic"1"for ± 250µA and a logic"0" for ± 50 µA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band.Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (C0) switches the charge pump drive amplifier's output off when it is set to a logic "1". Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic "1" connects P6 to F_{ref} and P7 to F_{div}.

Byte 5 programs the output ports P1 to P7 a logic "0" for a high impedence output , a logic "1" for low impedence (on).

READ MODE When the device is in the read mode the status data sent from the device on the SDA line takes the form shown in Table 2.
Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3 Volts and the programmed information lost (eg:when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedence when the device is initially powered up. Bit 2 (PLD) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively a logic 0 indicates a low level and a logic 1 for a high level. If the ports are to be used as input ports then they should not be programmed to output a low impedence state (logic 1). These inputs will then respond to data complying with standard TTL voltage levels. Finally Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in the typical application circuit.

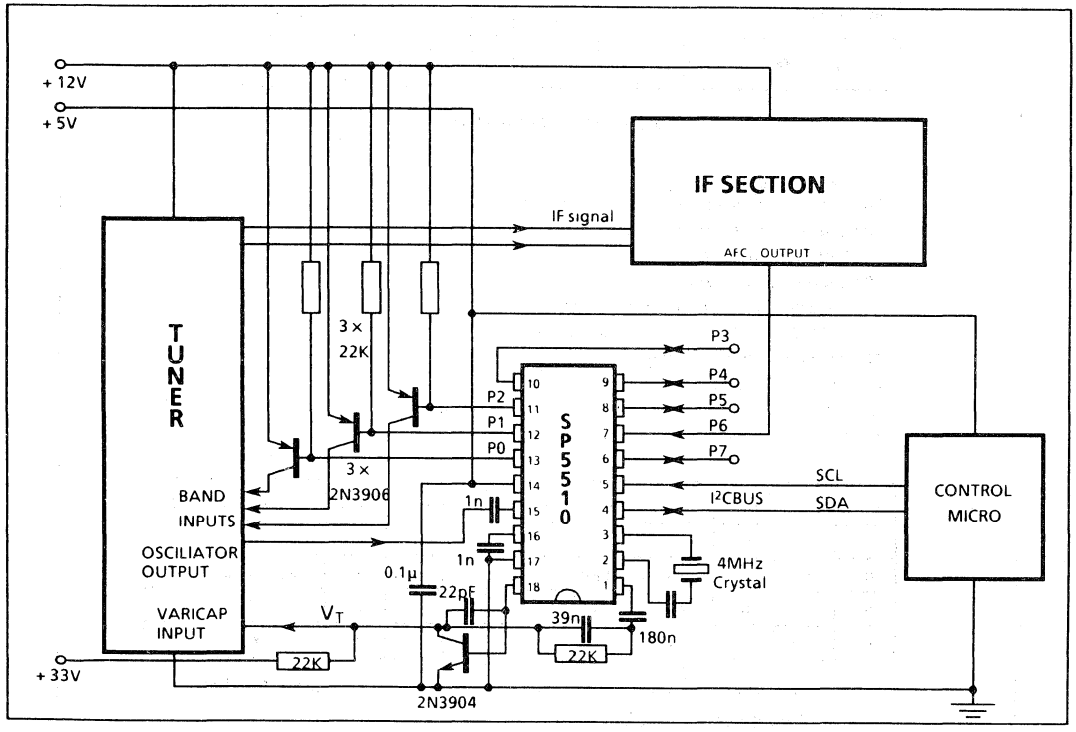


Fig 4 Typical application

PLESSEY
Semiconductors

SP973T8

30MHz TTL/CMOS 8-BIT FLASH ADC

The Plessey SP973T8 contains 255 high speed comparators which form a full flash analog to digital converter that requires no preceding sample and hold.

Its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage reference gives low DC drift over a wide operating temperature range (-40°C to +85°C in DG package).

The device also contains a full 8-bit D-type latch, which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

The SP973T8 is available in two variants: the SP973T8 B has ±½ LSB differential linearity and the SP973T8 C has ±1 LSB differential linearity, with a consequent cost advantage.

The ADC is designed for applications where power consumption is at a premium (550mW typ).

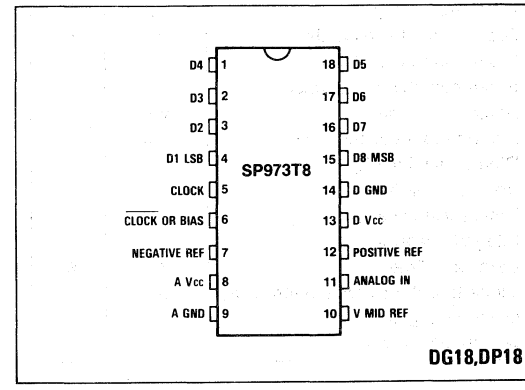


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP973T8 B DG (Industrial - Ceramic DIL package)
SP973T8 C DP (Commercial - Plastic DIL package)

FEATURES

- Wideband Analog Input: 70MHz 3dB (Typ.)
- Flash Converter, No Sample and Hold Required
- Low Power Consumption (550mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- Band Gap for Good Temperature Stability
- Wide Operating Temperature Range
- Static Protection on all Digital Inputs and Outputs
- Designed for Wideband Application
- Single 5V Supply
- No Missing Codes

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	12V
Output current	10mA
Input voltage	Vcc
Storage temperature	-55°C to +175°C
Operating temperature	<150°C

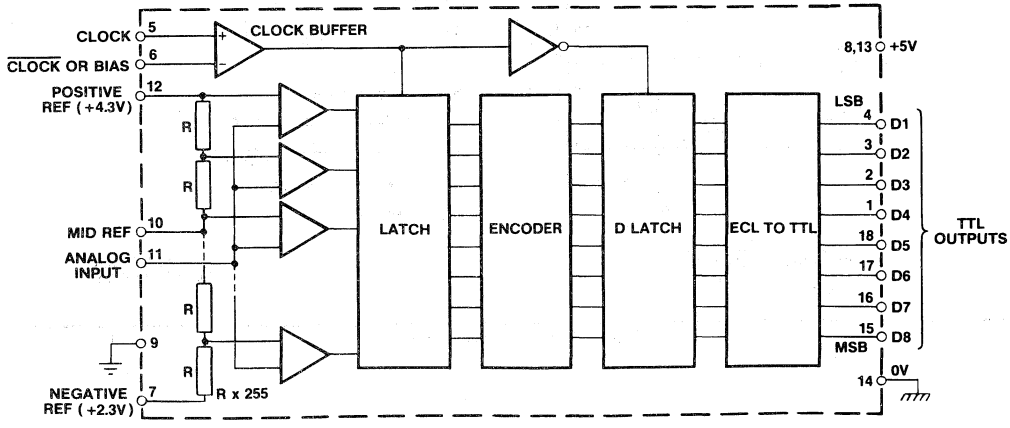


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{CC} = +5V ± 0.25V,

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		95		mA	
Power consumption			550	700	mW	
Clock frequency	fc	30			MHz	
Digital output level high	V_H	3.5	4.3		V	One TTL load. Fig.5
Digital output level low	V_L		0.3	0.4	V	One TTL load. Fig.5
Reference chain resistance	Rr		390		Ω	
Analog input range	V_{IN}	2.3		4.3	V	
Analog input capacitance	C_{IN}		40		pF	
Differential linearity				±0.5	LSB	SP973T8 B (DG package)
Integral linearity				±1.0	LSB	SP973T8 B (DG package)
Differential linearity				±1.0	LSB	SP973T8 C (DP package)
Integral linearity				±1.0	LSB	SP973T8 C (DP package)
Data valid time	tv	40	45		ns	20MHz clock
Clock to output propagation delay	tpd			10	ns	After 1 cycle delay
Differential gain				1	%	
Differential phase				1	Deg	

THERMAL CHARACTERISTICS

SP973T8 B θ_{JA} = 92°C/W
θ_{JC} = 21°C/W
SP973T8 C θ_{JA} = 75°C/W
θ_{JC} = 20°C/W

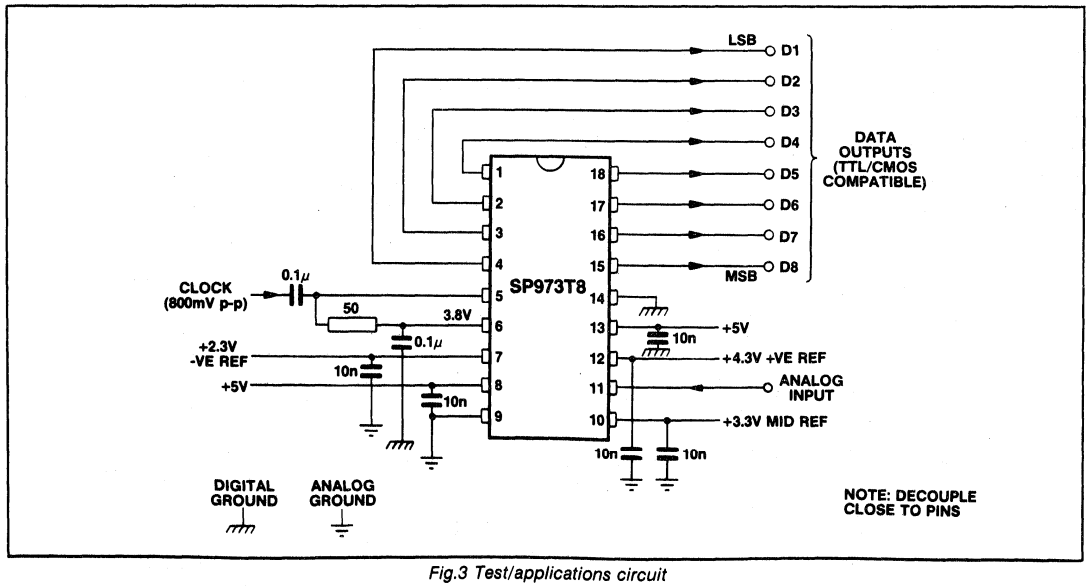


Fig.3 Test/applications circuit

OPERATING NOTES

The SP973T8 ADC will operate at clock frequencies up to and above 30MHz. It is therefore necessary to take care with the ground plane and component placement around the device.

Split analog and digital grounds with good decoupling close to the device pins, will reduce digital to analog crosstalk and hence aid performance.

The optimum differential linearity is achieved using the widest possible reference voltage. Therefore standard applications should use +4.3V positive reference and +2.3V negative reference.

The optimum input signal for use with these recommended reference voltages is 2V p-p biased at +3.3V.

The Plessey SL9999 is a suitable op-amp/ADC driver to provide this offset and drive the SP973T8 input at high speed.

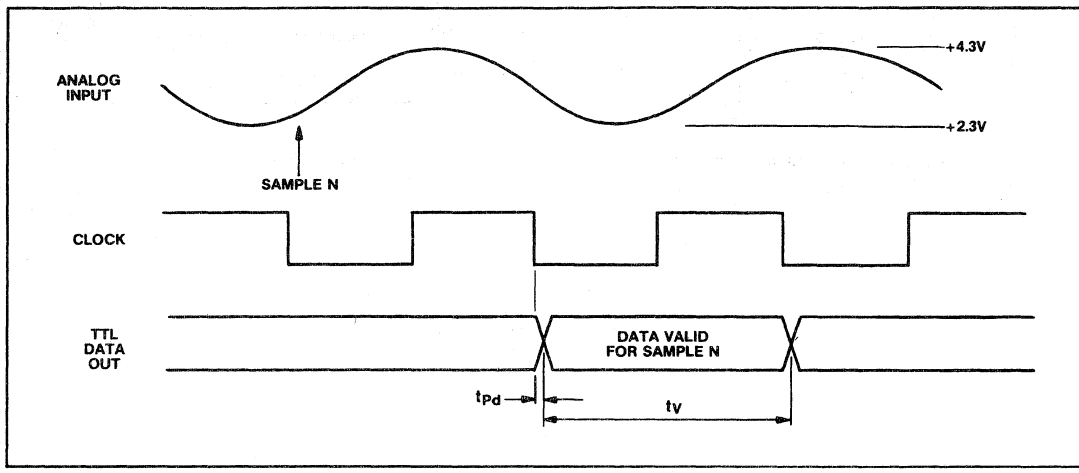


Fig.4 Timing diagram

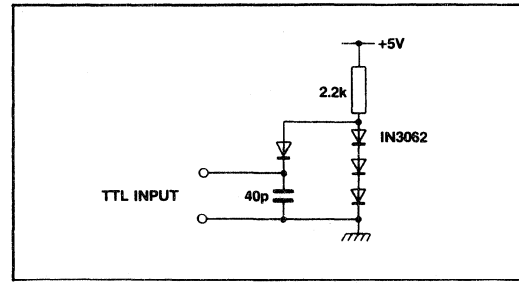


Fig.5 Standard TTL test load

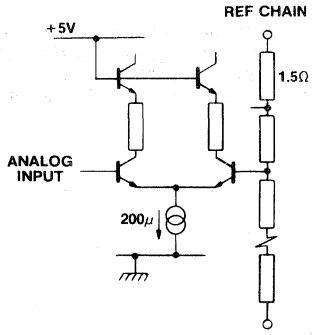


Fig.6a One of 255 analog inputs connected to pin 8

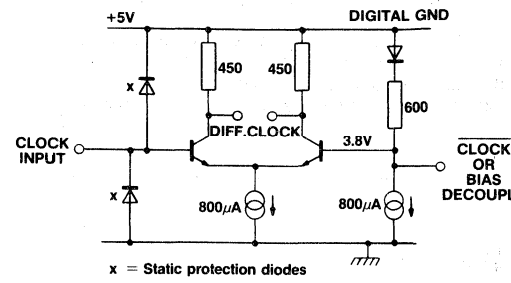


Fig.6b Clock input

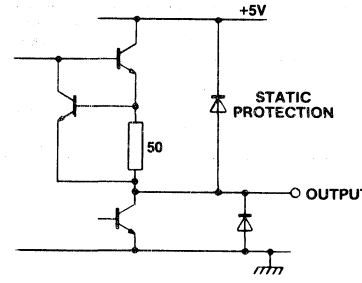


Fig.6c TTL output stage

Fig.6 Internal circuits

PLESSEY
Semiconductors

TDA5030A

TV VHF MIXER OSCILLATOR/UHF IF PREAMPLIFIER/IF AMPLIFIER

The TDA5030A is designed for use within a UHF/VHF TV tuner and consists of a VHF local oscillator, a VHF mixer, a UHF IF preamplifier and an IF amplifier for driving a SAW filter. The device also includes a buffered output from the VHF local oscillator to drive a prescaler or synthesiser and a UHF/VHF switching circuit. The device requires a minimum of external components to produce a full VHF tuner with an IF amplifier for a UHF tuner section.

FEATURES

- Balanced VHF Mixer
- VHF Oscillator (70-520 MHz)
- Differential SAW Filter Drive
- IF Amp for UHF IF Input
- Buffered VHF Oscillator Output
- UHF/VHF Switching Circuit
- Full Static Protection on all Pins

APPLICATIONS

- TV Tuners for TV and Video Recorders

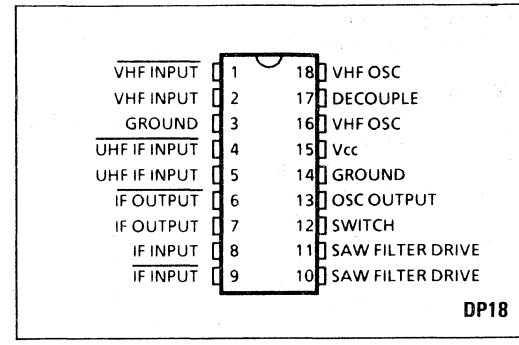


Fig 1 Pin Connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	14V
Input voltage	5V
VHF Switching voltage	Vcc + 0.3V
VHF Switching current	10mA
Output current	10mA
Operating temperature range	-25°C to + 85°C
Storage temperature range	-55°C to + 125°C

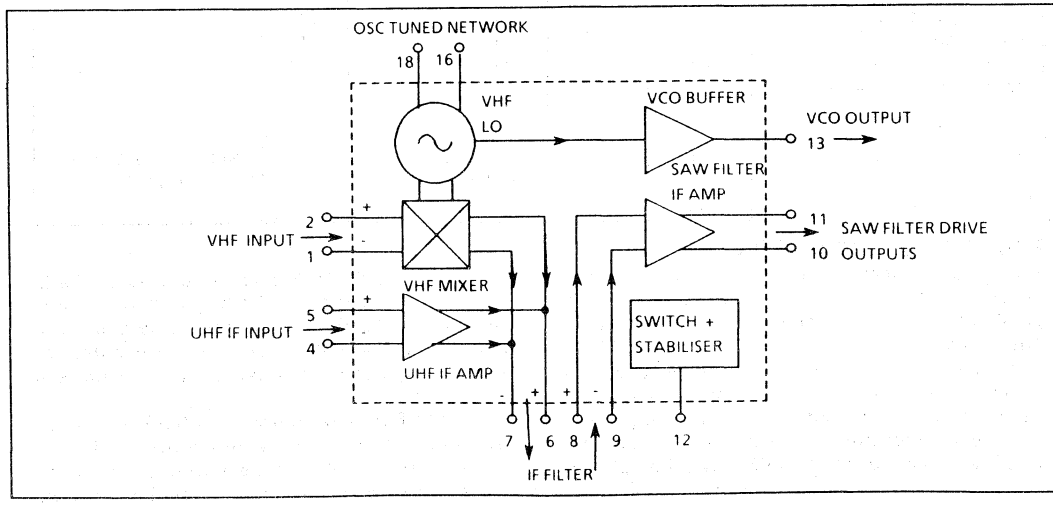


Fig 1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, Supply Voltage = +12V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage Vcc	15	10	12	13.2	V	
Supply Current	15	-	42	55	mA	VHF Oscillator on
Switch voltage level for VHF	12	0	-	2.5	V	
Switch voltage level for UHF	12	9.5	-	Vcc + 0.3	V	
Switch current	12	0.05	-	0.7	mA	UHF selected
VHF Local Oscillator/Buffer						
Frequency range	13	70	-	470	MHz	
Frequency shift with Vcc	13	-	-	200	KHz	ΔVcc = 10% F = 70 to 330 MHz
Output Voltage	13	14	20	-	mV RMS	F < 100MHz
	13	10	20	-	mV RMS	F > 100MHz
Output impedance	13	-	90	-	Ω	
RF on Local oscillator output	13	-	-30	-	dB	w.r.t. local oscillator
IFon Local oscillator output	13	-	-30	-	dB	w.r.t. local oscillator
Local oscillator harmonics	13	-	-14	-	dB	w.r.t. local oscillator
VHF Mixer(including IF amp)						
Voltage gain	1,2,10,11	23	25	27	dB	See test circuit
Input conductance	1,2	-	0.23	-	mS	50MHz
	1,2	-	0.5	-	mS	225MHz
	1,2	-	0.67	-	mS	300MHz
Input capacitance	1,2	-	2.5	-	pF	
Output impedance	6,7	-	1.6	-	KΩ	(mixer only)
Noise Figure		-	7	-	dB	50
		-	8.5	-	dB	225MHz
		-	9.5	-	dB	300MHz
		-	10.25	-	dB	470MHz
Input for 1% cross-modulation(in channel)	1,2	97	99		dBμV	
UHF IF Amplifier(IF amp incl)						
Voltage gain	4,5,10,11	32	34	36	dB	
Input conductance	4,5	-	0.3	-	mS	
Input capacitance	4,5	-	3	-	pF	
Noise Factor			5	6	dB	
Input for 1% cross-modulation(in channel)	4,5	88	90	-	dBμV	
SAW filter IF amplifier						
Input impedance	8,9	-	300 + 100j	-	Ω	Load = 2K (between Pin 10 and 11)
Output impedance	10,11	-	200	-	Ω	

FUNCTIONAL DESCRIPTION

The on board VHF Local oscillator will oscillate between 70 and 470 MHz depending on the parallel tuned circuit connected to pins 16 and 18. The tuned circuit is coupled to pins 16 and 18 via two 1.8 pF capacitors, as in Fig 2, these capacitors provide the correct transfer caracteristics for oscillation. The tuned circuit will require a switcheable inductor if more than one of the VHF bands are to be tuned to, Fig 2 shows the inductor values required for European VHF Bands I and III.

The input to the VHF mixer can be differential or single ended with one input decoupled, as in Fig 2.

The output of the VHF mixer is coupled to the IF amplifier via a simple IF filter and two 150Ω resistors. The 150Ω resistors limit the gain of the IF amplifier to ensure stable operation. The output of the IF amplifier is designed to directly drive a standard SAW filter.

The VHF Local oscillator has a buffered output designed to drive a prescaler or synthesiser directly.

An alternative IF source,e.g. from a UHF mixer, can be coupled into the tuner after the mixer via Pins 4 and 5. This input is enabled and the VHF Local oscillator disabled when Pin 12 is taken high.

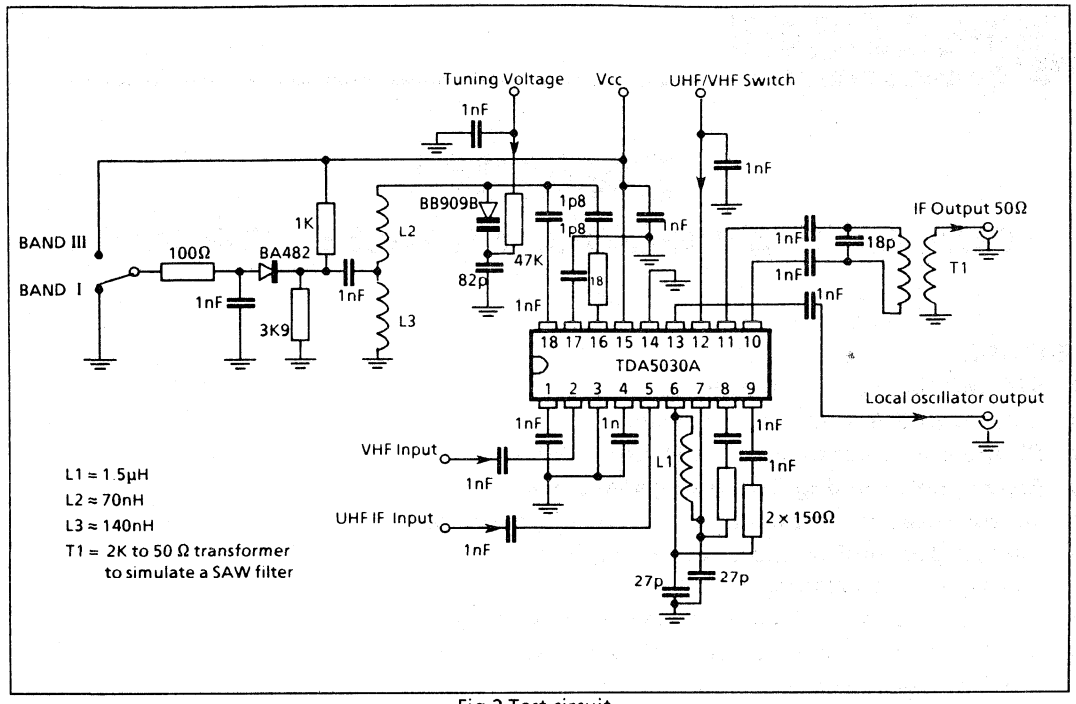


Fig 2 Test circuit

PCB LAYOUT

The Tuner should be layed out with the oscillator and decoupling components suituated as close as possible to the TDA5030A . A double sided PCB with a good earth plane is advised, although it is not essential.

PLESSEY
Semiconductors

ZNA134J

CCIR/EIA TV SYNCHRONISING PULSE GENERATOR

FEATURES

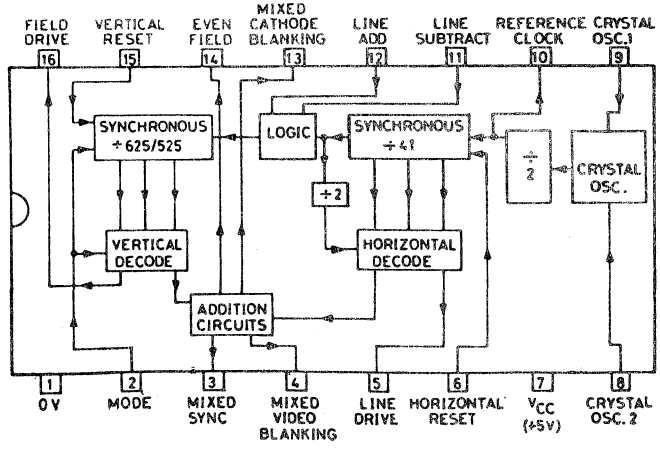
- 625 and 525 line standards.
- CCIR and EIA standard outputs.
- Single 5 volt supply, fully TTL compatible.
- Easy synchronising between generators.
- Direct reset to vertical and horizontal counters.
- Facility for adding and subtracting lines.
- Automatic interlacing.
- On chip oscillator (requiring external crystal).
- Can be driven with an external oscillator.
- Field reference output.

GENERAL DESCRIPTION

The ZNA134 integrated circuit utilises a 2.5 MHz* crystal to generate all the horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in 625 or 525 line commercial, industrial or military television systems. The synchronous dividers and decoding logic employed within the unit ensure perfect interlace, together with spike-free output waveforms having precisely defined relative positions and pulse widths. The device is contained in a 16 pin D.I.L. and can be selected to operate over the military temperature range.

*Dependent on line system used, series resonant.

SYSTEM DIAGRAM



DG16

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Maximum value
Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C*
Storage Temperature Range	−65°C to +150°C

*Also available over wider range on request.

OPERATING CHARACTERISTICS

(over recommended temperature range)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	Volts
Supply Current	I_S		–	100	–	mA
High-level Input Voltage	V_{IH}		2.4	–	–	Volts
Low-level Input Voltage	V_{IL}		–	–	0.8	Volts
High-level Input Current	I_{IH}	V_{CC} = 5V, V_I = 2.4V (See Note 1)	–	–	40	μA
Low-level Input Current	I_{IL}	V_{CC} = 5V, V_I = 0 V. (See Note 1)	−40	–	–	μA
High-level Output Voltage	V_{OH}	V_{CC} = 5V, $I_{source} \leqslant 80\mu A$ (See Note 2)	2.4	–	–	Volts
Low-level Output Voltage	V_{OL}	V_{CC} = 5V, $I_{sink} \leqslant$ 3.2 mA (See Note 2)	–	–	0.5	Volts
Clock frequency	f_{clock}	625 lines, Mode = '1' 525 lines, Mode = '0'	– –	2.56250 2.5830	– –	MHz MHz
External Oscillator Pulse Width	t_w	-ve going pulse, 625/525 lines	150	200	250	ns

Note 1

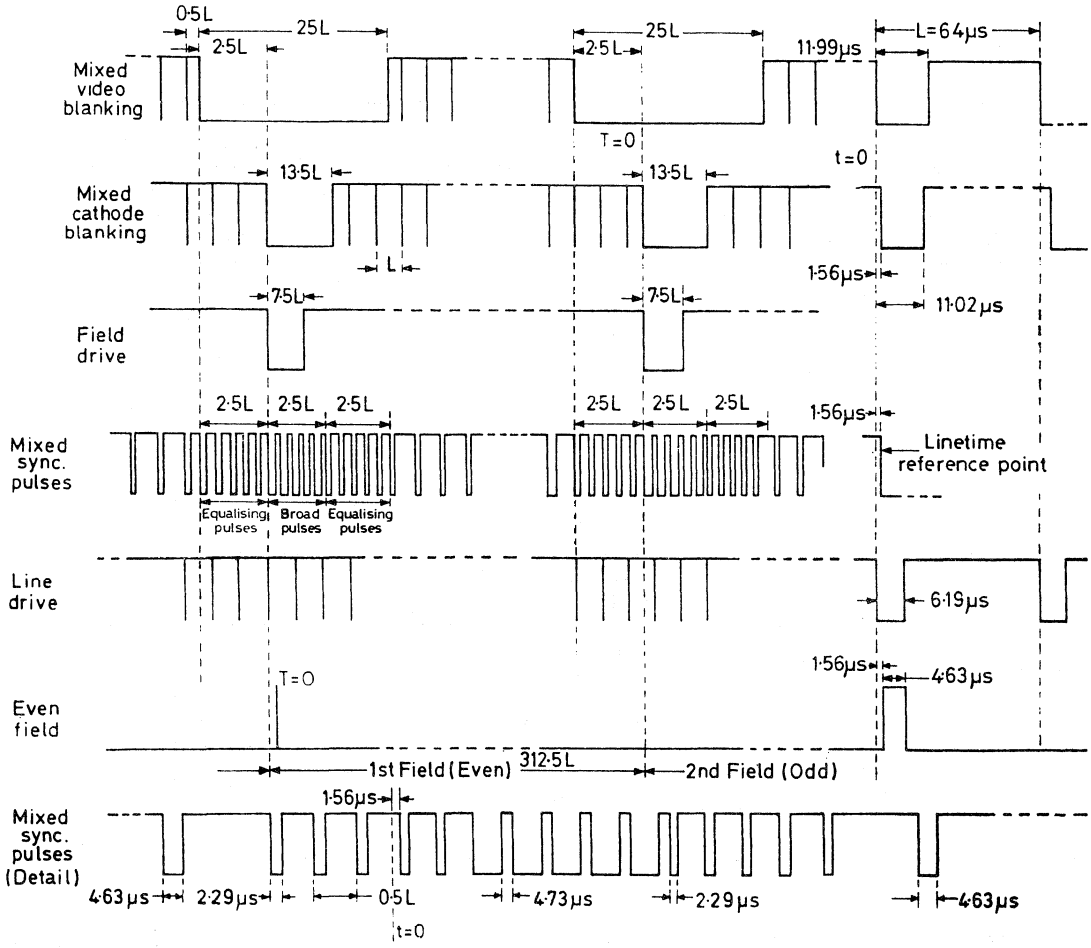
Input conditions only apply to mode, horizontal reset, vertical reset, line subtract and line add. For input conditions of oscillator inputs C.0.1, C.0.2, see applications section.

Note 2

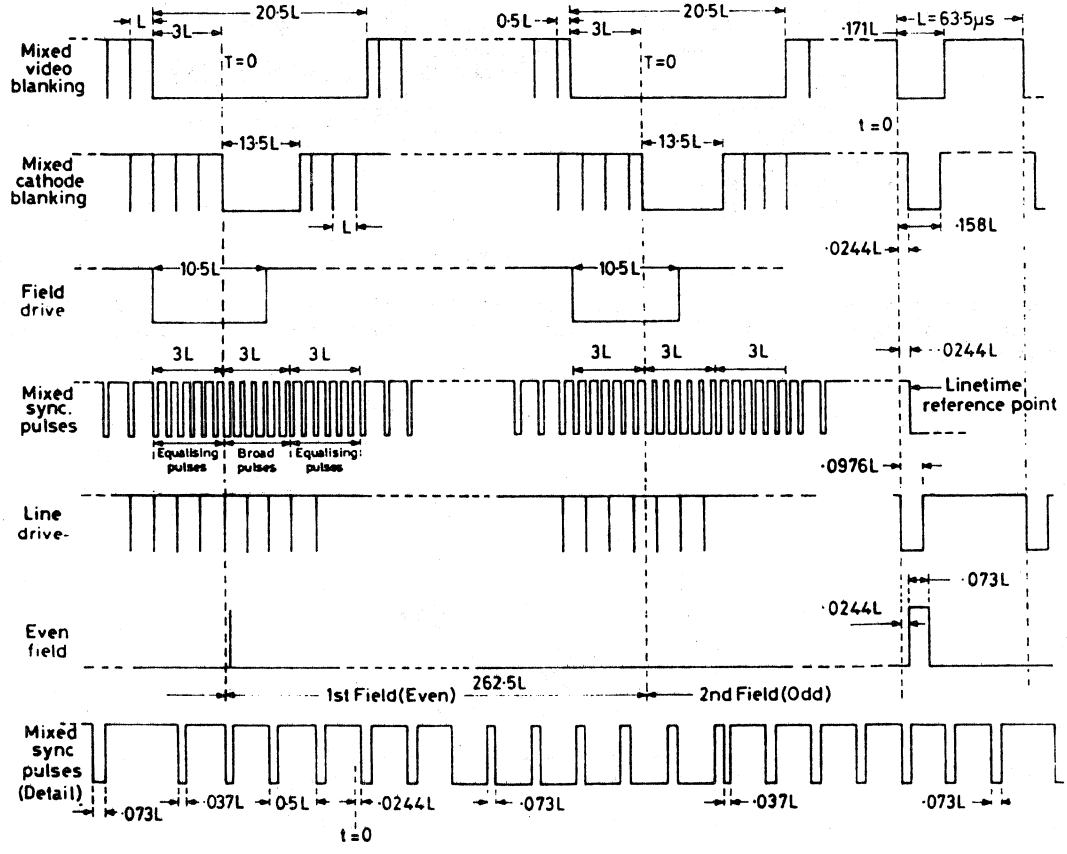
All outputs – mixed sync, mixed video blanking, line drive, reference clock, mixed cathode blanking, even field and field drive have internal 10kΩ pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors. These should have a minimum value of 2kΩ.

OUTPUT WAVEFORMS

(a) 625 line CCIR standard output (Mode = 1).
Crystal frequency = 2.5625 MHz.
Line frequency = 15.625 kHz, Field frequency = 50 Hz.
Line period = 64 μs, Field period = 20 ms.



(b) 525 line EIA standard output (Mode = 0).
Crystal frequency = 2.5830 MHz
Line frequency = 15.750 kHz, Field frequency = 60 Hz
Line period = 63.5 μs, Field period = 16.66 ms.



APPLICATIONS INFORMATION

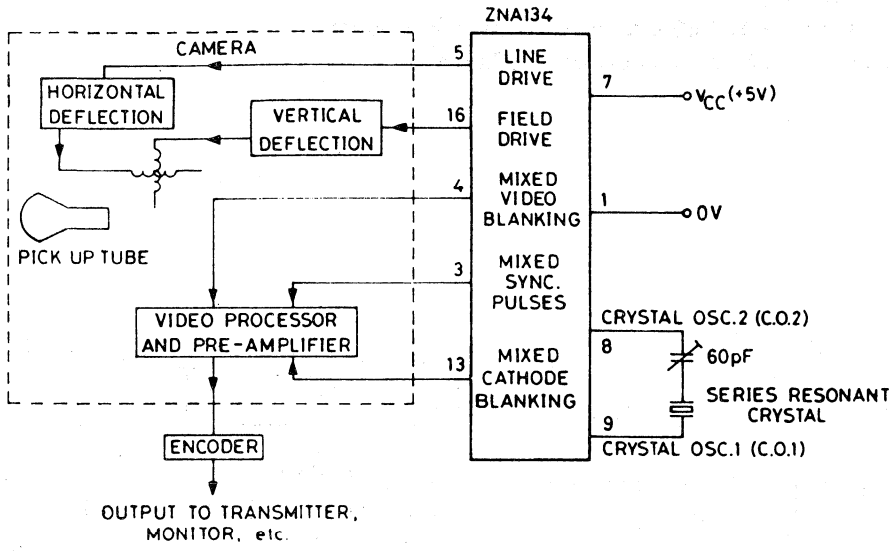


Fig. 1. Application in a TV system

The sync. pulse generator can be driven from an external oscillator if required. C.O.1 must then be connected via a 10kΩ resistor to V_{CC}. The external oscillator can then drive directly into C.O.2 input as shown in Fig. 2.

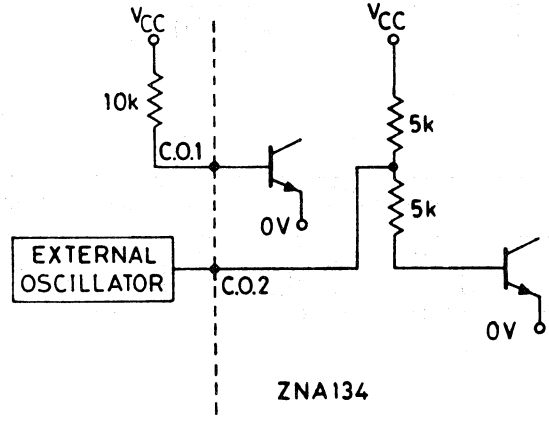


Fig. 2

Mode input (pin 2) can be connected directly to V_{CC} or 0V for 625 or 525 line operation respectively Any of the inputs: vertical reset, horizontal reset, line add, line subtract, not being used should be connected to 0V.

SIMPLE METHOD OF SYNCHRONISATION USING VERTICAL AND HORIZONTAL RESET

Line synchronisation (Fig. 3) is achieved by using a narrow positive going pulse derived from the negative going edge of the Line Drive output of the first generator to drive the Horizontal Reset inputs of the other generators. This monostable pulse, which should have a width of 200 ns ± 40 ns, resets the generators to the start of a line (t = 0). This results in the Line Drive waveforms of the driven generators being one reference clock period (≃800 ns) delayed from the first generator. The C.O.2 pins of the generators must be connected together.

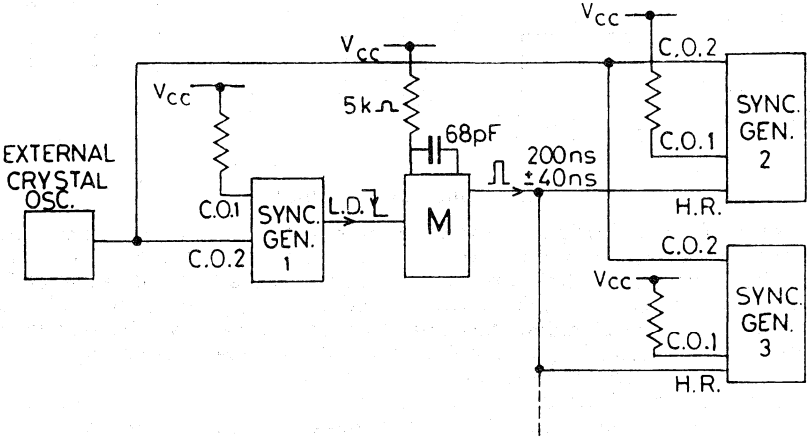


Fig. 3 Line Synchronisation using Horizontal Reset

Field Synchronisation (Fig. 4) is achieved by driving the Vertical Reset inputs of the driven generators directly from the Even Field output of the first generator (the Line drive outputs should already be in phase). This resets the generators to the start of the first field (T = 0, start of broad pulses.)

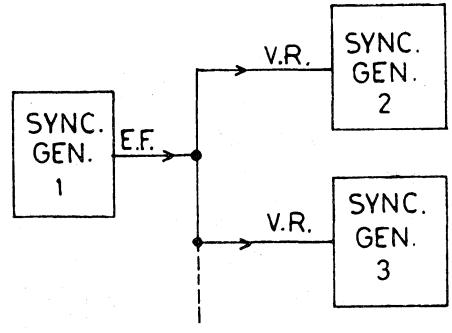


Fig. 4 Field Synchronisation using Vertical Reset

With this method of synchronisation, line sync and field sync are lost at the monitor for a brief period due to a sudden change in the Mixed Sync waveform. Hence it is only suitable for CCTV systems where momentary loss of picture is not critical or where the generators are to be synchronised automatically at power switch on.

SYNCHRONISATION USING THE LINE ADD/SUBTRACT FACILITY

This is suitable where generator lock must be achieved gradually, i.e. without loss of picture at the receiver, as in studio camera systems.

Line Synchronisation can be achieved smoothly by the use of a phase locked loop technique rather than the direct Horizontal Reset technique (Fig. 5).

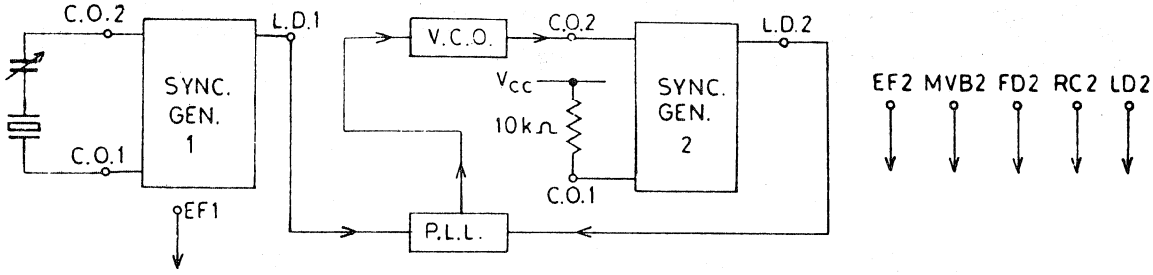


Fig. 5 Line Lock Circuitry

Field Synchronisation (Fig. 6). The generator waveforms are brought into synchronisation by adding or subtracting one line per frame to the second generator until the waveforms are exactly in phase. This is achieved by adding or inhibiting pulses at the start of the first full line after field blanking, thus preventing any changes to the mixed sync. waveform during the broad and equalising pulse periods. Lines are 'added' by clocking the vertical counter faster than the normal half line rate. Setting Line Add high for a period equal to 4 Reference Clock pulses, increments the vertical counter by one line thus effectively reducing the field period by one line.

Lines are 'subtracted' by inhibiting the clock pulses to the vertical counter. Setting Line Subtract high for a period of one line leaves the state of the vertical counter unchanged for one line thus effectively increasing the field period by one line.

Hence the add or subtract periods are generated by counting Reference Clock or Line Drive pulses respectively with a 3 bit counter.

Lines are added or subtracted until the generators are in phase. The two Even Field outputs together generate a pulse which inhibits the add/subtract circuitry when an in-phase condition occurs.

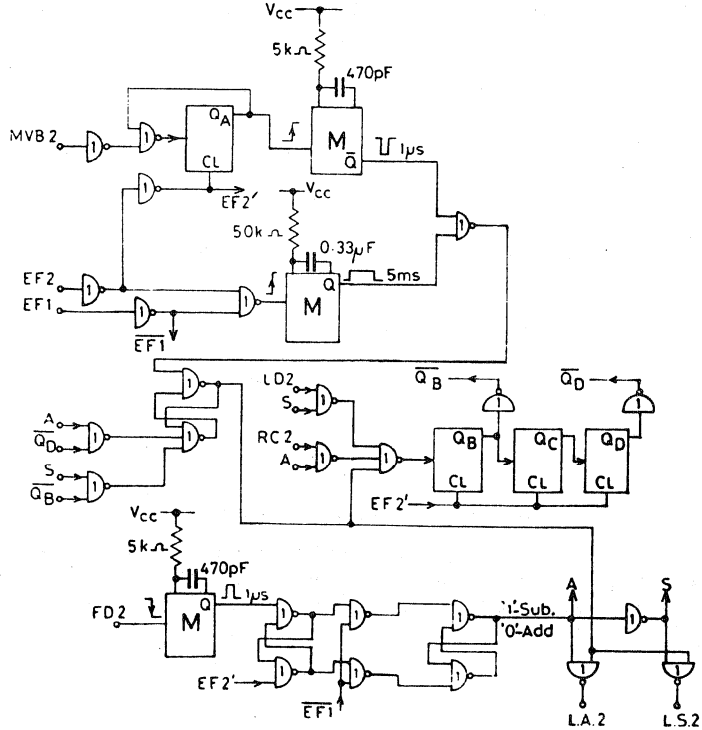


Fig. 6 Field Lock Circuitry

Lines are added to the second generator if EF2 is less than one field period delayed from EF1, and subtracted if EF2 is greater than one field period delayed from EF1 to reduce synchronisation time The add/subtract circuitry can be built using nine TTL packages :-

4 off	7402
1 off	7427
1 off	7404
1 off	74123
1 off	74121
1 off	7493

The circuit in Fig. 6 adds or subtracts one line per frame but this could be extended to two or more lines per frame by adding further bits to the 3 bit counter and decoding the relevant states. Similarly half a line per frame can be added by decoding 'QC' instead of 'QB'.

The circuit operates in 625 or 525 line mode without any changes to the component values.

PLESSEY
Semiconductors

ZNA234E

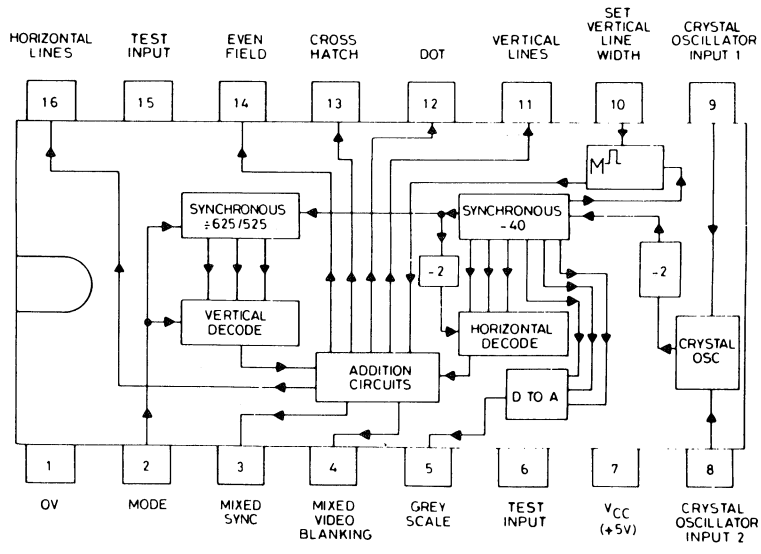
TV PATTERN GENERATOR

FEATURES

- Single 5V supply.
- 625 or 525 line operation.
- Sync and Blanking outputs to CCIR or EIA Standard.
- Field Reference output.
- Separate outputs for:
  - Crosshatch
  - Dot
  - Vertical Lines
  - Horizontal Lines
  - Greyscale
  - Mixed Sync
  - Mixed Video Blanking
- Adjustable vertical line width.

DESCRIPTION

The ZNA234E integrated circuit makes available all the waveforms necessary to produce cross-hatch, dot and greyscale test patterns on a television screen. All that is required is a 2.50MHz crystal (or external oscillator) and a minimum number of external components for mixing video, sync and blanking pulses to give a composite video signal. This can be either injected directly into the video stages of a receiver, or used to drive a UHF modulator/oscillator for connection to the aerial socket. The device is contained in a 16 pin DIL package.



System Diagram **DP16**

ABSOLUTE MAXIUMUM RATINGS

Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

OPERATING CHARACTERISTICS (over recommended temperature range).

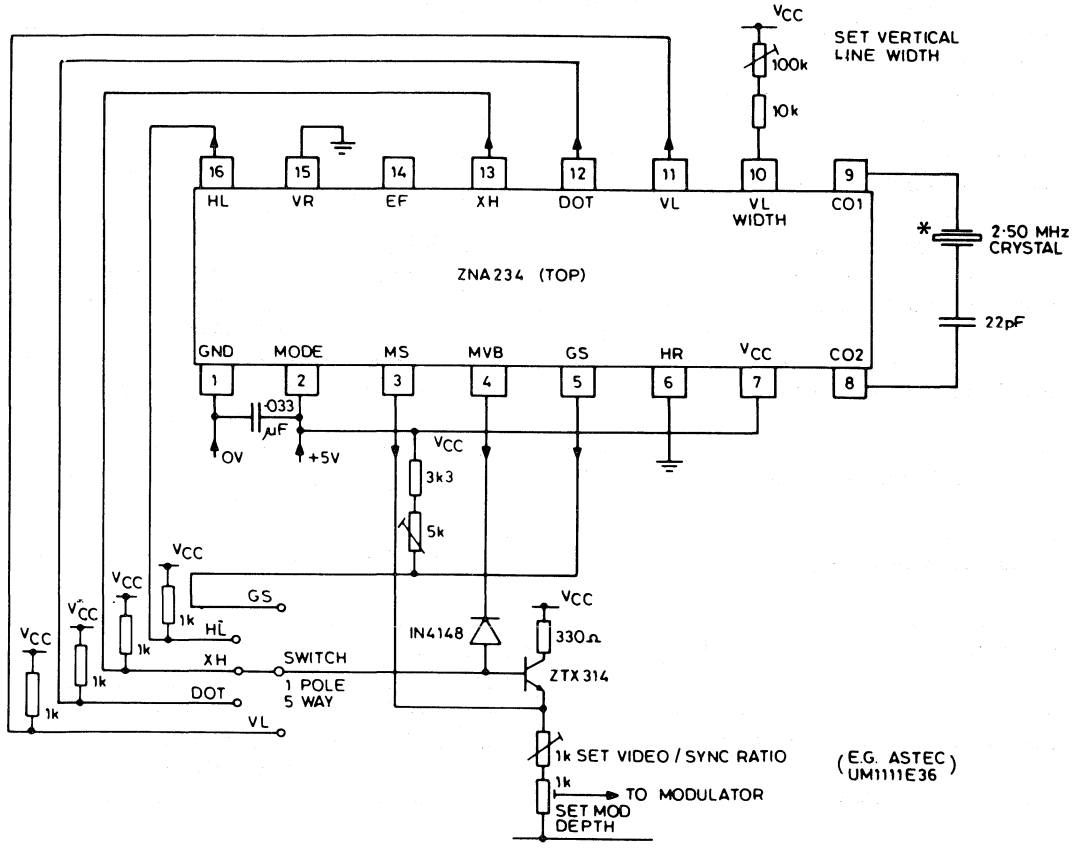
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{CC}	4.75	5.0	5.25	Volts	
Supply Current	I_S	–	135	–	mA	
High-level Input Voltage	V_{IH}	2.4	–	–	Volts	
Low-level Input Voltage	V_{IL}	–	–	0.8	Volts	
High-level Input Current	I_{IH}	–	–	40	μA	$V_{CC}=5V$, $V_I=2.4V$ (See Note 1)
Low-level Input Current	I_{IL}	−40	–	–	μA	$V_{CC}=5V$, $V_I=0V$ (See Note 1)
High-level Output Voltage	V_{OH}	2.4	–	–	Volts	$V_{CC}=5V$, $I_{Source}\leqslant 250\mu A$ (See Note 2)
Low-level Output Voltage	V_{OL}	–	–	0.5	Volts	$V_{CC}=5V$, $I_{Sink}\leqslant 5.0mA$ (See Note 2)
Clock Frequency	f_{clock}	– –	2.500 2.520	– –	MHz MHz	625 lines, Mode = '1' 525 lines, Mode = '0'
External Oscillator Pulse Width	t_w	150	200	250	ns	−ve going pulse, 625/525 lines

Note 1:
Input conditions only apply to mode input. For input conditions of oscillator inputs C01, C02, see applications section.

Note 2:
All outputs except greyscale, i.e. mixed sync, mixed video blanking, vertical lines, dots, crosshatch, even field and horizontal lines have internal 3k3 pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors, These should have a minimum value of 1 kΩ.

COMPLETE PATTERN GENERATOR USING THE ZNA234

(for detailed information see applications section)



*The following Companies can supply suitable crystals for use with the ZNA234

IQD
(Interface Quartz Devices Limited),
Crewkerne,
Somerset.
Tel: 0460 74433 Telex: 46283
Contact: Mr. Jarvis

McKnight Crystal Company,
Hardley Industrial Estate,
Hythe, Southampton.
Tel: 0703 848961 Telex: 47506
Contact: Mr. Carpenter

SEI
(Salford Electrical Instruments Limited),
Times Mill,
Heywood, Lancashire OL10 4NE
Tel: 0706 67501 Telex: 635106
Contact: Mr. P. Kenyon or Mr. D. Standring

OUTPUT INFORMATION AND WAVEFORMS

(a) **625 Lines** CCIR Timing (Mode=1)
Crystal Frequency = 2.50MHz
Line Frequency = 15.625kHz,
Line Period = 64μs
Field Frequency = 50Hz,
Field Period = 20ms.

Outputs
20 Horizontal Lines; 18 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

Crosshatch squares have approx. 1.4:1 aspect ratio (0.98" × 0.67" on 20" screen).

For timing diagrams see page 5.

(b) **525 Lines** EIA Timing (Mode=0)
Crystal Frequency = 2.520MHz
Line Frequency = 15.750kHz,
Line Period = 63.5μs
Field Frequency = 60Hz,
Field Period = 16.66ms.

Outputs
17 Horizontal Lines; 15 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

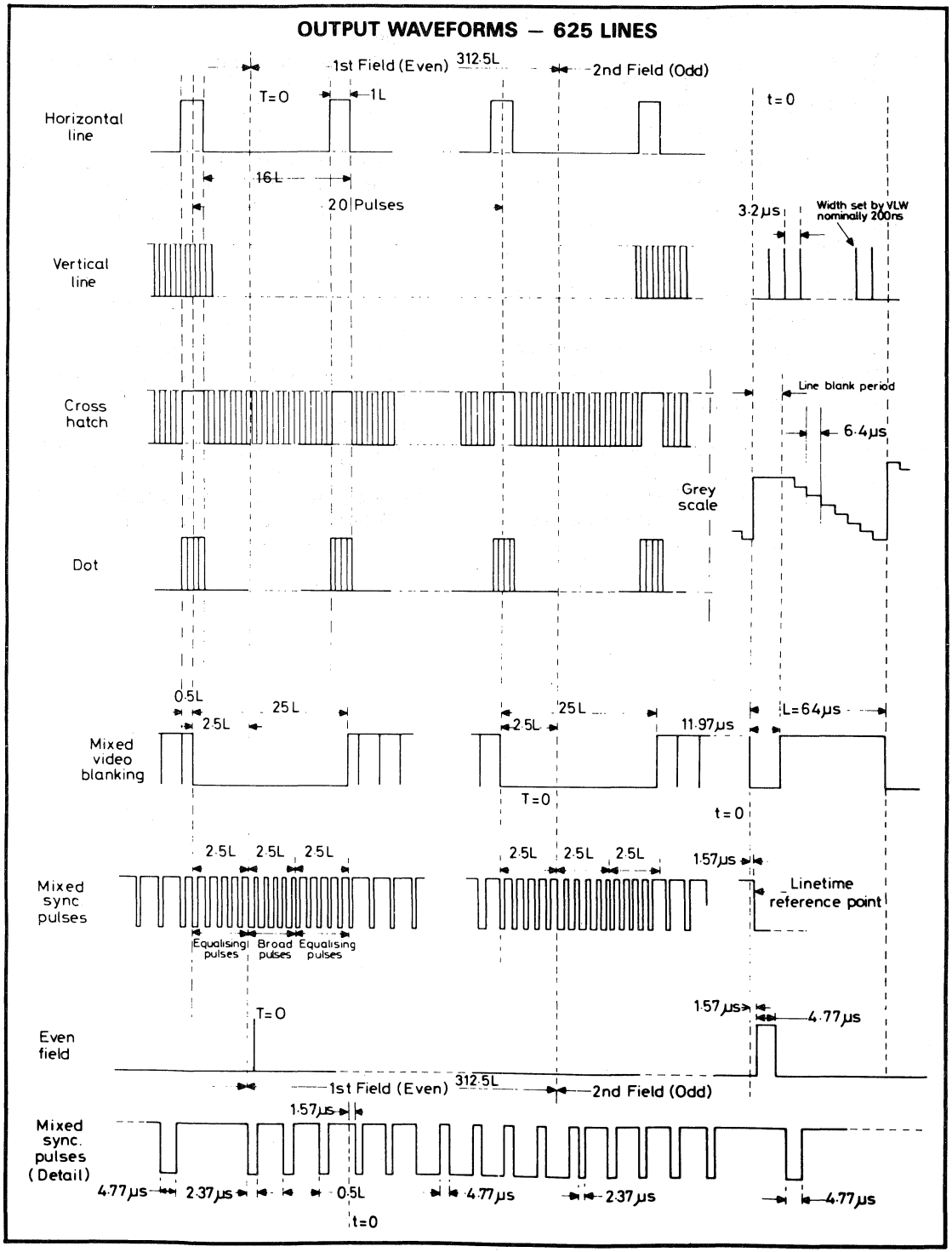
Crosshatch squares have approx 1. 2:1 aspect ratio (0.97" × 0.79" on 20" screen.)

For timing diagrams see page 6.

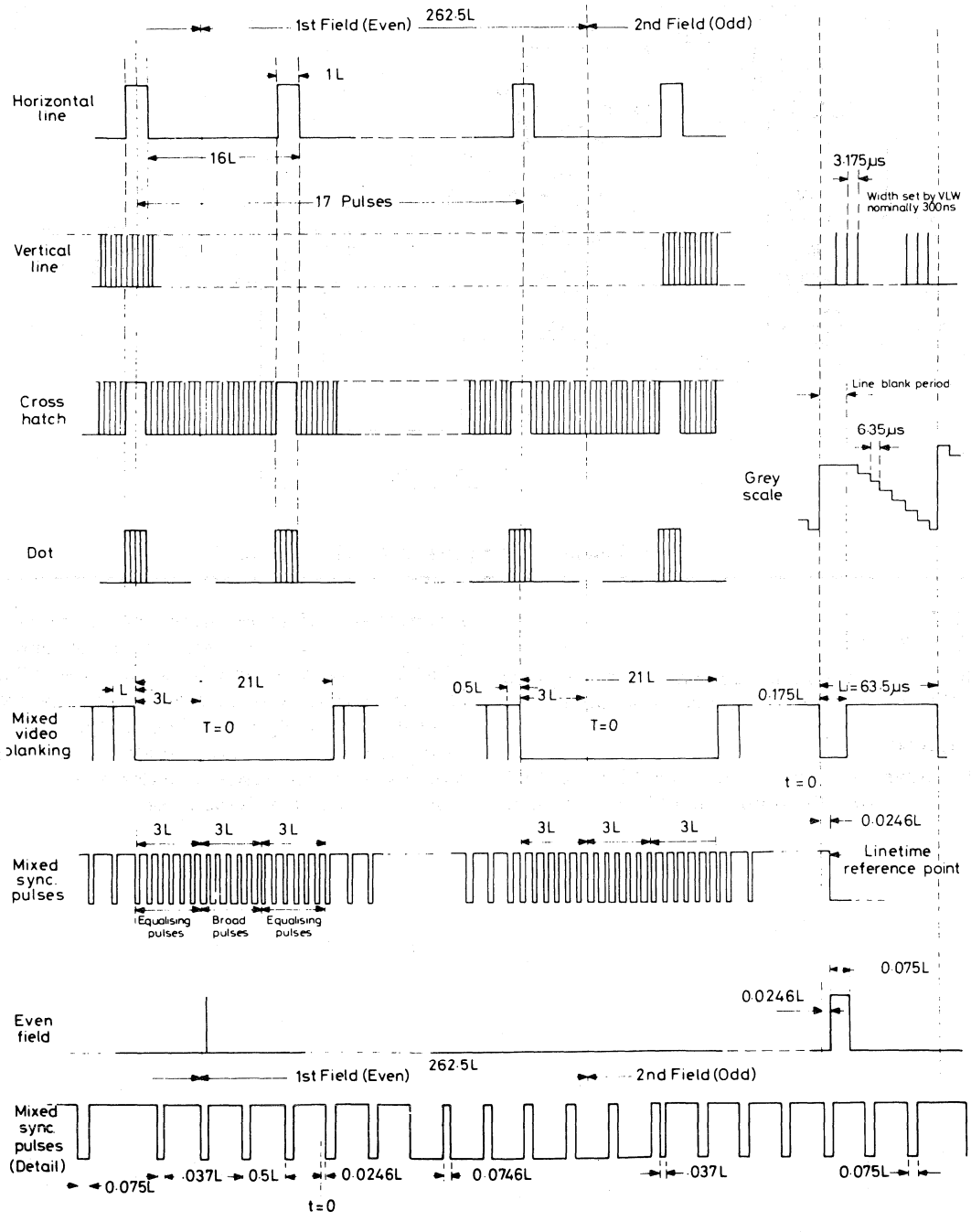
The horizontal line waveform consists of pulses 1 line wide occuring every 16 lines, producing horizontal lines 2 lines wide (owing to interlacing) on the screen. The vertical line waveform is a continuous series of pulses nominally 300ns wide occuring every 3μs (approximately). As these pulses occur in the same position in every line period the result is a series of vertical lines on the screen.

The two waveforms are fed to internal AND and OR gates to produce dot and crosshatch outputs respectively.

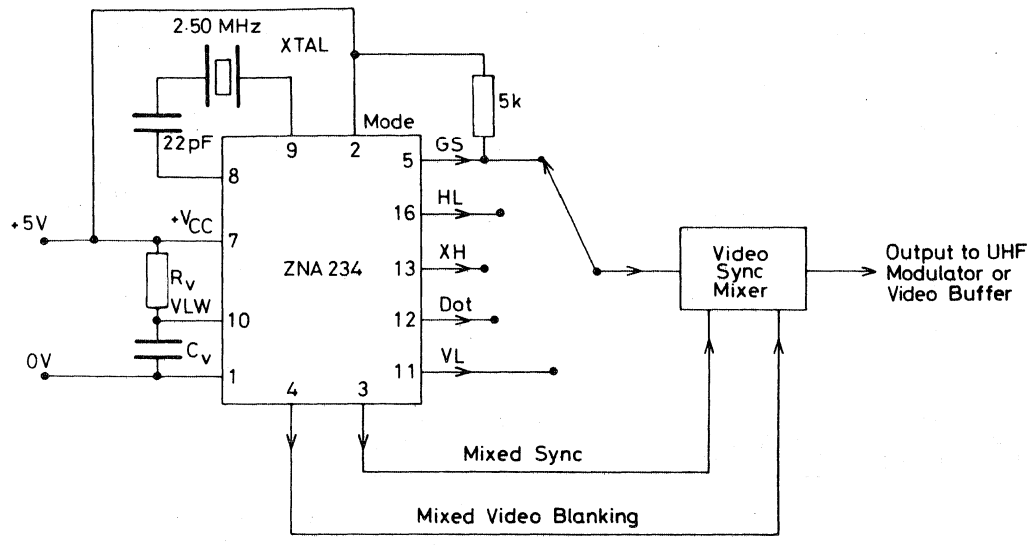
OUTPUT WAVEFORMS — 625 LINES



OUTPUT WAVEFORMS — 525 LINES



APPLICATION INFORMATION



T.V. Pattern Generator Using the ZNA234 (625 lines)

NOTES:

Mode, Pin 2

The mode input should be connected to V_{CC} for 625 lines or to 0V for 525 line operation.

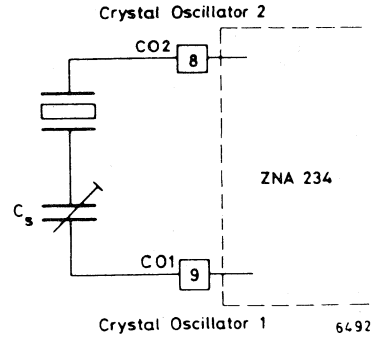
Greyscale, Pin 5

The greyscale output is produced by a D to A converter from the horizontal counter. The D to A converter is effectively a switched current sink providing 8 equal current steps of approx 60μA/step. When used with an external pull-up resistor, 8 voltage steps are produced (approx 0.3V/step with $R_L = 5K$). The output has a saturation level of approximately +2V and requires a buffer stage (emitter follower) to match into the video/sync mixer.

Oscillator. Pins 8 and 9.
The ZNA234 oscillator can be driven in several ways, depending on the application.

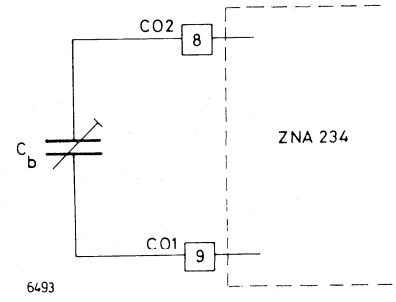
(a) Using external 2.50MHz crystal (625 lines mode)

Series
Resonant
Crystal



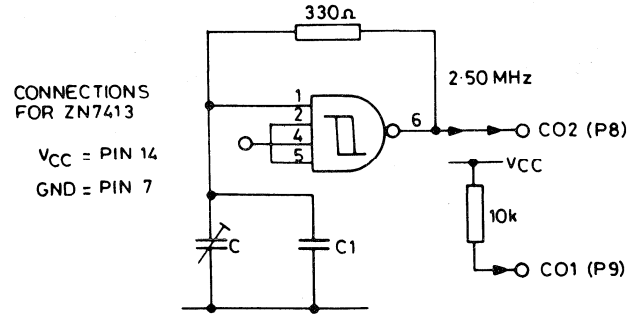
C_s is normally about 22pF

(b) If stability is not important, a capacitor may be used instead of the crystal.



$C_b \approx 15pF$

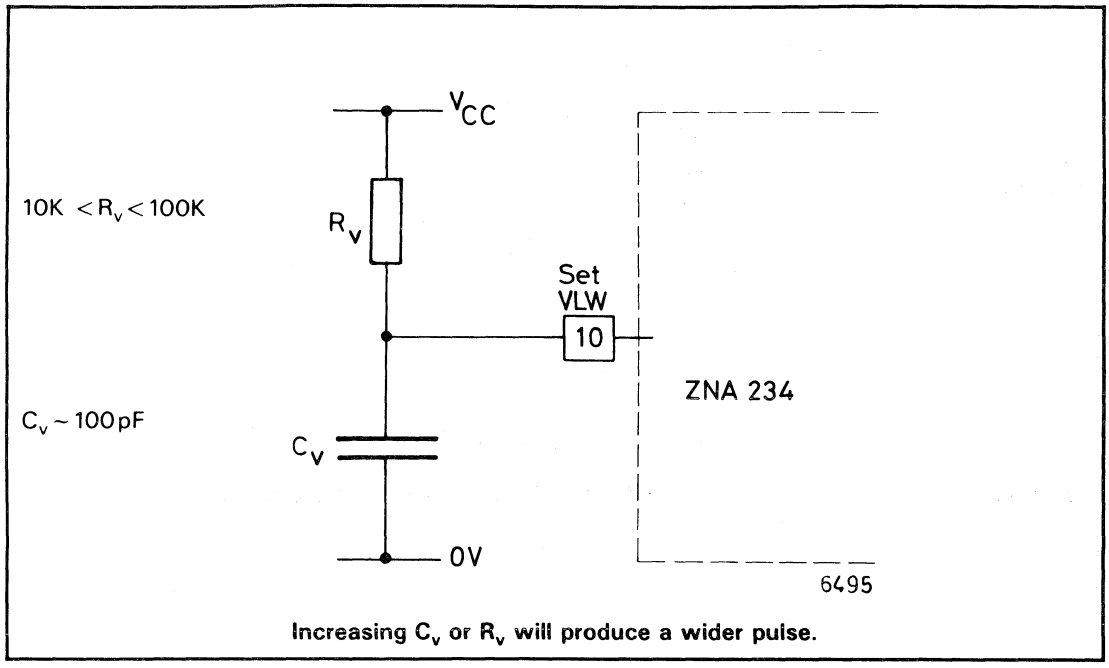
(c) Alternative oscillator circuits.



The external oscillator pulse width t_w, must be within the range shown in the table on page 2.

Vertical Line Width, Pin 10

Provision has been made for the width of the vertical lines to be varied if required. With pin 10 open circuit, the width of the vertical line pulses generated by the device is approximately 300ns. The pulse width may be varied from 100ns to 1μs by connecting a capacitor and resistor to pin 10 as shown below.



Increasing C_V or R_V will produce a wider pulse.

N.B. If pin 10 is left open circuit to give a 300ns pulse width, any external capacitance on the pin (e.g. from long lead or p.c.b track) will affect the timing. It is, therefore, recommended that if pin 10 is to be left open circuit then no connection at all is made to it.

Test Inputs, Pins 6 and 15

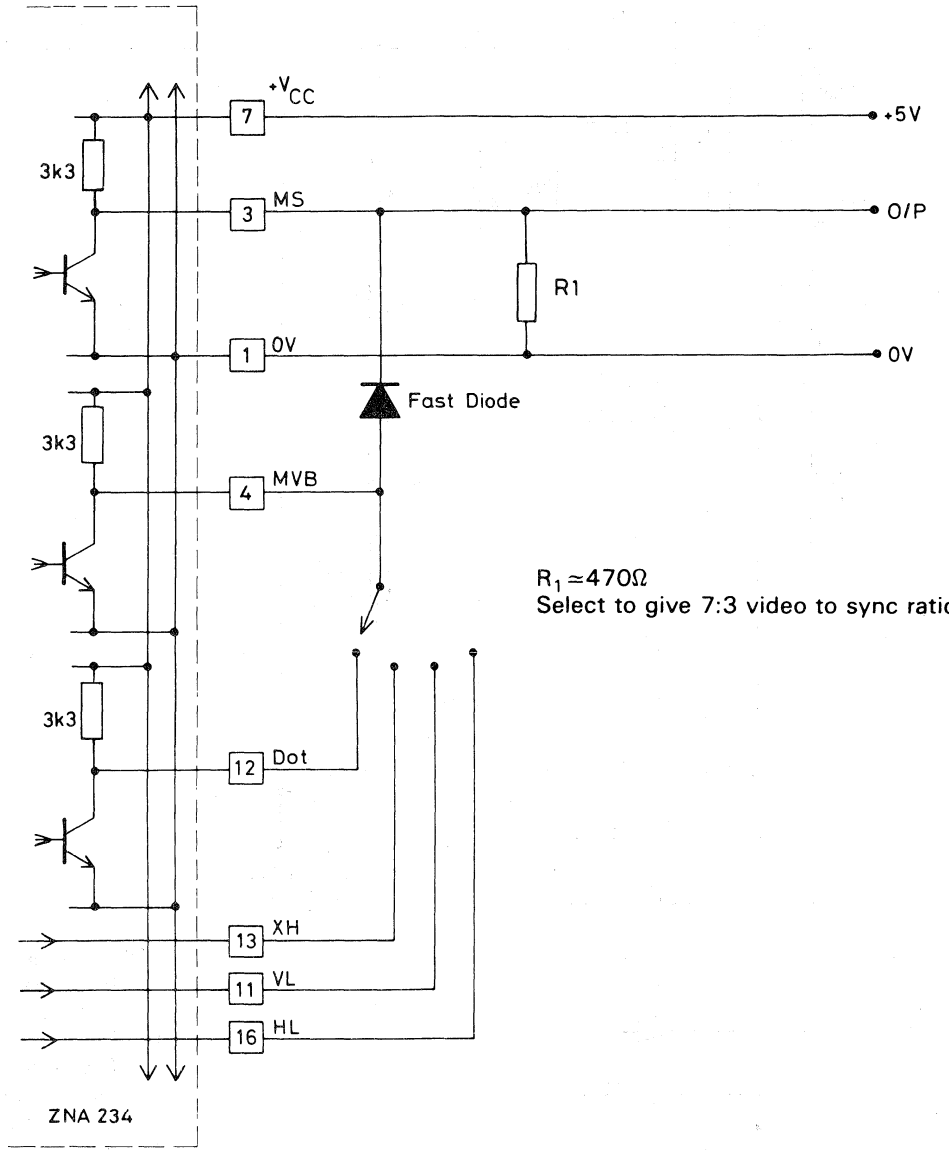
These should be connected to 0V.

Circuits for Video/Sync Mixer

The following two circuits on pages 10 and 11 for the video/sync mixer are suggested as starting points only. They have been found to work on the bench, but no detailed applications work has been carried out to date.

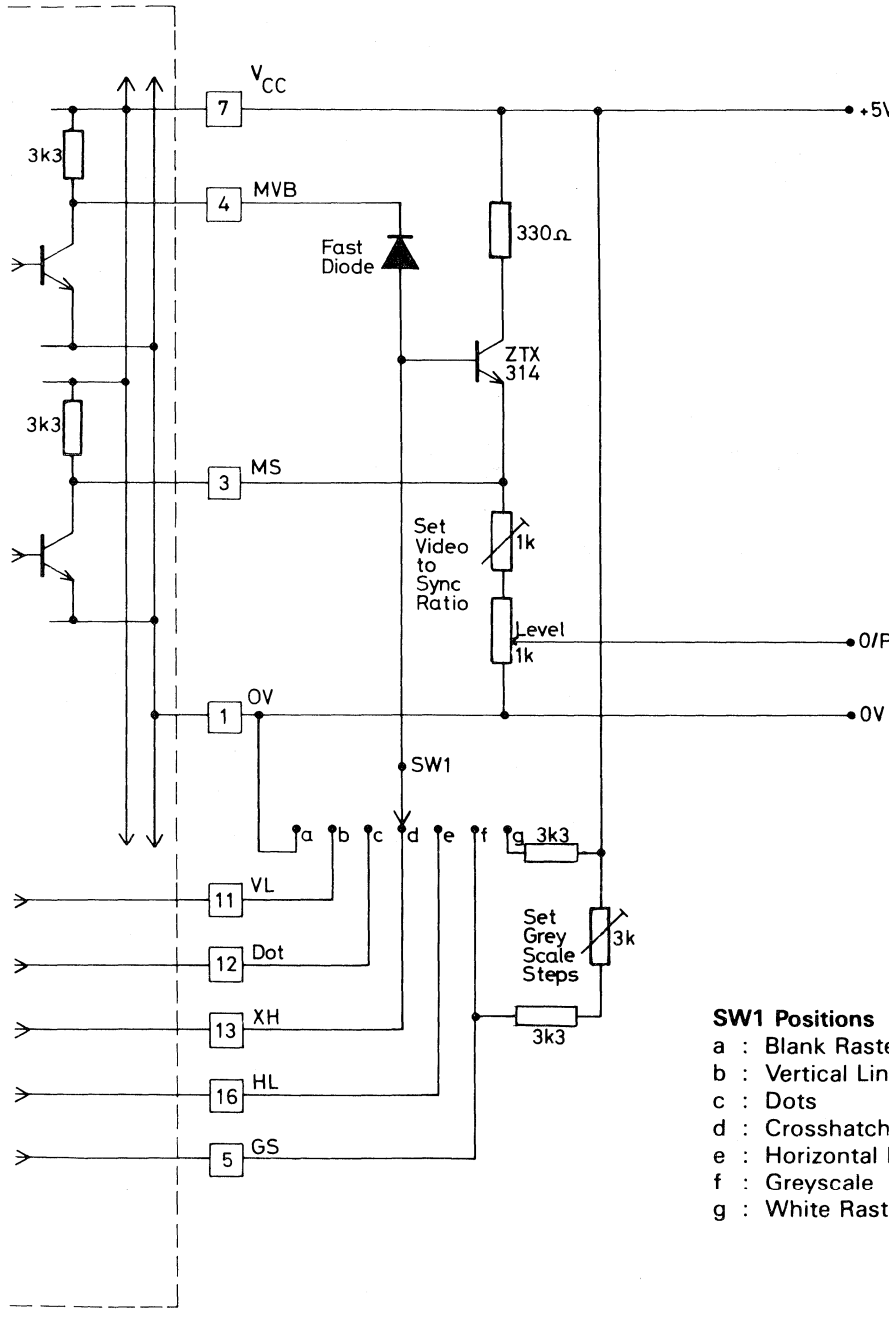
The circuit on page 10 is probably the simplest possible method, but it does have the disadvantage that the Greyscale output cannot be used owing to its different d.c. levels compared with the other video outputs. The second circuit, page 11, is hardly any more complex, and does allow the use of the Greyscale output.

SIMPLE CIRCUIT FOR VIDEO/SYNC MIXER (NO GREYSCALE)



$R_1 \simeq 470\Omega$
Select to give 7:3 video to sync ratio.

CIRCUIT FOR VIDEO/SYNC MIXER ALLOWING USE OF GREYSCALE



SW1 Positions

a : Blank Raster
b : Vertical Lines
c : Dots
d : Crosshatch
e : Horizontal Lines
f : Greyscale
g : White Raster

ZN454E

TRIPLE 4-BIT VIDEO D-A CONVERTER

The ZN454 consists of three 4-bit D-A converters, providing a colour palette of 4096 possible display colours. The required logic translators, control logic, a reference voltage source and reference amplifier are also integrated on-chip.

Each D-A converter accepts 4-bit digital video data and SYNC/BLANK signals directly from a TTL source and produces a composite video output to directly drive a 75Ω line terminated by a 75Ω load at both ends.

The ZN454 is ideally suited for pixel colour generation in graphics display systems requiring 4-bit colour resolution. The high linearity of each DAC ensures excellent colour contrast and the fast update rate allows the device to be interfaced to monitors with a resolution of up to 1024 x 1280 pixels assuming a standard refresh rate of 60Hz.

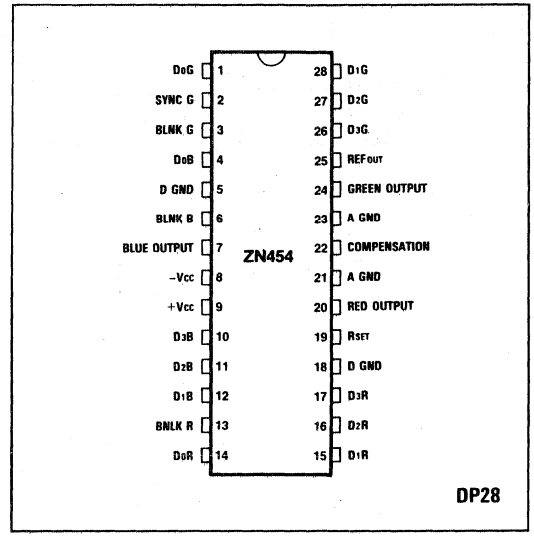


Fig.1 Pin connections - top view

FEATURES

- 3 Video DAC's - Ideal for Colour Graphics
- Fast, 8ns Settling Time
- Update Rates to 100MHz
- Low Glitch Energy
- ¼ LSB Linearity Error
- On-Chip Reference Source
- Composite Sync and Blank Inputs
- TTL Compatible Inputs
- Generates Standard Video Signal Output Across a Doubly Terminated 75 Ohm Load
- 28 Pin DIL Package

GENERAL CIRCUIT DESCRIPTION

Each D-A converter of the ZN454 uses high speed switches to steer current from precision current sources to either analog ground or to the analog output - as governed by the digital inputs (see Fig.4). The analog output voltage is now obtained from these weighted current sources producing the desired voltage drop across the 37.5Ω load impedance. The gain of the D-A converters is adjustable via RSET.

Since the ZN454 utilises current output DAC's the output impedance is inherently high. Thus a 75Ω resistance is required (adjacent to each DAC output) to shunt this high impedance and provide the correct impedance for driving a 75Ω line terminated in 75Ω at the monitor. The desired 1V p-p composite signal will now be developed across this effective 37.5Ω output impedance.

The grey scale output current of each DAC has 16 levels from 0 to -17mA nominally (see Fig.3). This develops 16 levels of output voltage from 0 to -643mV across the specified 37.5Ω load impedance. the 'REFERENCE WHITE' level (0V) corresponds to the digital input code 1111 and the 'REFERENCE BLACK' (-643mV) to 0000.

A logic '1' on the BLANK input overrides the data inputs and drives the output to 71mV more negative than the 'REFERENCE BLACK' level. This corresponds to the 'BLANKING' (or 'blacker-than-black') level.

Activating the SYNC input (logic '1') with the BLANK input 'high' drives the output to 286mV more negative than the 'BLANKING' level. This voltage (nominally -1V) corresponds to the 'SYNC' level.

GAIN ADJUSTMENT (RSET)

RSET provides a means of adjusting the current in the weighted current sources. An amplifier compares the voltage developed across RSET, with the reference voltage. If RSET is increased/decreased the amplifier output causes the current through RSET to decrease/increase (to bring the voltage across RSET back in line with the reference voltage). This also causes the current in each of the current sources to decrease/increase (see Fig.3). In this manner the magnitude of the output waveform can be varied to obtain the desired levels.

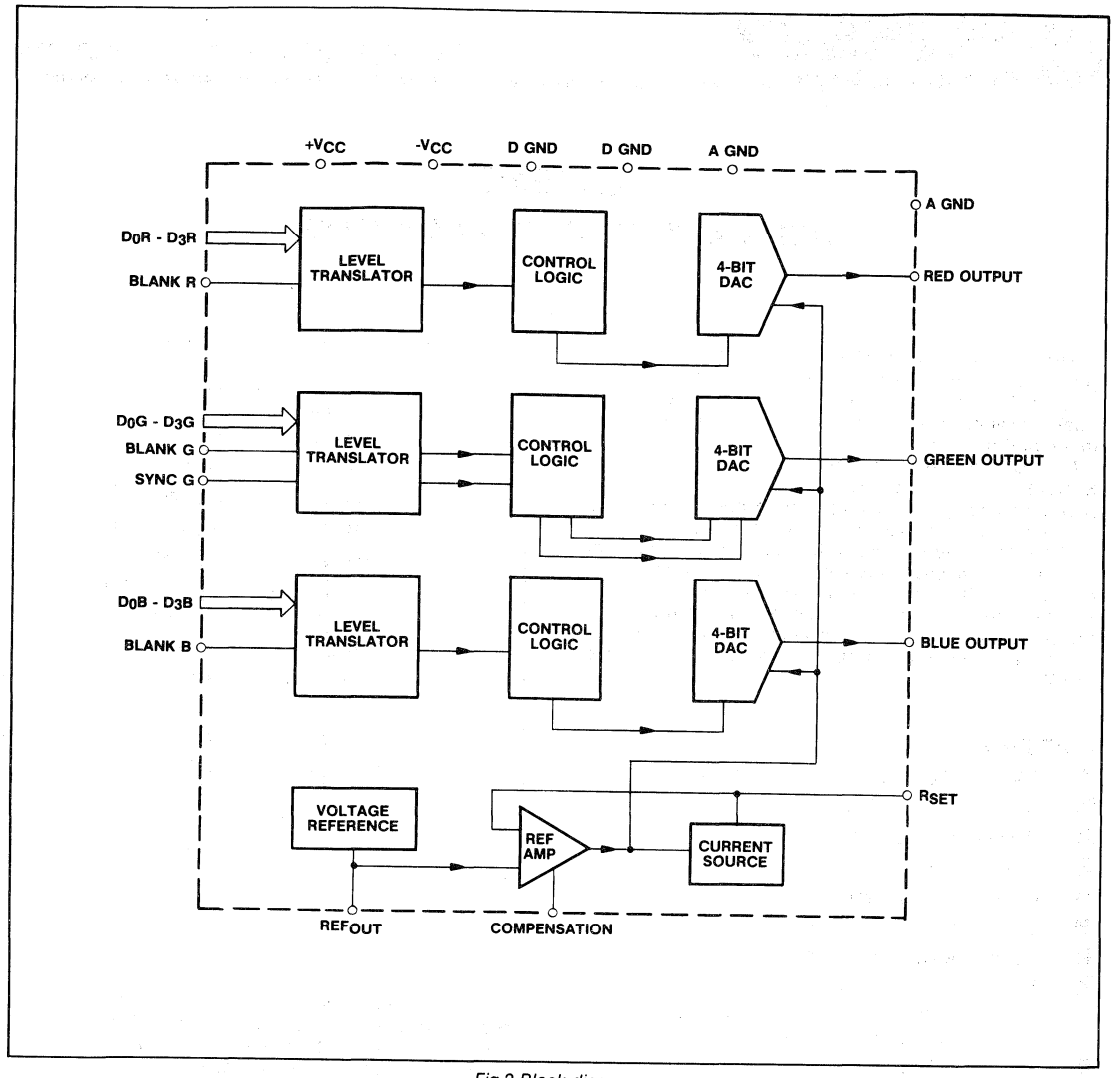


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $+V_{CC}$	+6V
Supply voltage, $-V_{CC}$	-6V
Logic input voltage	$+V_{CC}$
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_{CC} = ±5V, R_L = 37.5Ω and R_{SET} = 180Ω

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Resolution		4			Bits	
LSB weight (current)			1.13		mA	Note 1
LSB weight (voltage)			43		mV	
Accuracy						
Linearity error			±0.25	±0.5	LSB	
Differential linearity error				±0.5	LBS	Note 2
Offset error			-5.0	-15.0	mV	
Gain error				±5	% of nom.FSR	
Speed performance - Grey scale output						
Rise/fall times (voltage)			3	5	ns	10-90% of final value
Settling time (voltage)			8		ns	Note 3
Maximum update rate			100		MHz	Note 4
Slew rate			180		V/μs	10-90% of final value
Glitch energy			60		pV-s	Note 5
Temperature coefficient						
Offset			10		ppm/°C	Measured with
Gain			500		ppm/°C	internal reference
Data, sync and blank inputs						
Logic compatibility			**TTL**			
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}			0.8	V	
High level input current	$I_{IH(1)}$			+20	μA	V_{CC} = max, V_{in} = 5.5V
	$I_{IH(2)}$			±10	μA	V_{CC} = max, V_{in} = 2.4V
Low level input current	I_{IL}			-1.6	mA	V_{CC} = max, V_{in} = 0.4V
Coding (see Fig.2)			**Complementary binary**			
Output - Grey scale						
Voltage range			0.64		V	Note 1
Current range			17		mA	
Output - Composite sync						
Voltage range			286		mV	
Current range			7.6		mA	
Output - Composite blanking						
Voltage range			71		mV	
Current range			1.9		mA	
Output voltage compliance		0		1.5	V	
Internal voltage reference						
Output voltage	V_{REF}		-1.26		V	
Output voltage tolerance				±3.0	%	
Output voltage TC			200		ppm/°C	0°C to 70°C
Power supply requirements						
Supply voltage	+V_{CC}	4.5	5.0	5.5	V	
	-V_{CC}	-4.5	-5.0	-5.5	V	
Supply current	+I_{CC}		22.5		mA	
	-I_{CC}		136.0		mA	

NOTES
1. LSB and full-scale output levels adjustable with R_{SET}. 2. Monotonicity guaranteed over full operating temperature range.
3. The settling time was measured as the time between the start of the output rising/falling edge to where the output entered and remained within ±½ LSB of the final value. The value quoted is for a transition from reference white to reference black and vice versa, and does not include the inherent input propagation delay (2-3ns). See section describing settling time measurement.
4. The maximum update rate is limited by the full-scale settling time to rated accuracy.
5. Measurement of glitch energy is discussed in a later section of this data sheet.

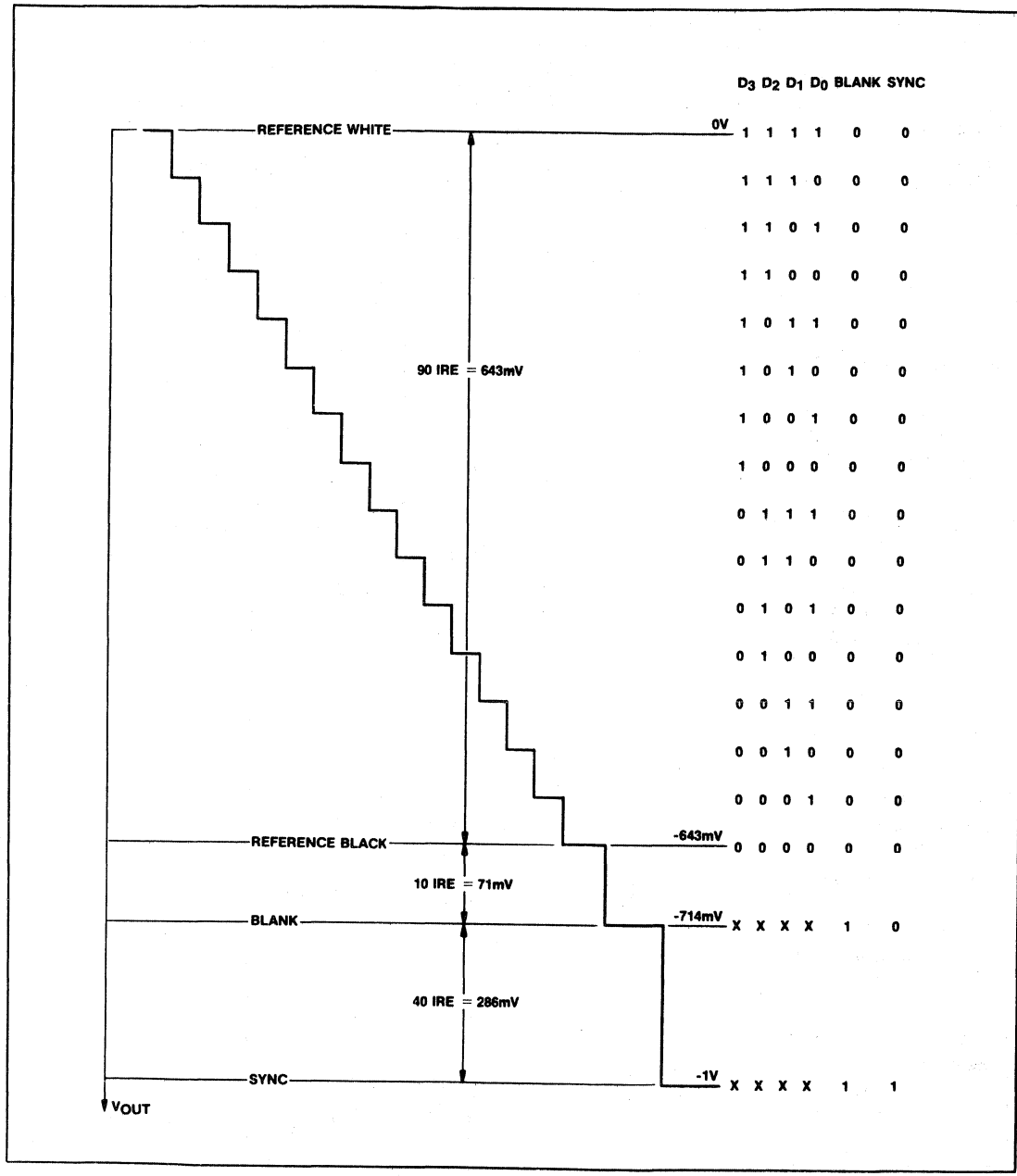


Fig.3 Typical composite video output waveform

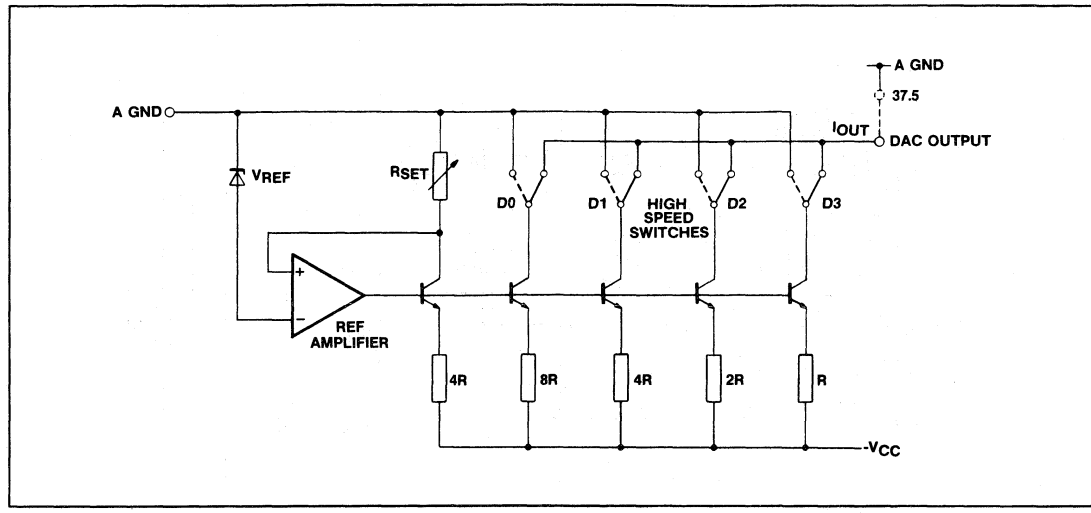


Fig.4 Current source array (schematic)

DIGITAL INPUTS

The digital inputs are high speed level translators (see Fig.5).

The ZN454 requires very few external components for normal operation. Fig.6 illustrates the external component connections.

LAYOUT CONSIDERATIONS

When using the ZN454, as with any other device of this kind, certain precautions must be taken to obtain the best performance.

Some of the requirements are:

1. A ground plane board providing a good earth and with good power supply connections, to keep noise to a minimum.

2. Good decoupling - especially around all the fast switching circuits - including a 0.1μF capacitor from both the +5V and -5V supplies positioned close to the ZN454. The ground connections for these capacitors should be adjacent.

3. Some physical separation between the digital input tracks to minimise crosstalk.

4. Matched digital input signal paths to avoid introducing any unnecessary time skew between the inputs. This would cause glitches on the DAC outputs with changing codes. Also the outputs from the driving device will have to be well matched for the same reason.

5. 75Ω resistors close to the DAC outputs, to provide the correct impedance for driving 75Ω lines.

SETTLING TIME AND GLITCH ENERGY MEASUREMENT

In a finished design the ZN454 would be soldered directly into the board to obtain the best performance possible. However for evaluation purposes a socket really needs to be used. This will give some degradation in performance but useful results can still be obtained.

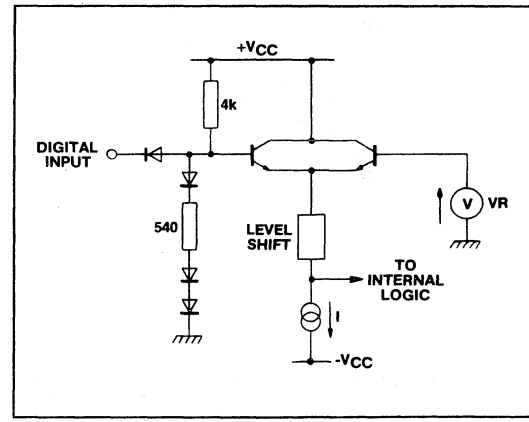


Fig.5 Equivalent circuit of sync, blank and data inputs

Measurement of settling time and glitch energy is not a straightforward task and all of the recommendations previously noted must be adhered to. If these parameters are to be measured using an oscilloscope, great care must be taken to avoid corrupting the analog outputs e.g. conventional probes cannot simply be clipped onto the outputs as this would cause reflections giving rise to errors. Instead the ZN454 needs a 75Ω termination near the chip, a 75Ω cable - also grounded close to the chip - connecting to a 75Ω lead through termination at the oscilloscope. Optimum cable length is about 6 inches but it may need trimming around this. Also the oscilloscope obviously needs to have sufficient bandwidth to cope with the rise and fall times encountered.

The digital circuits driving the DAC's must not introduce too much noise, or time skew between the bit inputs. This

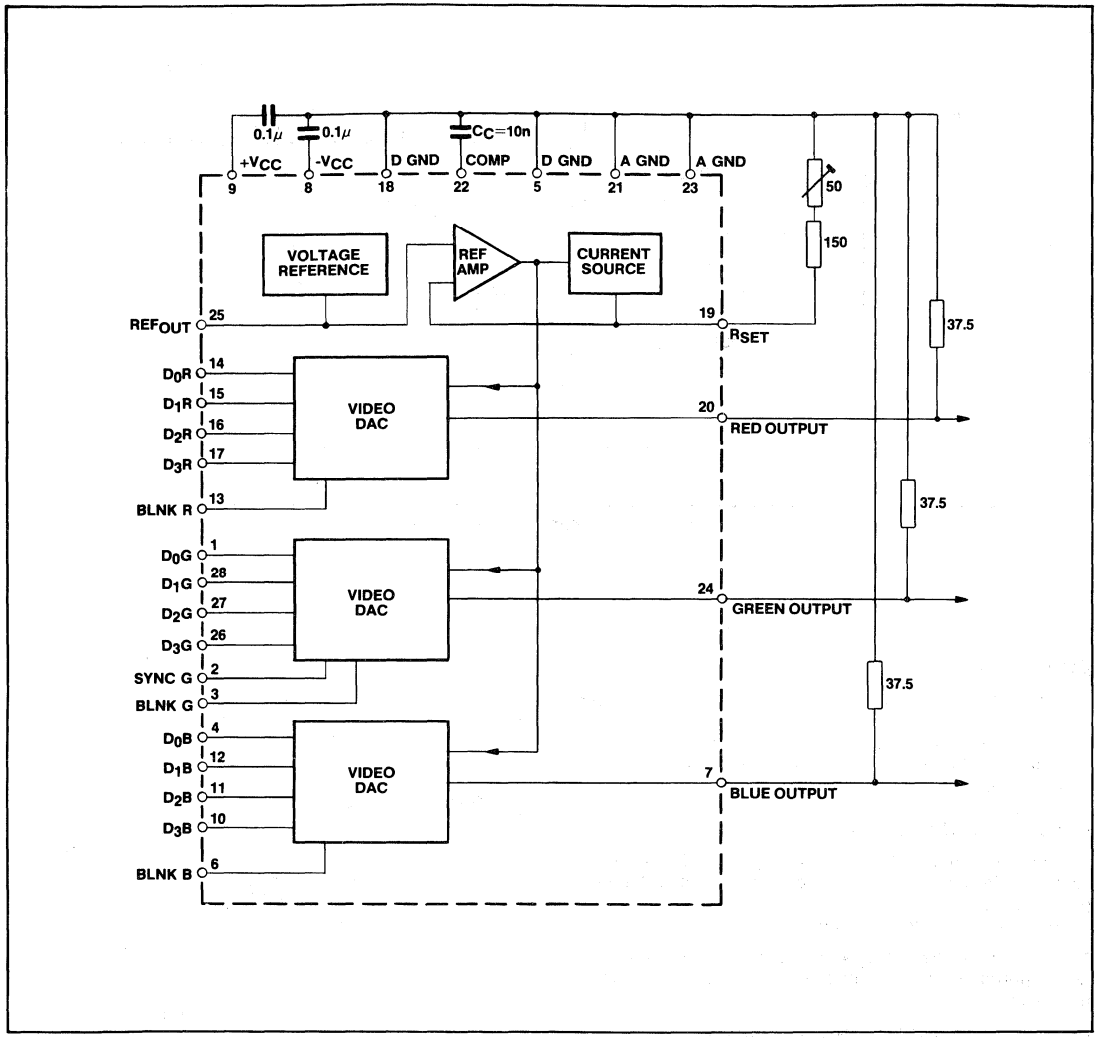


Fig.6 External component connections

can considerably affect the results. However, a convenient way of minimising these problems for evaluation purposes, is to drive the digital inputs directly from a pulse generator. Full-scale transitions of the grey scale can now be monitored by wiring the inputs to a given DAC in parallel (terminating in 50Ω) and clocking with the pulse generator. Each output can now be examined in turn. The circuit diagram is as in Fig.6 except that the sync and blank inputs will be tied low. The 37.5Ω terminations on the DAC output, and the digital input signals are provided as described above. Fig.7 shows an actual full-scale (grey scale) output transition measured using the above procedure, giving a settling time of 5.12ns.

Glitch energy measurements, at the major transition for example, can also be measured by driving the digital inputs directly from a pulse generator but it will need to have well matched complementary outputs. Also the lead lengths from the generator to the digital inputs will have to be well matched (and terminated in 50Ω). This is so because this measurement is especially critical of any time skew between the input signals. Indeed even an ideal DAC would produce glitches if there were timing differences between these changing input signals. These time skew errors which would manifest themselves as exaggerated glitches on the DAC output, are referred to the point at which the input signals cross the digital input thresholds (≏1.5V nom.). Thus the characteristics of the driving signals will have some effect on the amplitude of the glitches, which may be minimised by careful design. The circuit arrangement for measuring the glitch energy is as above but with the digital inputs being switched through different codes. Fig.8 shows an actual mid-scale glitch, measured using the above procedure.

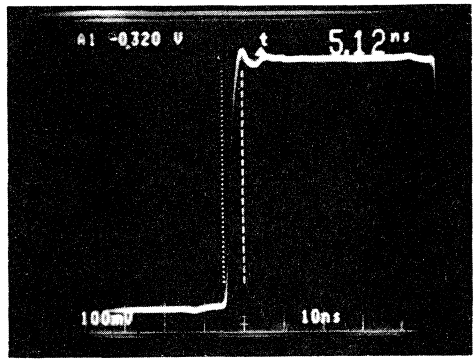


Fig.7 Full-scale output transition - settling time

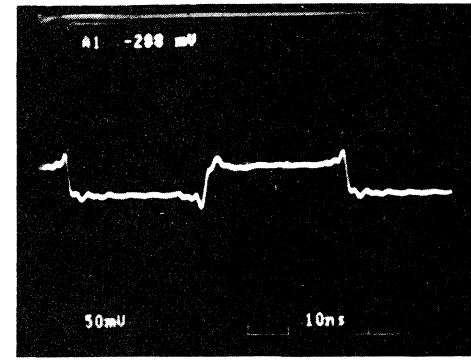


Fig.8 Mid-scale output glitch

GLOSSARY OF VIDEO TERMS

Raster scan

The method of sweeping a CRT one line at a time to generate and display images.

Composite video signal

The VIDEO signal plus the BLANK and SYNC signals.

Video signal

The portion of the composite VIDEO SIGNAL which varies in grey scale levels between 'reference white' and 'reference black' - this is the portion which is visually observed.

Sync signal

The portion of the video waveform that synchronises the raster scanning process.

Grey scale

The discrete levels between and including 'reference white' and 'reference black' - there are 16 levels for a 4-bit DAC.

Blanking level

The level separating the SYNC portion from the VIDEO portion. Usually referred to as the FRONT PORCH or BACK PORCH, this is the level which will shut off the electron guns resulting in the blackest possible display.

Sync level

The negative peak level of the sync signal.

Reference black level

The maximum negative level of the VIDEO signal.

Reference white level

The maximum positive level of the VIDEO signal.

Application Notes

Satellite Receiver Design

The start-up phase of engineering developments is often characterised by a multiplicity of opinions and solutions to the problem, adding great interest but not a little confusion to the subject. In the course of time the situation clarifies with one or two solutions gradually gaining wide acceptance due to their simplicity and cost effective nature. Such is the situation in the satellite receiver market at the present time, where standards are few and far between with even transmission characteristics differing from one broadcast company to another, but with a trend towards a more standard receiver emerging.

In order to simplify the situation, only the single conversion and block conversion systems will be discussed here although much of the applications information and most of the products will be appropriate to other situations.

SINGLE CONVERSION RECEIVERS

The simplest form of receiver is probably the single conversion type shown in Fig.1. Here, the incoming signal is amplified and mixed with the local oscillator signal to produce a lower intermediate frequency in a similar manner to a conventional TV. Unfortunately both the amplifying and mixing processes have to be performed close to the dish, the first due to noise considerations, the second because it is not economic to transmit the high frequencies used in satellite reception via a relatively long coaxial cable.

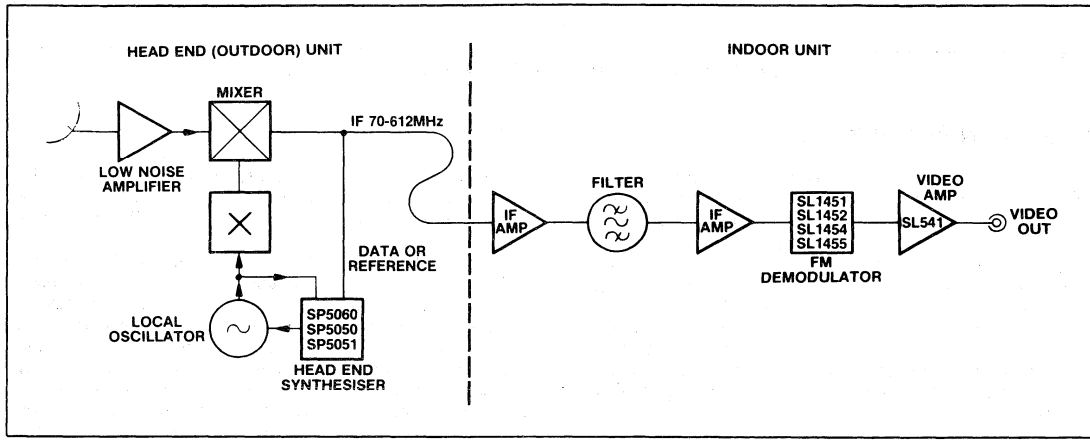


Fig.1 Simplified block diagram of single conversion receiver

The intermediate frequency is received by the indoor unit where an IF filter passes only the required signal to the FM demodulator. The choice of this intermediate frequency is one of the main areas of disagreement between designers, some using the existing 70MHz standard used in microwave link communications, but others adopting various higher frequencies up to 612MHz, making use of the low cost demodulators, SAW filters and amplifiers becoming available for these frequencies.

Now that the high cost objections to high IF usage have been overcome, other technical advantages, such as greater demodulator linearity (due to the lower percentage deviation) and simpler receiver design (because the inherently higher image rejection makes tracking filters unnecessary), will eventually ensure the universal adoption of high intermediate frequencies.

Design of single conversion receivers is complicated to some degree because programme selection is determined at the head end, requiring in the simplest case of a non-synthesised receiver, a variable DC tuning voltage to be passed from the indoor to outdoor units.

This will probably require an additional cable, because the DC power supply for the head end unit will already be carried by the signal coax. Where synthesised tuning is required the situation is additionally complicated as digital tuning information or a variable frequency reference must be transferred to the head end. Because the programme selection is determined at the receiver head end, the single conversion receiver has the disadvantage that reception of only one signal is possible from a dish, removing the possibility of watching alternative programmes in different rooms of a house and making the system unsuitable for feeding apartment blocks or hotels.

BLOCK CONVERSION RECEIVER

The block converter type of receiver shown in Fig.2 overcomes most of the disadvantages of the single conversion type by using a fixed frequency local oscillator at the head end. By this method all the available signals in the satellite band sharing the same polarisation are down-converted to an intermediate frequency usually ranging from 950MHz to 1450MHz or 1750MHz for transmission to the indoor unit. this technique transfers programme selection to the indoor unit and so removes the need for data or reference transmission to the head end. The technique also allows connection of several receiver units tuned to different signals and provides good image rejection due to the use of a relatively high IF. Programme selection is obtained by further down-converting the required signal to a fixed second IF using a voltage controlled local oscillator. A SAW filter or other type of bandpass filter is used at this point to reject unwanted signals. The choice of second IF is flexible as in the case of the single conversion receiver, with the same arguments causing a trend towards the use of higher frequencies.

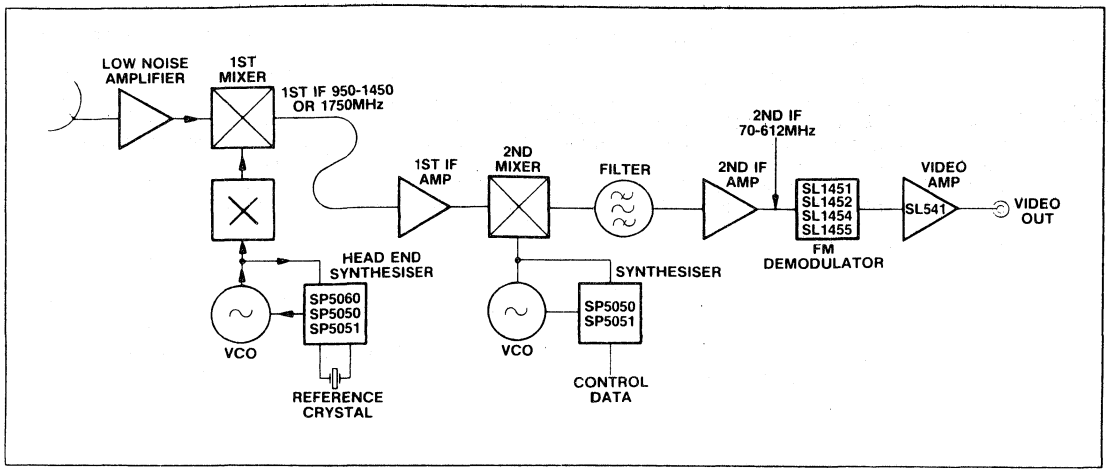


Fig.2 Simplified block diagram of block conversion satellite receiver

SIGNAL TO NOISE THRESHOLD

In a frequency modulated system, as used in satellite TV reception, the demodulated signal to noise ratio decreases linearly with decreasing carrier to noise ratio before demodulation, until a level known as the threshold point is reached. Below the threshold point, the output signal to noise ratio decreases rapidly, producing short duration high amplitude impulses which in the context of TV reception manifest themselves as light or dark spots on the picture commonly known as 'sparklies'. The threshold is defined as that point where the output signal to noise ratio departs by 1dB from the straight line relationship with the input carrier to noise ratio.

THRESHOLD EXTENSION

In an ideal world, the best method of obtaining a perfect picture at all times would be to ensure a good carrier to noise ratio under all reception conditions by using an adequate receiving dish, but in urban situations or in fringe areas, the size of dish required might be unacceptable and some method of extending the threshold point of the detector is desirable.

Although in many cases some form of threshold extension will be found necessary to achieve the required receiver performance, it should be noted that (as is often the case in engineering) improved performance in one direction means a compromise in another. Threshold-extended FM demodulators are no exception, and unless carefully designed, problems such as picture tearing on fast black to white transitions can occur. Although threshold extension techniques can successfully delay the onset of sparklies, under poor carrier to noise ratio conditions the effect **will** occur, generally producing noise pulses of longer duration than those from an unextended demodulator such as the SL1452.

Frequency Synthesiser Applications

SP5060 2GHz FREQUENCY SYNTHESISER

In the block converter type of receiver shown in Fig.2, the local oscillator signal to the first mixer is a fixed frequency and is often controlled by a dielectric stabiliser. A more stable control of frequency may be obtained by using a phase locked loop synthesiser with crystal reference, such as the SP5050 or SP5051. Although either of these products could be used in such an application, the need for a 16-bit input word to select the operating frequency is a disadvantage when the device is situated at the remote end of the receiver downlead. Local generation of the necessary data word using CMOS logic elements or sending a suitably coded data word along the downlead are possible solutions to the problem, but it may be simpler to use the SP5060 fixed frequency synthesiser. The SP5060 can synthesise any frequency in the range 300MHz to 2.0GHz when fed with the appropriate reference.

The C-band satellite signals cover the range from about 3.67 to 4.17GHz and using a frequency doubling mixer with low side oscillator injection, down conversion to the 950-1450MHz standard IF range will occur if the oscillator frequency is set at 1.36GHz. Since the multiplication ratio between the local oscillator and the reference input to the SP5060 is 256, a 5.3125MHz crystal reference will be required, as shown in Fig.3. A similar system but with a much greater degree of local oscillator multiplication could be used in a block down converter for 12GHz DBS reception.

The SP5060 can also be used for head end tuning in single conversion receivers by feeding a variable reference frequency along the downlead from the indoor unit. Since the reference is at a very different frequency from the IF the two can be easily separated with a minimum of filtering.

The variable reference frequency for this type of system is best generated using a low frequency synthesiser contained in the indoor unit, and a system using the Plessey NJ8820 is shown in Figs. 4 and 5.

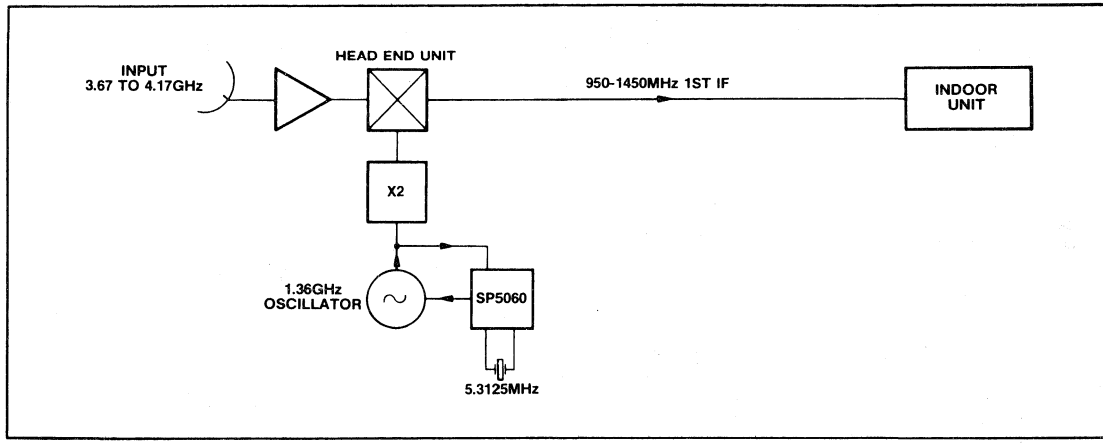


Fig.3 Synthesised block down converter system

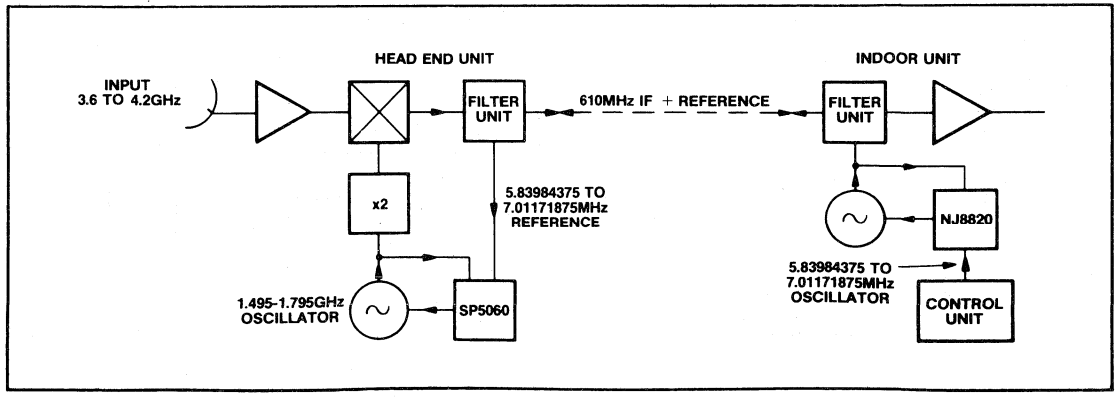


Fig.4 Block diagram of synthesised single conversion receiver

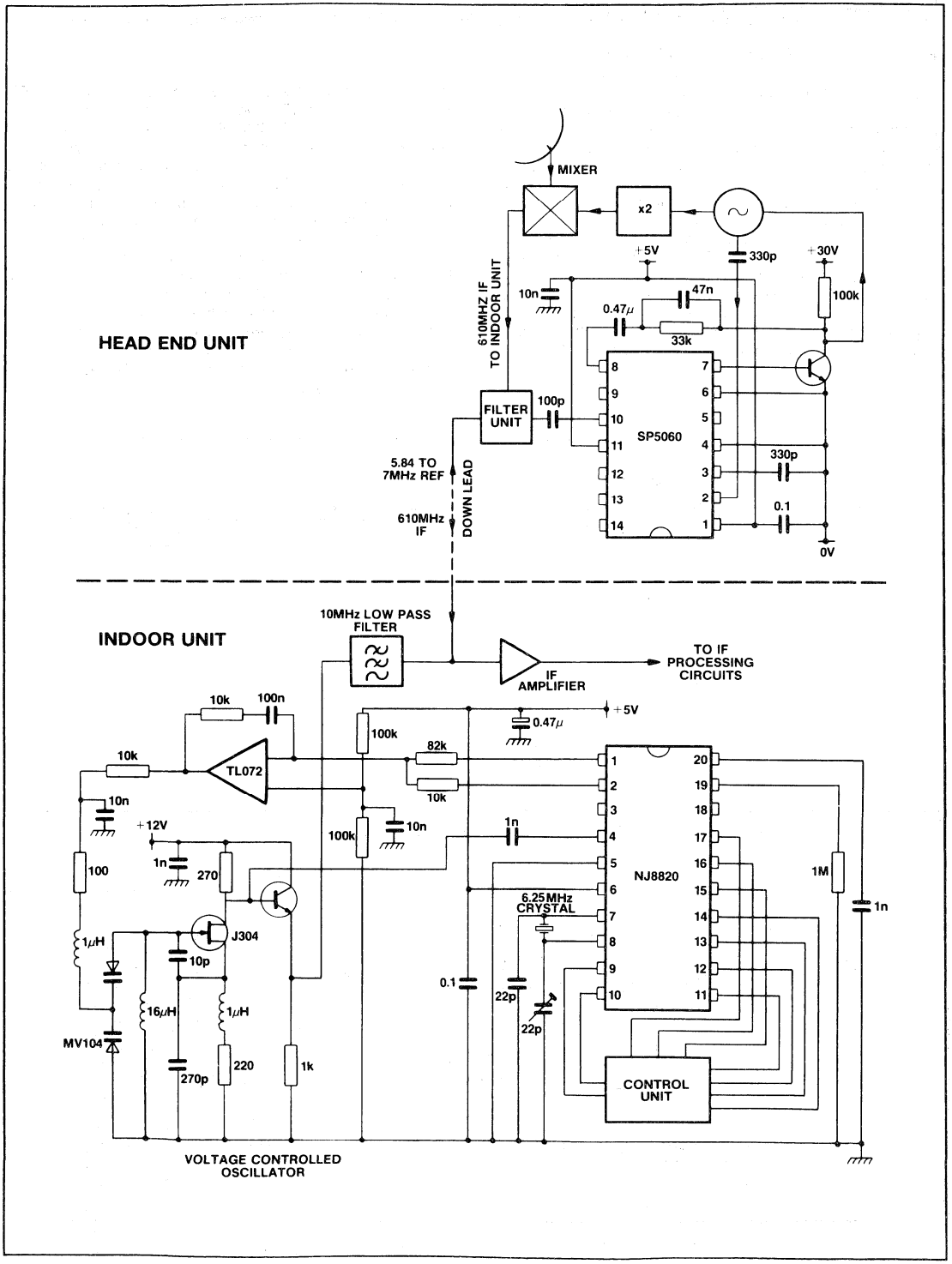


Fig.5 Circuit of double synthesiser

Using a frequency doubling mixer or x2 multiplier and assuming a 3.6 to 4.2GHz tuning requirement, 610MHz IF and a low side local oscillator, the required oscillator frequency range will be 1.495 to 1.795GHz.

The ratio of reference frequency to synthesised frequency of the SP5060 is 256, giving a reference requirement to be produced by the NJ8820 of 5.83984375 to 7.01171875MHz. Similarly, if the step size at the mixer is set at 10MHz the reference step becomes 19.53125kHz.

Although these numbers are beginning to look somewhat formidable, the NJ8820 is capable of producing the required output if a 6.25MHz reference crystal is used with the reference counter programmed to divide by 160, or 320 including the fixed divide by 2. Frequency adjustment to anywhere in the required range can now be obtained by setting the ratio of the N counter in the NJ8820 as follows:

$$\text{Step size of NJ8820} = \frac{\text{crystal reference frequency}}{160 \times 2}$$

$$= \frac{6.25\text{MHz}}{320}$$

$$= 19.53125\text{kHz}$$

Programming input for reference counter

$$= \text{binary } 160$$

$$= 00010100000$$

To tune a minimum frequency of 5.83984375MHz (for a mixer LO input of 2.99GHz) requires input to the NJ8820 N counter of:

$$\frac{5.83984375\text{MHz}}{19.53125\text{kHz}} = 299$$

$$= 0100101011$$

NOTE: Using this scheme the ratio at the NJ8820 N counter is equal to the local oscillator mixer input frequency in GHz x 100. For example, if the LO input to the mixer is required to be 3.15GHz the ratio will be 315 or binary 0100111011.

The flexible programming ability of the NJ8820 will allow a receiver using this system to be controlled using either a microprocessor or a multi-position switch in conjunction with a PROM as shown in the NJ8820 data sheet.

SP5051 2GHz SYNTHESISER
SP5052 2.3GHz SYNTHESISER

Block conversion receivers generally produce a first IF ranging from 950MHz to 1450MHz in the case of the US C-band services, and from 950MHz to 1750MHz for the proposed DBS services. Using a high side local oscillator necessary to obtain the required tuning range, and with a European standard 480MHz 2nd IF the required frequency range will be 1430MHz to 2230MHz obtainable by raising the SP5051/SP5052 reference frequency to about 4.36MHz. Although calculating a suitable reference frequency to just cover the maximum requirement will give the smallest step size and therefore greatest resolution if fine tuning for AFC is used, the step size for any data bit does not coincide with the 19.18MHz standard DBS channel spacing, possibly increasing the complexity of the control software. A better solution might be to increase the reference frequency to 4.795MHz giving a rather curious minimum step size of 0.14984375MHz but producing a 19.18MHz step for the 2^7 data bit.

For a C-band system, a suitable reference frequency might be 5MHz giving a 20MHz step for the 2^7 data bit with a minimum step size of 0.15625MHz and a theoretical maximum synthesised frequency of 2.5598GHz, well above that required for a 612MHz IF.

REMOTE PROGRAMMING OF SP5000 SERIES SYNTHESISERS

Although remote programming of SP5000 series synthesisers appears complex at first sight, with a requirement for Chip Enable and Data Clock signals as well as the frequency data, the task can be greatly simplified using the circuit shown in Fig.6.

Obviously it is most convenient to have only a single downlead between the head end and indoor units of a satellite receiver, and therefore the system shown in Fig.6 sends data along the downlead at a relatively low frequency (125kHz) which can be easily filtered from the IF signal. The data is sent as a burst of 125kHz, representing a '1', and a logic '0' by the absence of signal. The duration of each logic bit is 64 cycles of 125kHz equivalent to a time period of 0.512ms (see Fig.7).

Data Clock and Chip Enable inputs are generated locally from the data input to avoid having to encode these on the overworked downlead, the process being initiated by the leading edge of the first data bit which must always be logic 1. Since the first data bit is used only by the band select or control outputs, this causes no frequency setting limitation and the second bit is still available for use as a polarisation setting control.

Circuit Description (Fig.6)

The 567 phase locked loop tone decoder chip is set to detect the bursts of 125kHz, producing a low output at pin 8 when the input is present. Loop and output filter components are selected to give fast response consistent with reasonable noise performance. As the first bit in the data stream must always be a logic '1', the negative-going edge at pin 8 produced at the beginning of bit 1 is used to trigger the R-S flip-flop formed by two CMOS NAND gates thus initiating the decoding process. Pin 8 also provides the data input to the SP5000 series device whilst the R-S flip-flop provides Chip Enable.

Once the R-S flip-flop is triggered, the output of the 567 oscillator, at or very close to 125kHz (depending on the presence or lack of 125kHz at the input), drives the 4040 counter. After 32 cycles of the 125kHz input data stream the Q6 output on pin 2 goes high providing a data clock signal to the synthesiser in the centre of the 64 cycle data period. Data clock pulses will continue from pin 2 until all 16 data bits are clocked, when the Q10 output on pin 14 goes high resetting the R-S flip-flop and terminating the chip enable signal. The R-S flip-flop also resets the 4040 leaving the system to be retriggered by the next data stream.

A suitably encoded data stream can be generated under program control from a microprocessor or perhaps more easily by gating under program control the divided output from the microprocessor oscillator (often 4MHz, which, when divided by 32 gives 125kHz).

A low pass filter such as that shown in Fig.6 should be inserted between the downlead and data generating logic to prevent harmonics from the logic section interfering with the picture when fine tuning is used. The same filter will also prevent loading of the IF output by the logic.

MICROPROCESSOR CONTROL

Although as shown above there are various down conversion systems applicable to satellite reception, all have a requirement for some form of control system. A microprocessor used in this control function usually gives greatest flexibility allowing decoding of remote control and local keyboard inputs, generation of input data for synthesisers, channel display and a program memory feature using a single component.

Full and comprehensive details of such a system using the SP5000 synthesiser range are given in the publication P.S.2011 'Single Chip Frequency Synthesis'.

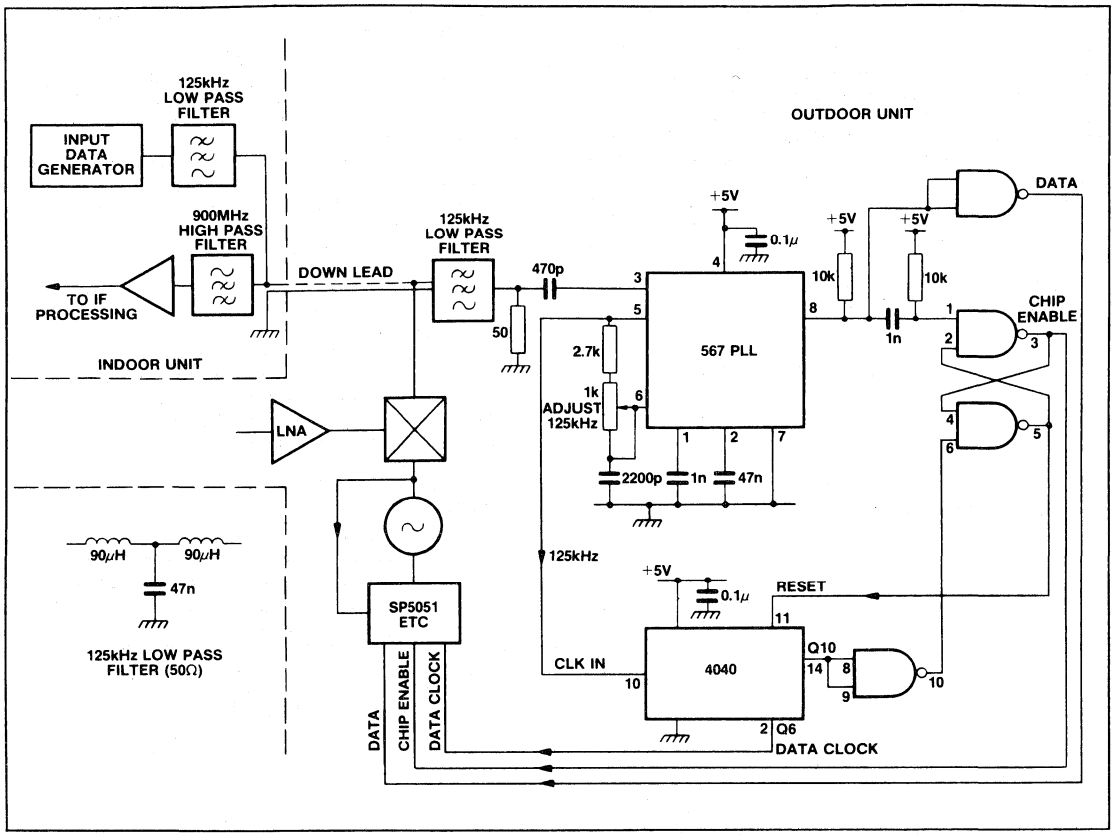


Fig.6 Remote data receiver circuit diagram

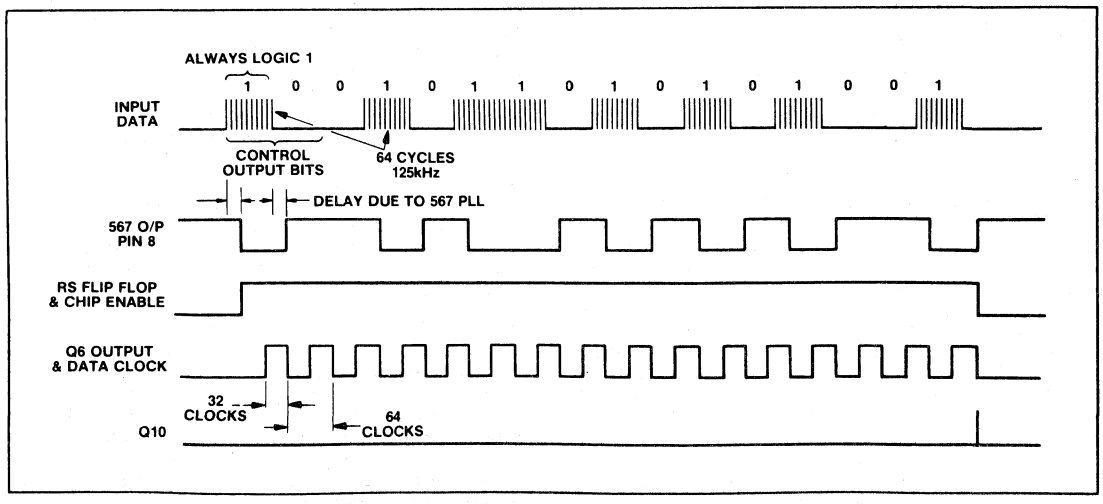


Fig.7 Remote data receiver waveforms

A Low Cost 1.5 to 2.2GHz Voltage Controlled Oscillator

The introduction of the Plessey Semiconductors range of 2GHz synthesisers and prescalers for low cost applications such as consumer satellite TV reception has created a requirement for an economic VCO design covering a frequency range from around 1.5GHz to 2.2GHz. Although suitable hybrid oscillator designs are available from various manufacturers, these generally carry a price tag at least an order of magnitude higher than that of the synthesiser thus making their use in consumer equipment hopelessly uneconomic.

The design shown in Fig.8 has been developed using low cost components which should be easily available, the varicap diodes being normal UHF TV tuning types and the transistor a standard catalog item.

A major problem when operating at these frequencies is that the series inductance of most capacitors becomes very significant compared with that required in the resonator circuit and also prevents good decoupling. These problems are overcome when designing fixed frequency oscillators by replacing the normal resonant circuits and decoupling capacitors with open or short circuited resonant transmission lines, but a design requiring wide frequency variation must use more conventional techniques.

The transistor is biased to about 15mA using a 22kΩ resistor from collector to base. Any problems with decoupling at the emitter are avoided by connecting the emitter direct to ground. Stabilisation of the bias point relies on the 330Ω collector load resistor providing a degree of feedback. A small inductor in series with the collector load resistor reduces any loading and improves the effectiveness of the +12V supply decoupling. A series tuned circuit consisting of a small inductor and two varicap diodes is connected between collector and base with a 390pF capacitor providing DC isolation of the varicap diodes from the collector voltage. To avoid the introduction of any additional series inductance, the varicap diodes are connected direct to the transistor base without a coupling capacitor. The oscillator frequency is varied by adjusting the varicap bias voltage from 0 to 30V via a 47kΩ isolating resistor. Output amplitude from the basic oscillator is much higher than the input requirements of the synthesiser or prescaler and therefore about 10dB of attenuation is provided by a resistive attenuator.

As might be expected with an oscillator operating at this frequency, layout is fairly critical and the layout shown in Fig.9 should be followed accurately or extensive trials made before any variations are attempted. The prototype oscillators were made on standard 1/16 inch fibreglass board, but it was found impossible to mount the frequency determining components on the board without greatly affecting the frequency range available; these components are therefore mounted off board, relying on short lead lengths to provide sufficient rigidity.

OSCILLATOR SPECIFICATION

Operating voltage : +9V to +14V
Frequency range : 1.5GHz to 2.2GHz
Varicap voltage range : 0V to +30V
Output level : (with 10dB attenuator) -10dBm (70mV)

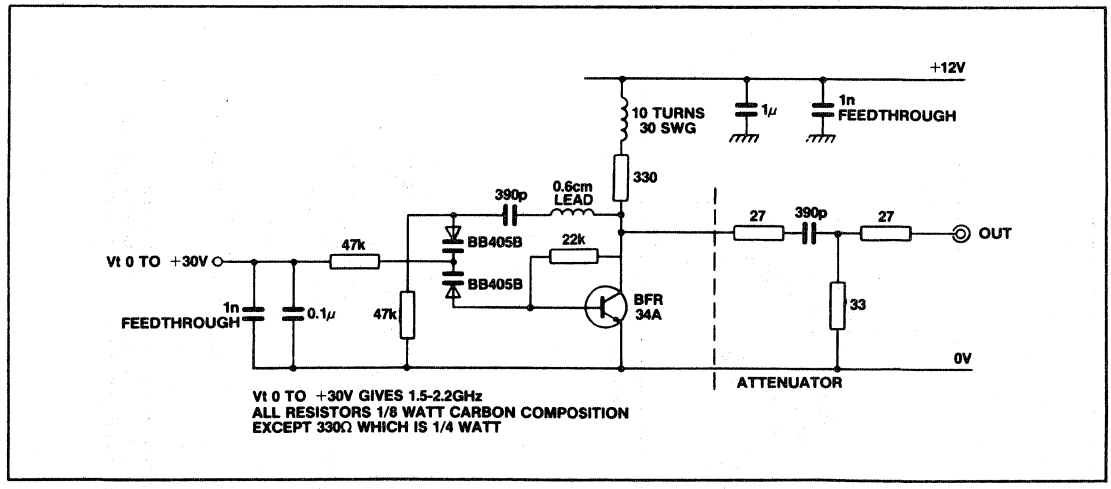
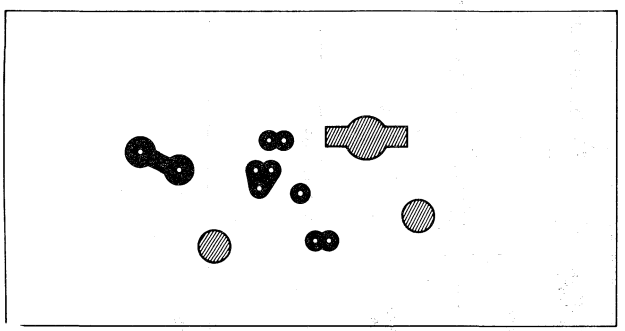
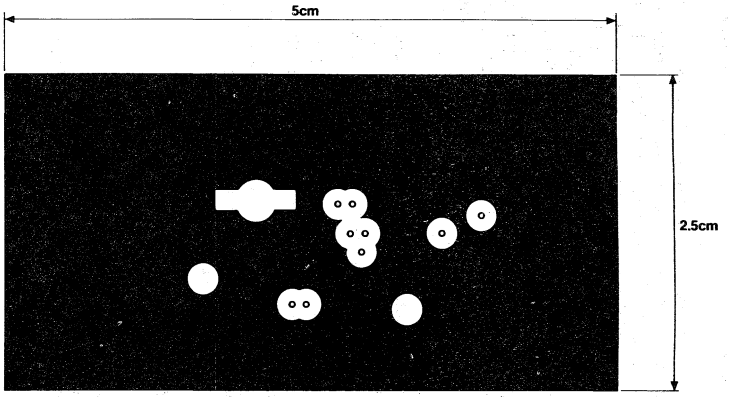


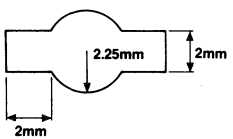
Fig.8 2GHz VCO circut diagram



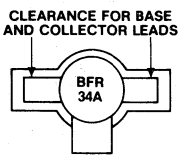
Track side



Ground plane

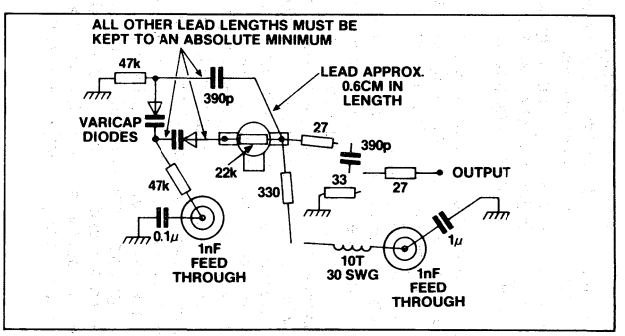


CUT-OUT



EMITTER
LEAD SOLDERED TO GROUND LANE

Transistor mounting details. In order to reduce the transistor lead lengths to a minimum, a hole is cut into the board as shown and the transistor mounted flush on the component side of the board.



Component overlay

Fig.9 Oscillator printed board layout

FM Demodulator Applications

SL1451 THRESHOLD EXTENDED DEMODULATOR

The SL1451 is a Phase locked loop FM demodulator for use at intermediate frequencies in the 400-700MHz range. The chip contains all the necessary building blocks to form a complete demodulator as shown in the simplified block diagram Fig.10.

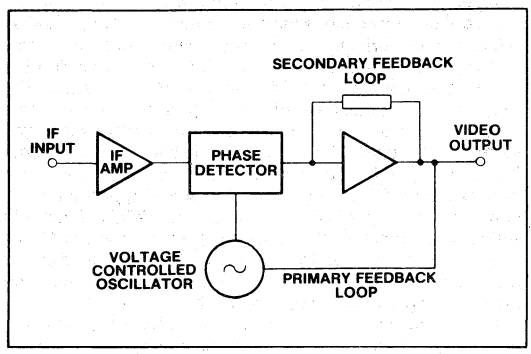


Fig.10 Block diagram of PLL

A 'basic' circuit configuration suitable for demodulating a 612MHz, 13.5MHz peak to peak signal is shown in Fig.11, whilst the circuits in Figs.12-15 are variations tailored to give improved performance under various conditions. These circuit variations will be discussed later.

The on-chip oscillator consists of a single transistor with emitter, base and collector connections bonded out to pins 3, 4 and 5 (see Fig.12). The collector, pin 5, is internally decoupled to ground, preventing the use of oscillator configurations requiring a signal output from the collector. Bias for the transistor is provided by internal resistors.

Using the Clapp variant of the well known Colpitts oscillator, the physical size of inductor required to achieve the operating frequency is increased to acceptable proportions by reducing the effective inductance using a series capacitor, in this case the varicap diode D1. The inductor can take the form of a straight 25mm length of 22 SWG wire separated by about 3mm from the ground plane or 2 turns 22 SWG approximately 4mm in diameter. Tuning to the precise centre frequency is accomplished by bending the straight inductor closer or further from the ground plane or by opening or closing the turns of the coil. In either case, correct tuning is established when the voltage at the video output pin 14 is at 4.5V DC (centre of linear video amplifier range and therefore centre of lock range). Alternatively the 3.9pF capacitor C5 can be replaced by a trimmer to adjust centre frequency.

The oscillator output from the emitter, at an optimum level (-10dBm) for threshold performance, is coupled by C8 to one input of the differential phase detector, the other being decoupled to ground by C10.

Differential outputs from the phase detector are internally connected to the video amplifier, which in turn drives the varicap diode D1 via the RF-blocking filter L1, maintaining phase lock with the RF input signal on pin 11. With the component values shown, the oscillator frequency gradient is approximately 14MHz/Volt giving a 1V video output from a 13.5MHz peak to peak deviation input signal.

The input amplifier is of differential design and is internally connected to the phase detector, this signal input being coupled to pin 11 via C11. A capacitor C6, decouples the other input to ground.

Although the input amplifier is of variable gain, programmable by varying the voltage on pin 10, most applications of the device give best threshold performance when the gain is at maximum. This is ensured by connecting the resistor R6 from pin 10 to VCC.

An AGC detector circuit connected to the RF amplifier output, provides an output at pin 9 which may be used to control the gain of preceding receiver amplifier circuits. The input amplifier has a signal handling range at pin 11 between -25dBm and 0dBm.

All capacitors associated with the oscillator and RF portions of the circuit should be suitable for use at high frequencies. Ceramic chip types are recommended.

Capacitors C1 and C2 connected between the differential inputs and outputs of the video amplifier determine the loop filter response and in Fig.11 are optimised for the DBS standard 13.5MHz peak to peak deviation at a centre frequency of 612MHz.

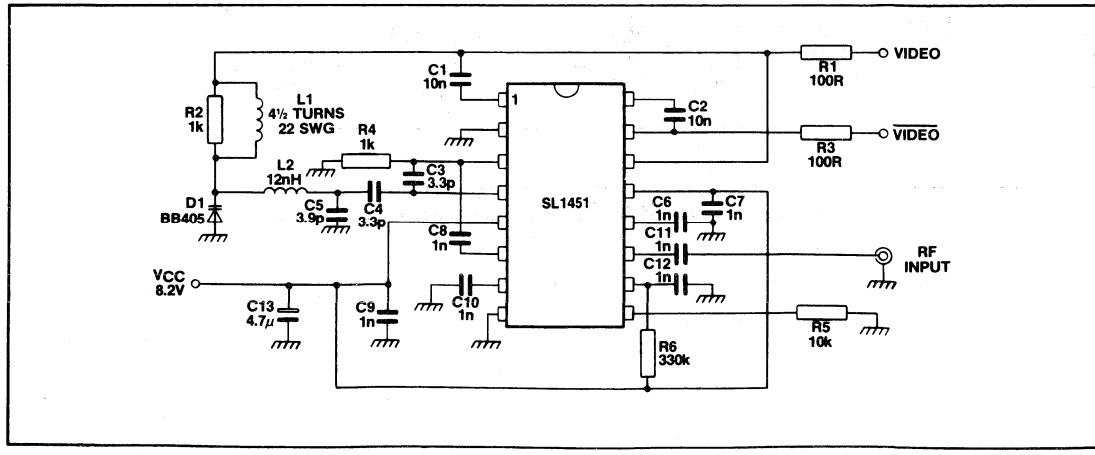


Fig.11 612MHz demodulator 13.5MHz peak to peak deviation

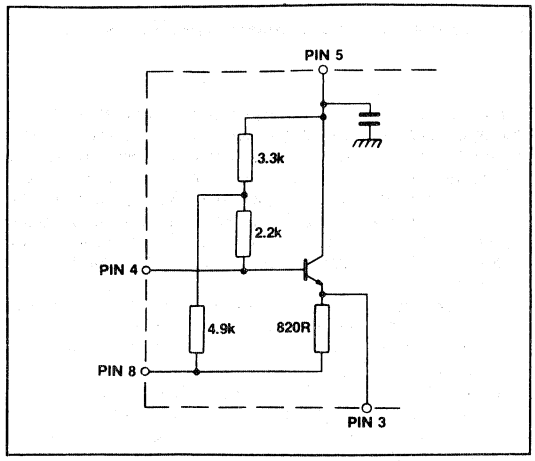


Fig.12 On-chip oscillator circuit

The circuit in Fig.11 has a measured threshold of 8dB and an 18MHz video bandwidth.

Although the circuit shown in Fig.11 gives optimum threshold performance for signals with peak to peak deviations up to about 15MHz, for wider deviation signals the loop filter components must be changed to prevent picture tearing on fast black to white transitions. The loop filter changes have a slight detrimental effect on the obtainable threshold.

For slightly wider deviation signals from about 15 to 20MHz peak to peak it is only necessary to reduce the feedback capacitors C1 and C2 from 10nF to 330pF giving a noise threshold of 8.5dB.

Signals with deviations greater than 20MHz can be accommodated by changing the video amplifier to a single sided configuration by decoupling one input and output (pins 15 and 16) as shown in Fig.13. A 330pF loop filter capacitor is connected between the active input and output pins. This circuit also exhibits an 8.5dB noise threshold.

When the signal to noise ratio at the input of the demodulator approaches the noise threshold point, sparklies (noise spikes), primarily occur in the saturated colour areas of the video. This effect can be reduced by increasing the open loop gain of the PLL at the chroma subcarrier frequency. A parallel tuned circuit (tuned to the chroma frequency) incorporated in the secondary feedback loop will increase the gain of the video amplifier at the chroma frequency and hence increase the open loop gain. For example, for a PAL system (f = 4.433MHz) a parallel tuned circuit comprising a 270pF capacitor and 4.77μH inductor in series with the standard feedback component in Fig.13 will improve the chorma performance. The Q of this tuned circuit must be greater than 10. A complete circuit diagram incorporating this modification is shown in Fig.14.

All the circuits shown so far have a 612MHz oscillator, but when required, it is relatively easy to modify the design for use at other frequencies. Fig.15 shows a design for 480MHz signals of 26MHz peak to peak deviation.

Due to the high operating frequency of the SL1451, particularly the oscillator and input amplifier circuits, care is needed in layout and component selection. A board layout for the circuit configuration with chroma trap (Fig.14) is shown in Fig.16.

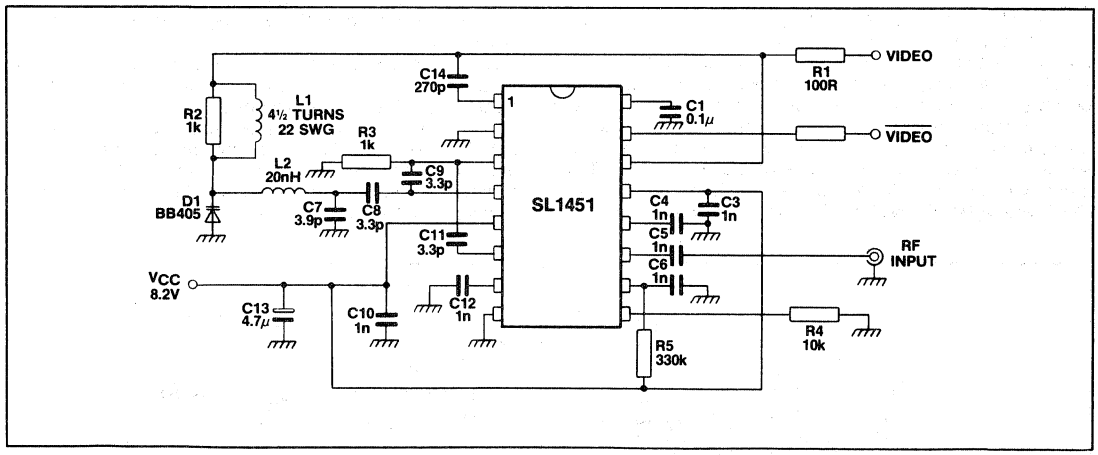


Fig.13 612MHz demodulator for up to 28MHz peak to peak deviation

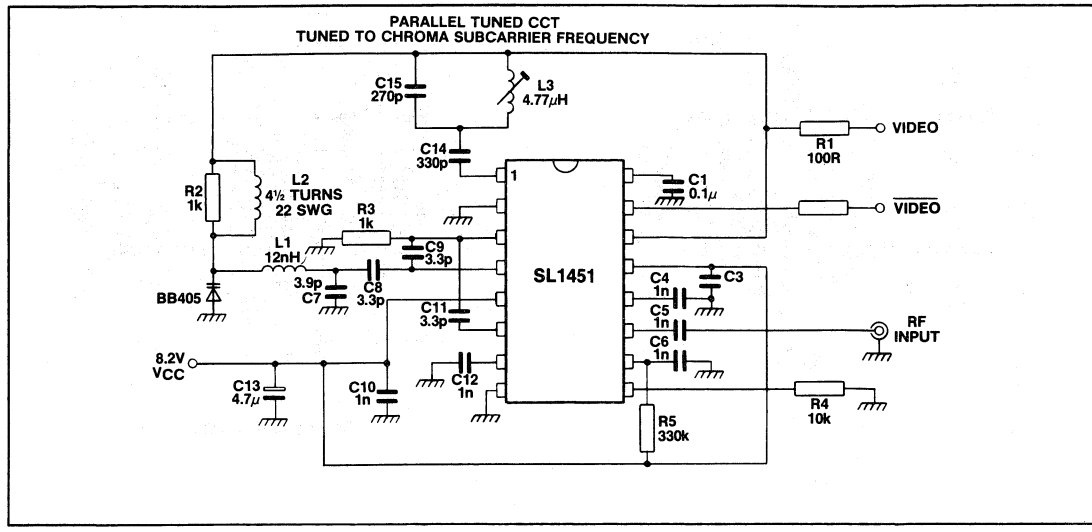


Fig.14 612MHz demodulator for up to 28MHz peak to peak deviation with improved chroma response (recommended PC board layout is given in Fig.16)

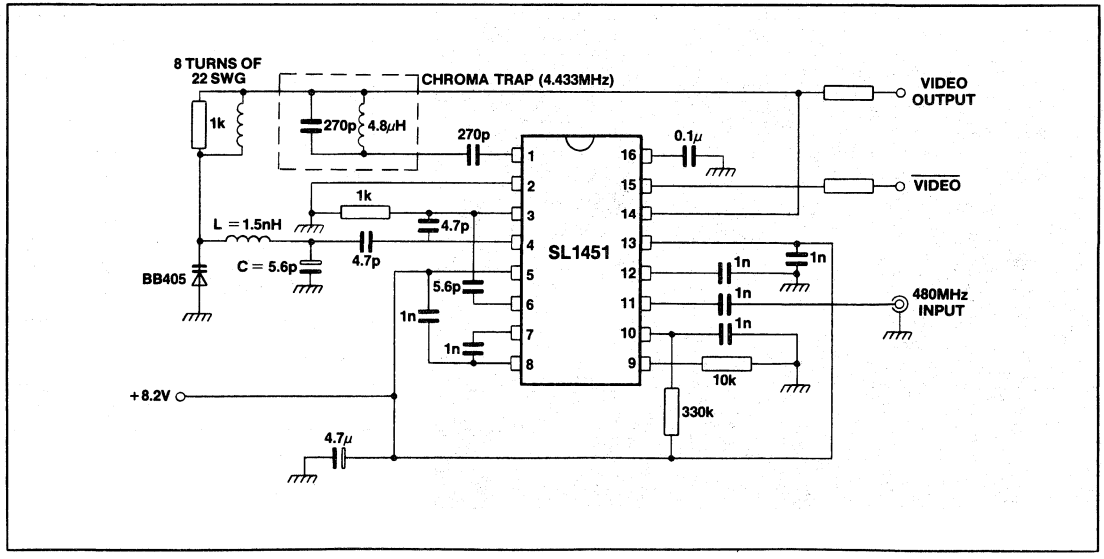
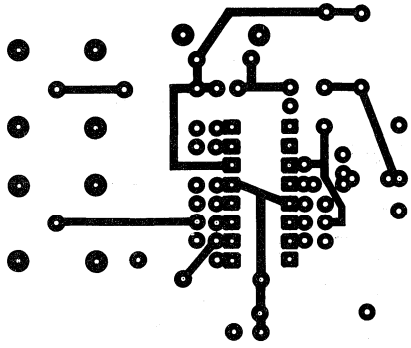
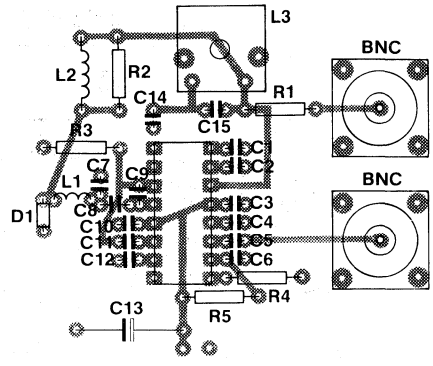


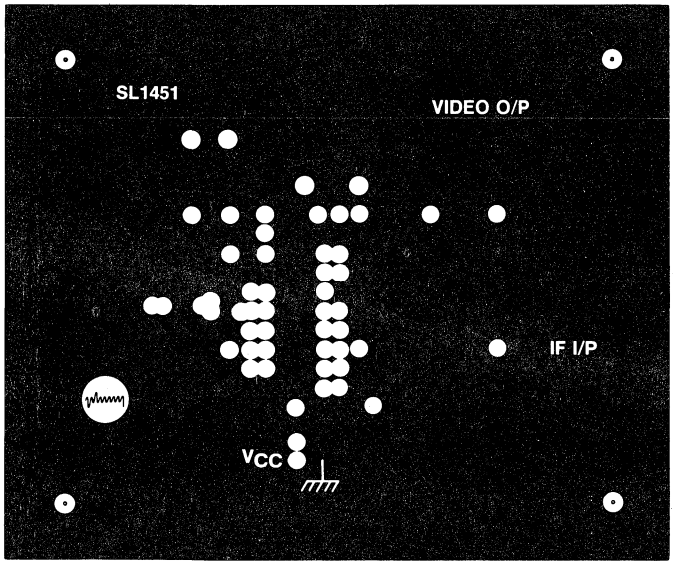
Fig.15 480MHz demodulator for up to 26MHz peak to peak deviation



Track side



Component overlay



Ground plane

COMPONENTS			
R1	100Ω	C1	0.1μF
R2	1k	C2	0.1μF
R3	1k	C3	1n
R4	10k	C4	1n
R5	330k	C5	1n
		C6	1n
L1	12nH	C7	3.9p
L2	4½ TURNS 22 SWG	C8	3.3p
L3	4.6μH TUNABLE	C9	3.3p
	TO CHROMA	C10	1n
	FREQUENCY	C11	3.3p
		C12	1n
D1	BB405	C13	4.7μ
		C14	330p
		C15	270p

Fig.16 SL1451 612MHz FM demodulator demonstration board with chroma trap (circuit shown in Fig.14)

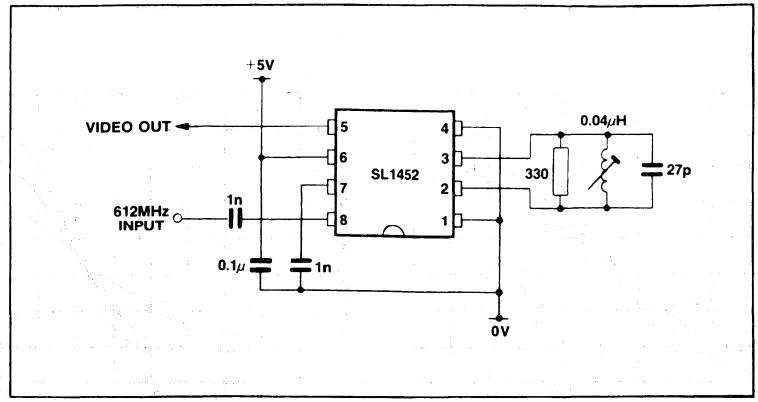


Fig.17 Typical application of SL1452

SL1452 QUADRATURE DEMODULATOR

The SL1452 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.17, but as with most integrated circuits, particularly those working at high frequencies some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies: multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency, which is a quarter of the input frequency on pin 8 due to the two internal divide by 2 circuits (see Fig.2 on data sheet).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{(LC)}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restrict the video output available. In general for operation in the 400 to 600MHz range, an inductance value between 40 and 60nH is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.18.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800 resistor between pins 2 and 3 must be allowed for when calculating R.

Example

Design a quadrature circuit to demodulate a carrier on pin 8 with centre frequency 480MHz and video bandwidth of 10MHz.

For L = 40nH and f_{quad} = 120MHz,
C = 43.98pF (nearest preferred value 47pF)
From Table 1, Q required is approximately 6
therefore total R required is:

$$R = Q2\pi fL$$

$$= 6 \times 2 \times \pi \times \frac{480}{4} \times 10^6 \times 0.04 \times 10^{-6}$$

$$= 181 \text{ ohms}$$

allowing for the internal 800 ohm resistance between pins 2 and 3 (see Fig.3 of data sheet), the external resistance required is 234 ohms. Choose 270 ohms.

It should be remembered that the internal 800 ohm resistance is subject to production tolerances and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270 ohms obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	BANDWIDTH
10	7.5MHz
6	14MHz
4	23MHz

Table 1

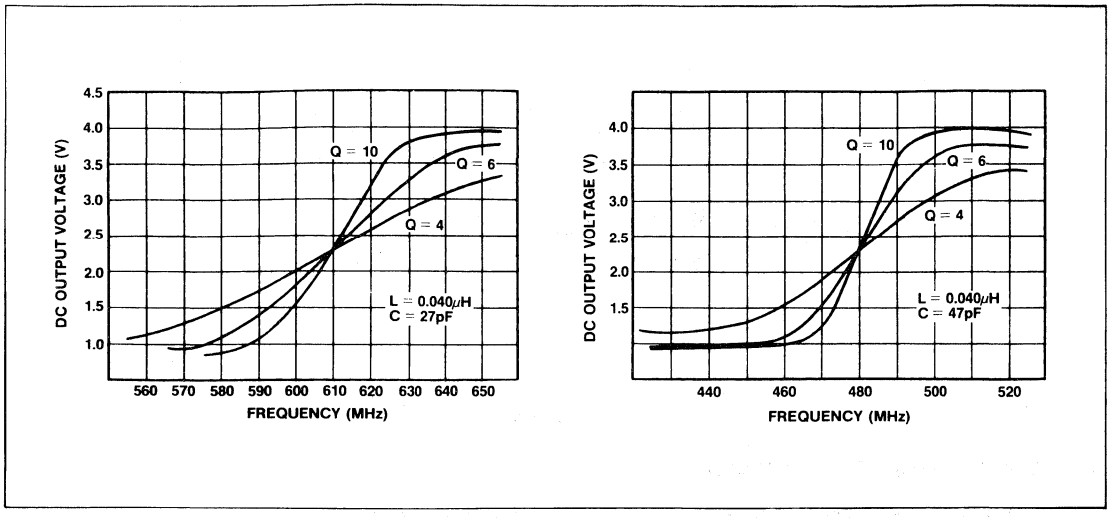


Fig.18 Output voltage versus input frequency

SL1455 EXTENDED THRESHOLD DEMODULATOR

The SL1455 is a wideband FM detector designed for Satellite TV applications. Fig.1a shows a typical application circuit for demodulating 612MHz and 480MHz wideband FM signals. The device is similar in principle to the SL1452 demodulator, but with the first divide by two stage replaced by an injection locked oscillator running at half the input frequency. Replacing the first divider in this way has the advantage that the noise threshold point can be extended by up to 3dB compared with a conventional quadrature detector such as the SL1452.

The span of input frequencies over which the oscillator will lock is referred to as the 'lock range'. The lock range of the oscillator is symmetrical about the centre frequency of the FM signal and can be altered by adjusting the input level to the device. Fig.20 shows how the lock range increases with input level.

An additional advantage of this device is the ability to program the degree of extension available by controlling the input level to the circuit.

Threshold extension is achieved by reducing the lock range of the oscillator so that it is just capable of locking onto the input FM signal (usually the peak to peak deviation +10MHz). The effect of reducing the lock range on noise threshold of a 612MHz demodulator is shown in Fig.21. The only detrimental effect of reducing the lock range is that it reduces the video bandwidth, see Fig.22.

The application circuits consists of 2 main sections, the tuned circuit for the oscillator and the quadrature network. The oscillator tuned circuit is designed to resonate at half the FM signal centre frequency with the internal device capacitance of 11pF between pins 3 and 4. The simplest solution is an inductor across pins 3 and 4. The value of this inductor can be calculated from:

$$L = \frac{1}{C_{INT}(2\pi f)^2} \quad C_{INT} = 11pF$$

However, this will produce a very small value of L for high frequency oscillators. A larger value of inductor can be used in series with a capacitor which effectively reduces inductance. The value of this capacitor can be calculated from:

$$C = \frac{1}{(Lp - L)(2\pi f)^2}$$

Lp = inductance used
L = inductance needed for resonance

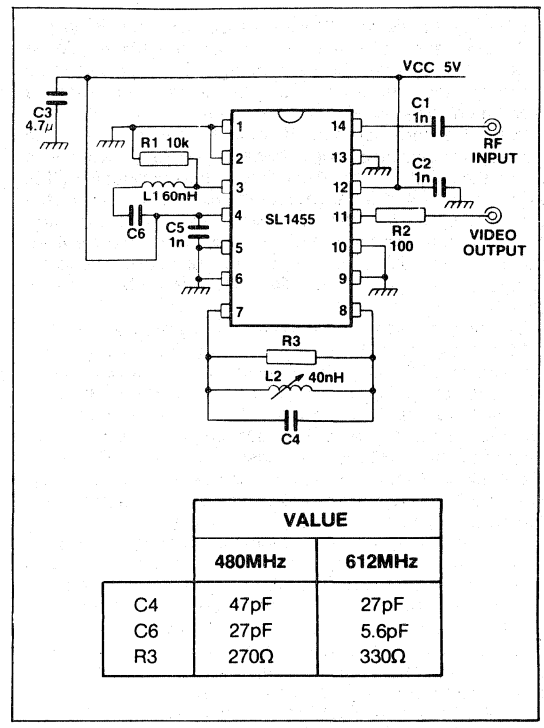
Lp must not be too much larger than L otherwise impractical values for C will be obtained.

Example

For a 612MHz FM demodulator a 306MHz oscillator is to be designed.

L = 24nH for resonance with the internal 11pF.

This is a rather small and non-standard value of inductor, so a more readily available value 60nH is chosen. To convert this to an effective inductance of 24nH, 7.6pF would theoretically be added in series but as practical track layout has some finite inductance (about 10nH in the layout shown in Fig.24) a revised capacitance of 5.6pF is more accurate.



	VALUE	
	480MHz	612MHz
C4	47pF	27pF
C6	27pF	5.6pF
R3	270Ω	330Ω

Fig.19 Typical application 480 and 612MHz threshold extended demodulator

One of the components in the tuned circuit should be made variable to fine tune the oscillator to half the FM signal centre frequency. The centre frequency needs to be relatively accurate for optimum threshold performance.

Calculations to determine the values of quadrature components between pins 7 and 8 are exactly as for the SL1452 (p.15), as are those given in the example for the damping resistor between pins 7 and 8 (pins 2 and 3 on the SL1452).

The Q factor determines the video output level and bandwidth (although with Q factors of below 10 the video bandwidth is defined by the lock range of the oscillator).

Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.23.

Practical System Design

When designing the PCB for the SL1455 good RF layout techniques should be applied. All track lengths should be kept to a minimum and decoupling capacitors placed as close to the device as possible. A ground plane is recommended - see Fig.24 for an example of layout.

With this form of demodulator a further increase in threshold extension can be achieved by designing a circuit in which the injection-locked oscillator tracks the incoming FM signal. To do this a varactor diode is incorporated in the oscillator circuit to produce a voltage controlled oscillator. This VCO can then be controlled by feedback from the video output. The amplitude of the video feedback to the oscillator is calculated so that the oscillator tracks the FM input very closely.

The only problem encountered when designing a system with video feedback is compensating for a 40ns delay introduced by the SL1455 between the FM input signal and the video output. This delay is insignificant for low frequency feedback to the tracking oscillator, but does effect the chroma feedback. For a PAL system (chroma subcarrier frequency = 4.433MHz) a phase advance of 63° in the feedback network is necessary to compensate for this delay. For an NTSC system a phase advance of 50° is necessary (chroma subcarrier frequency = 3.58MHz).

Most satellite broadcasts employ pre-emphasised signals in which the chroma and high frequency information has a much larger peak-to-peak deviation than the low frequency information. The feedback network needed to feed back the full demodulated video with the correct phase and amplitude would be very complex. But as a large portion of the signal is chroma subcarrier, using simple chroma feedback the overall noise threshold can be improved.

Fig.25 shows a 612MHz demodulator with chroma feedback for a PAL signal. The feedback network consists of an amplifier with phase correction components (C7, R4, R5, C9, R10). The voltage to frequency gain of the VCO is 5MHz per volt. As the oscillator locks to half the input frequency it will effectively track the input frequency at 10MHz per volt. The quadrature components are set to give a 1V peak-to-peak output for an input signal with a 20MHz peak-to-peak deviation. For the oscillator to track the chroma correctly a voltage gain of 2 is required in the feedback network.

The centre frequency of the oscillator is governed by the supply voltage and the variable 60nH inductor.

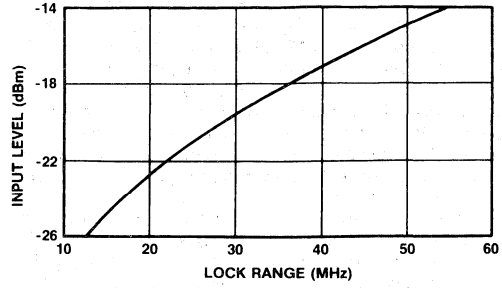


Fig.20 Lock range versus input level

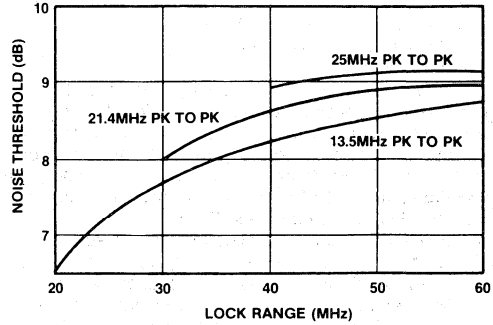


Fig.21 Lock range versus threshold

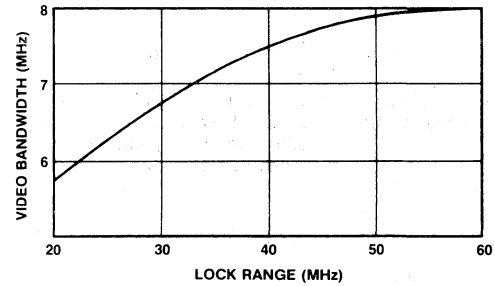


Fig.22 Lock range versus bandwidth

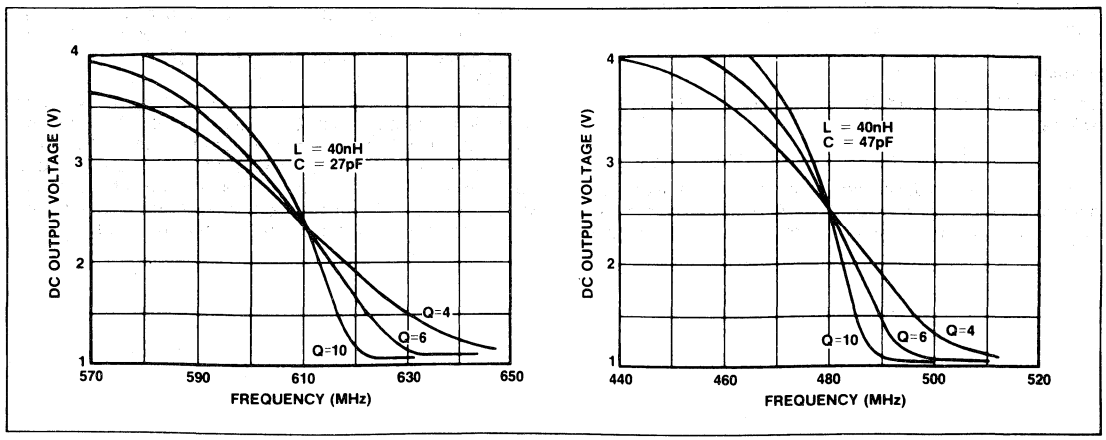
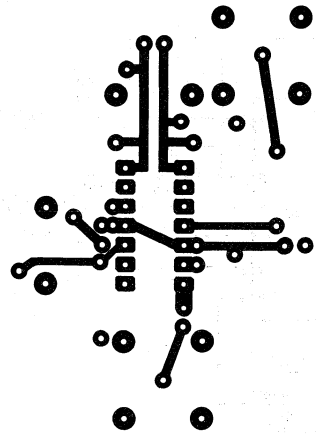
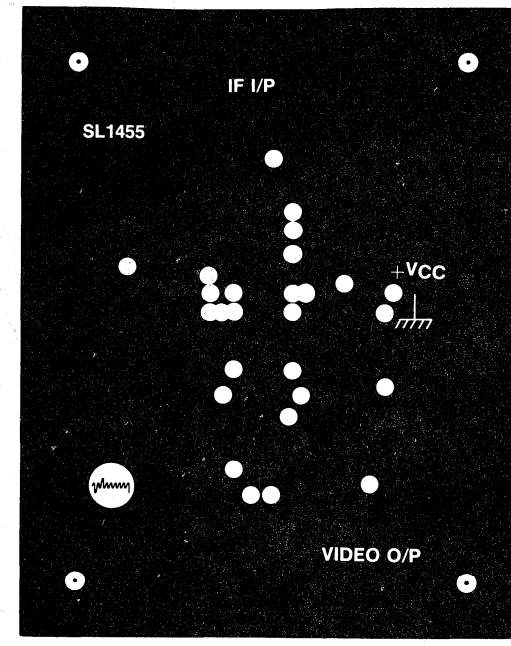


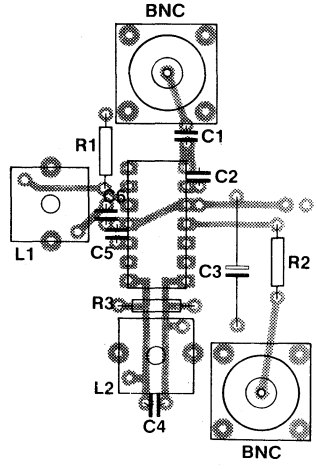
Fig.23 SL1455 output voltage versus input frequency for large lock range



Track side



Ground plane



Component overlay

COMPONENTS			
R1	10k	C1	1n
R2	100Ω	C2	1n
R3	330Ω	C3	4.7μ
		C4	27p
		C5	1n
		C6	5.6p
L1	60nH TOKO COIL		
L2	40nH TOKO COIL		
	+2 BNC SOCKETS		

Fig.24 Recommended board layout for 612MHz SL1455 FM demodulator circuit of Fig.19

This circuit improved the chroma noise threshold response without deteriorating the black and white noise threshold. Components for an NTSC version are C7 = 390pF, all others are the same as with the above PAL version.

To check that the feedback loop has a gain of just less than 1 (for stability) and that the phase compensation network is correct, the loop can be opened at point A and a signal (chroma frequency) injected from a signal generator to the VCO (via C11) and the output of the emitter follower (B) monitored. L3 should be adjusted for maximum output and the overall gain may be altered by varing R8. If the phase is incorrect, C9 and C7 should be checked. These measurements should be done whilst no signal is applied to the input of the device.

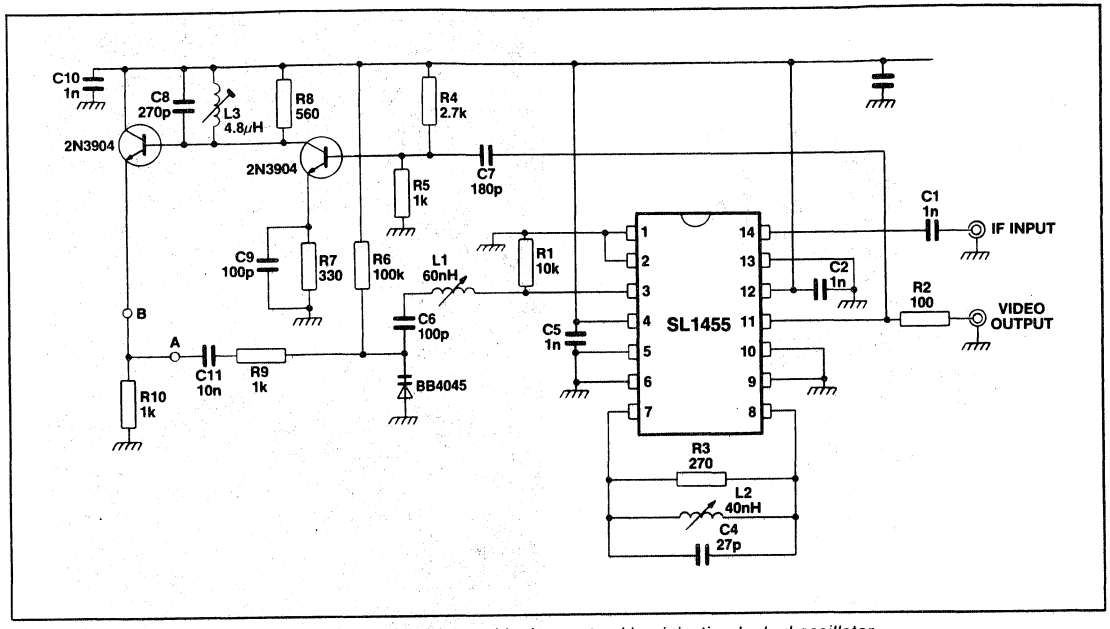


Fig.25 612MHz demodulator with chroma tracking injection locked oscillator

SL1454 LOW FREQUENCY QUADRATURE DEMODULATOR

The SL1454 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.26, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be attained by the simple precaution of keeping all components close to the SL1454, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies. A fairly stable component should be selected for the quadrature coil tuning capacitor to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum, but the input coupling and decoupling values can be smaller, about 1nF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if optimum performance is to be obtained.

Choose suitable values for L and C to resonate at the intermediate frequency you are applying to the device using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation S curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive lead to the demodulator and thereby restrict the video output available.

Once suitable values for L and C have been determined, the working Q for the quadrature circuit should be set, the Q value determing the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 2 and the graphs in Fig.27.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistor between pins 2 and 3 must be taken into account when calculating R.

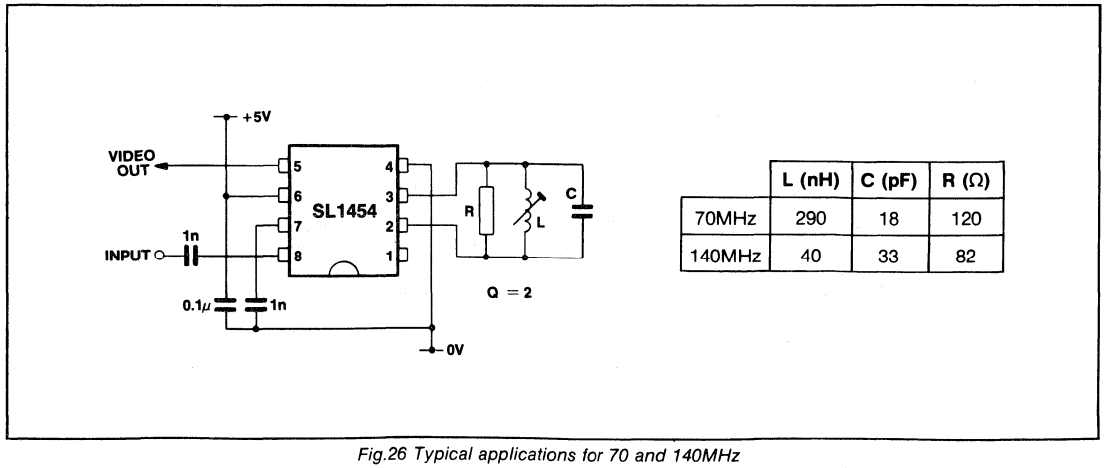
As can be seen from the graphs in Fig.27, for the demodulator to demodulate a 20MHz peak-to-peak deviation signal with optimum linearity a very low Q value needs to be chosen (<2). But this has the disadvantage of producing a demodulator with a very low peak-to-peak video output level.

One way of increasing the linear region of the S curve without reducing the video output level is to incorporate a dual tuned circuit to the normal quadrature tuned circuit.

Fig.28 shows an example of this form of dual tuned circuit, both sections have the same Q factor and the coupling capacitors are chosen to give the best linearity (linear phase response). Fig.27(b) shows the advantages of the dual tuned circuit. The effect of varying the Q factor of the dual tuned circuit on bandwidth is also described by Table 2.

Q	BANDWIDTH
6	10MHz
4	11MHz
2	12MHz

Table 2



	L (nH)	C (pF)	R (Ω)
70MHz	290	18	120
140MHz	40	33	82

Fig.26 Typical applications for 70 and 140MHz

Example

Design a quadrature circuit to demodulate a 140MHz carrier with 21.4MHz peak-to-peak deviation, modulated with a 25Hz triangular dispersion waveform of 2MHz peak-to-peak deviation. The video bandwidth required is 9MHz.

Choose L = 0.04μH
then C = 32.309pF (nearest preferred value = 33pF)

The next value to choose is the Q factor. As dispersion is employed linearity over the full 21.4MHz range needs to be optimised. The graphs in Fig.28 show that either a single tuned circuit with a Q of 2, or a dual tuned circuit with a Q of 3 is adequate. The dual tuned circuit has the advantage that the peak-to-peak video output is larger than that of the single tuned circuit, but extra components are required. Both circuits have a larger video bandwidth than the required 9MHz. The value of the damping resistor for the required Q is calculated as below:

For Q = 2

Total R = $Q2\pi fL$

$= 2 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$

$= 70.37\Omega$

Allowing for the internal 800Ω resistor the external resistance should be 77.1Ω, choose 82Ω.

For Q = 3

Total R = $Q2\pi fL$

$= 3 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$

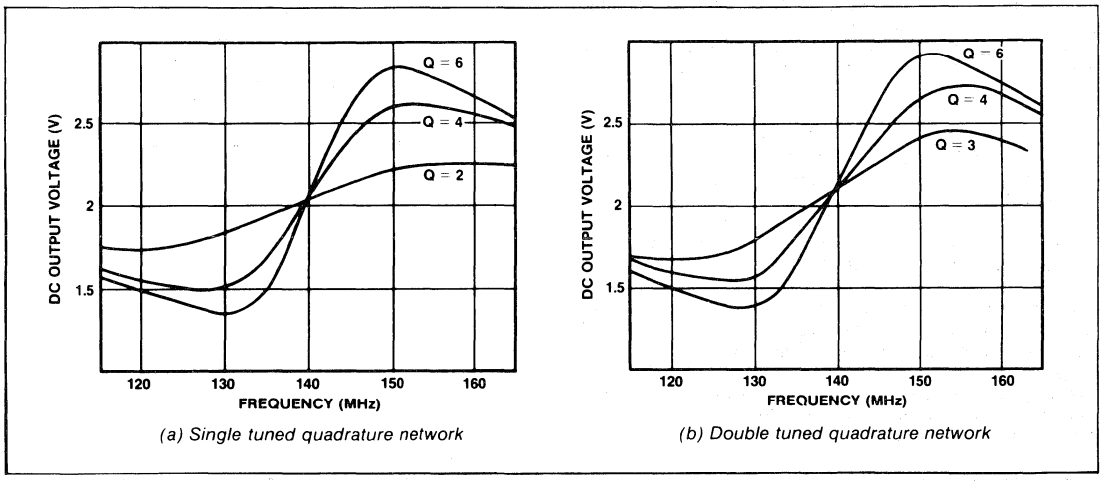
$= 105.56\Omega$

Allowing for the internal 800Ω resistor the external resistance should be 121.5Ω, choose 120Ω.

When using a dual tuned circuit the value of coupling capacitor is dependent on the Q factor. Table 3 gives a guide to the values need for best linearity.

Q	COUPLING CAPACITOR
6	3.9p
4	5.6p
3	10p

Table 3



(a) Single tuned quadrature network

(b) Double tuned quadrature network

Fig.27 Output voltage versus frequency

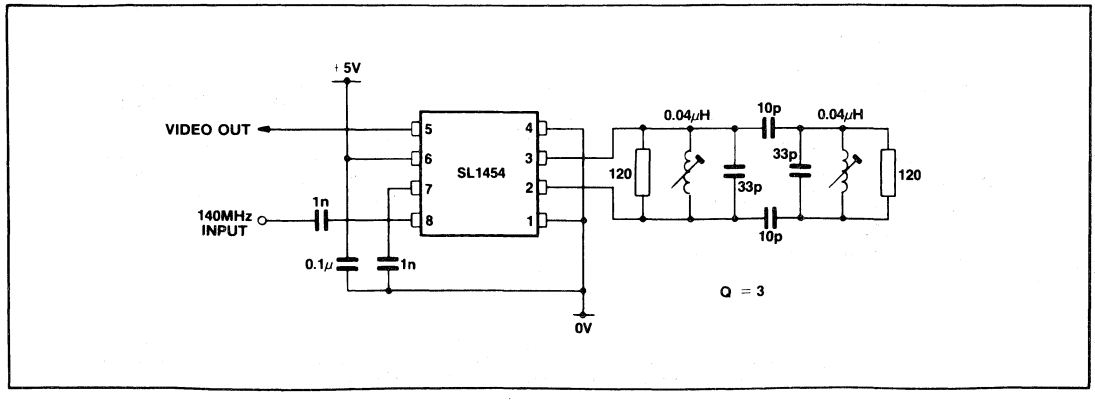


Fig.28 Example of a double tuned quadrature circuit

Designing with the SL1451 Phase Locked Loop

The SL1451 is a phase locked loop circuit originally designed as a demodulator for satellite TV signals. As a consequence of the trend towards high frequency IF design in satellite receivers, the SL1451 has been designed to operate at frequencies up to 612MHz, but despite this very high maximum operating frequency and specific design objective, the SL1451 is still useful as a general purpose phase locked loop in many other applications.

In order to demonstrate the versatility of the part, a design for an FM demodulator for broadcast radio was tested. The circuit diagram of the demodulator is shown in Fig.1 and a block diagram of the PLL system is shown in Fig.2. When designing for uses other than satellite TV demodulation, two main circuit areas require design changes, these are the oscillator and loop filter components.

OSCILLATOR DESIGN

The design is fairly straight forward as only a single transistor is involved as shown in Fig.3. Any conventional oscillator configuration is possible except those requiring an output from the collector as this is internally decoupled to ground. When operating at lower frequencies, in this case 10.7MHz it is simpler to use a Hartley type oscillator with tapped coil rather than the Colpitts type employed in the satellite demodulator since the low value internal bias resistors will not allow direct connection to the tuned circuit without excessive damping.

When designing the oscillator the centre frequency (in this case 10.7MHz) must be obtained at the centre point of the linear range of the output amplifier (4.5V) on pin 14, and the slope of the oscillator voltage/frequency characteristic must allow the output amplifier to remain within its linear range at the maximum expected deviation of the input signal. In this case, the oscillator slope has been set at about 0.1MHz/Volt, giving a maximum output swing of 1.5V p-p for a 150kHz deviation FM signal. The 68pF and 27pF capacitors associated with the varicap diodes control the oscillator slope characteristic. An isolating network preventing loading of the tuned circuit by the amplifier output is required. Values must be chosen to present a high impedance at the oscillator operating frequency (10.7MHz) but allow feedback of the maximum demodulated frequency, say 20kHz for mono FM radio.

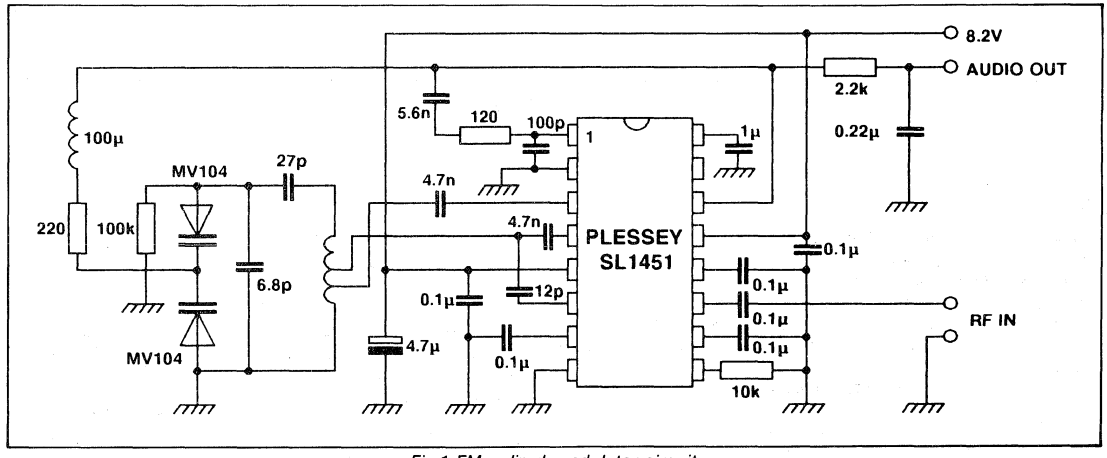


Fig.1 FM radio demodulator circuit

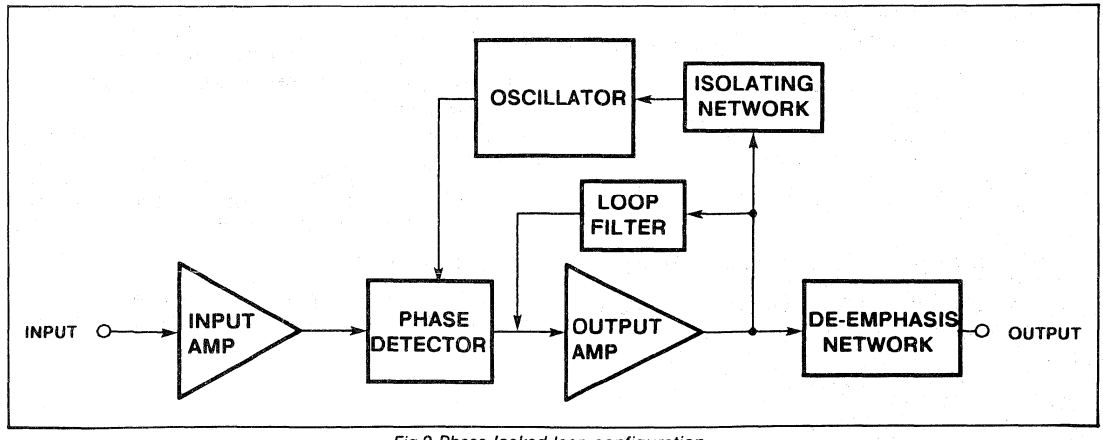


Fig.2 Phase locked loop configuration

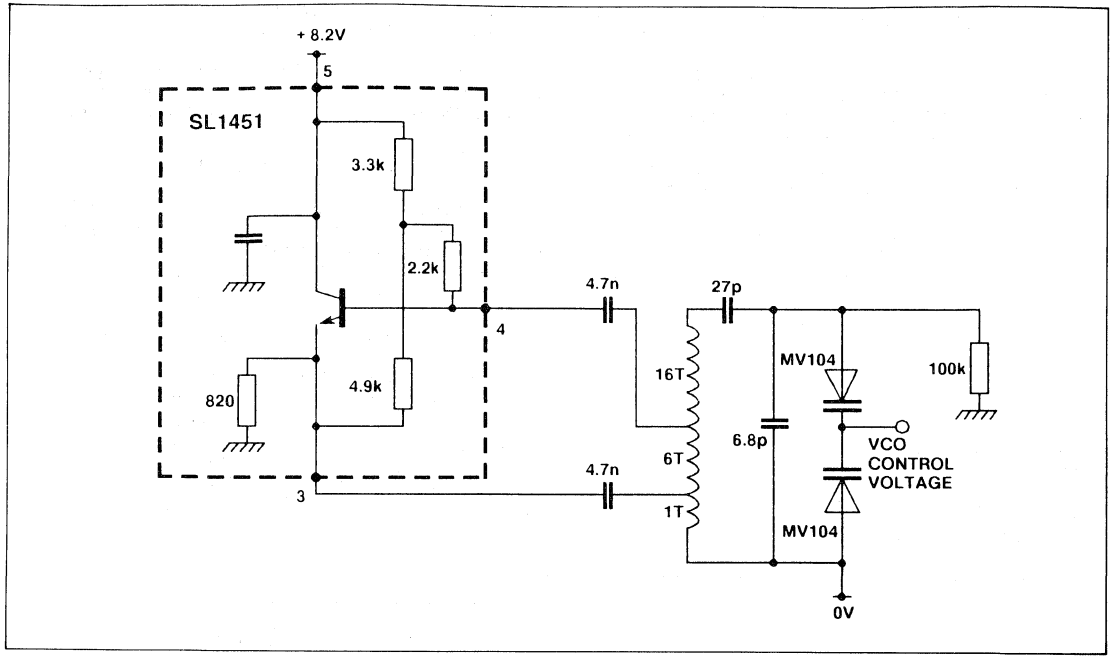


Fig.3 Oscillator configuration

LOOP FILTER

Having determined a suitable oscillator design, the most critical part of the design, the calculation of suitable values for the loop filter components is required. The equivalent circuit of the output amplifier with loop filter components is shown in Fig.4, and as can be seen, the choice of component is restricted to some extent, since R1 and part of R2 are internal.

The value of C can be determined from:

$$C = \frac{K_O K_D}{R1\ \omega n^2}$$

where: K_O is the phase detector gain in V/radian
K_D is the oscillator slope in radian/volt second
ωn is the natural loop bandwidth

Having determined the value of C, R2 can be obtained from:

$$R2 = \frac{2}{C\ \omega n}$$

where: is the damping factor
ωn is the natural loop bandwidth

For the prototype FM sound demodulator, the following parameters were used.

K_O = 0.5V/rad (from data sheet)
K_D = 0.628Mrad/Vs (100kHz/V oscillator design)
R1 = 570Ω (from Fig.4)
ωn = 0.314Mrad/Vs (50kHz natural loop bandwidth)
= 0.7071 (critical damping)

giving:

$$C = \frac{0.5 \times 0.628 \times 10^6}{570 \times (0.314 \times 10^6)} = 5.58nF$$

$$R2 = \frac{2 \times 0.7071}{5.58 \times 10^{-9} \times 10.314 \times 10^6} = 807.14\Omega$$

allowing for R2 int = 680Ω, R2 ext = 127Ω

All remaining components are non critical, being for coupling/decoupling purposes, apart from the 2.2k/0.022μF RC time constant on the output which provides a 50μs de-emphasis characteristic.

The demodulator was tested in a standard FM receiver using a CA3089 type limiting strip and quadrature demodulator. A connection was made between the input of the SL1451 and the output of the 3089 limiting strip on pin 8 thus bypassing the quadrature detector. Compared to the standard quadrature detector, a noticeable improvement in output signal to noise ratio at low input levels and an improvement in adjacent channel rejection was found.

SUMMARY OF SL1451 FM DEMODULATOR PERFORMANCE

Centre of IF		10.6MHz
Pull in range	10.5MHz to 10.75MHz Input	= -30dBm
Hold range	10.37MHz to 10.75MHz Input	= -30dBm
Input sensitivity for ±75kHz deviation at 15kHz		-30dBm
Distortion with ±75kHz deviation at 1kHz		<1%

CONCLUSION

The SL1451 is useful as a general purpose phase locked loop as well as in satellite TV FM demodulator applications.

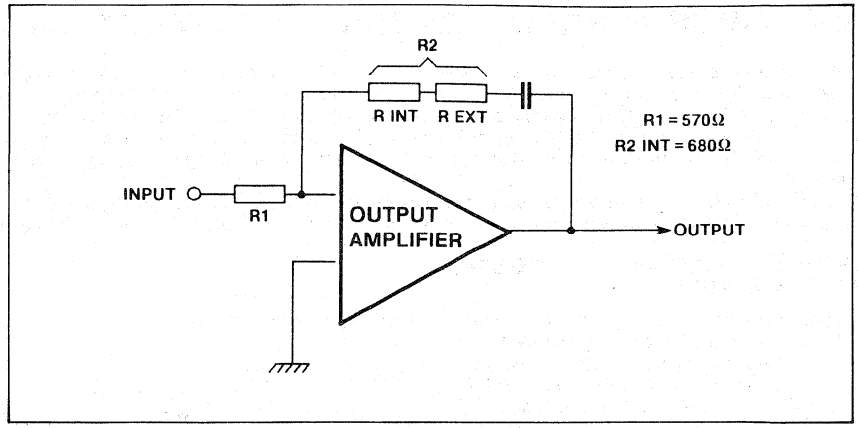


Fig.4 Equivalent circuit of amplifier with loop filter components

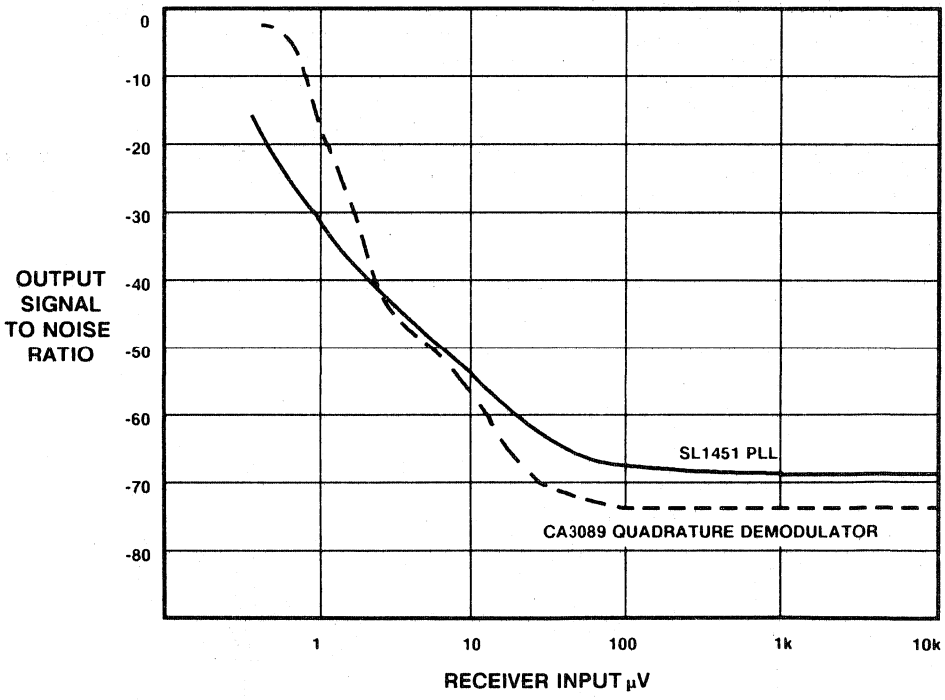


Fig.5

MV500 - CMOS Remote Control Transmitter

This application note describes a number of circuits using the MV500 which show how, by utilising various device characteristics, its use may be extended from the standard application circuit shown in the data sheet.

One of the main features of the MV500 is its ability to work at low supply voltages. Reduction in the supply voltage, however, has the drawback of limiting the range of the infra-red link. One possible method of improving this range is shown.

It is sometimes desirable to transmit data via a fixed wire link instead of using infra-red and two examples are given of this type of communication.

Occasionally, it is required to interface a remote transmitter to a logic system rather than a simple keyboard. In these cases, it is often desirable to present data to the transmitter in the form of a binary code and a method of achieving this is shown.

INCREASING THE RANGE OF AN INFRA-RED LINK AT LOW SUPPLY VOLTAGES

The intensity and therefore range of the infra-red link is determined by the current in the transmitting diodes. As the supply voltge is reduced, the minimum current available from the MV500 output drops from 50mA at 6V to 10mA at 3V. The transistor driving the transmitting diodes is required to work in a saturated mode with very low collector voltage in this application, particularly with the supply reduced to 3V. Under these conditions, the available gain to be expected from the output transistor will be low, preventing a suitable drive current being available for the transmitting diodes if the standard single transistor circuit is used.

Fig.1 shows a circuit suitable for use at lower voltages where an additional transistor is used to ensure adequate diode current. To ensure a low saturation voltage for the PNP transistor, the base drive is set to around a tenth of the required output current by the 8.2Ω resistor in series with the base. The requirements for saturation voltage are less critical for the NPN transistor which is operating at a collector current only one tenth that in the output transistor. In this case a much higher gain can be expected and the 10mA available from the MV500 is quite adequate.

The critical characteristics for the transistors used in the prototype are as follows:

PNP TYPE - ZTX749

Parameter	Typ.	Max.	Conditions
$V_{CE\ (SAT)}$	0.23V	0.5V	IC = 2A, IB = 200mA
hfe	75	150	IC = 2A, V_{CE} = 2V

NPN TYPE - ZTX650

Parameter	Typ.	Max.	Conditions
$V_{CE\ (SAT)}$	0.12V	0.3V	IC = 1A, IB = 100mA
hfe	100	200	IC = 500mA, V_{CE} = 2V

The peak current in the diodes is controlled by the 1Ω resistors in series. Using this value the current is approximately 750mA in each diode.

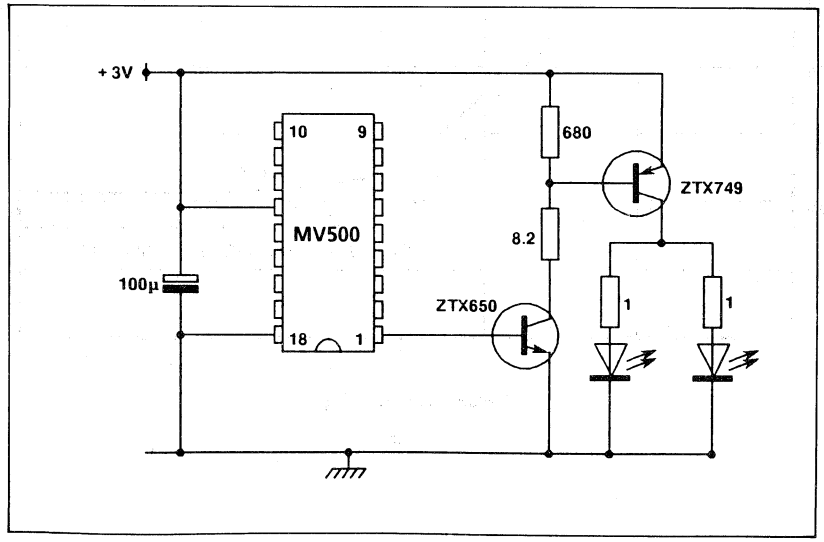


Fig.1 Increasing range of infra-red link

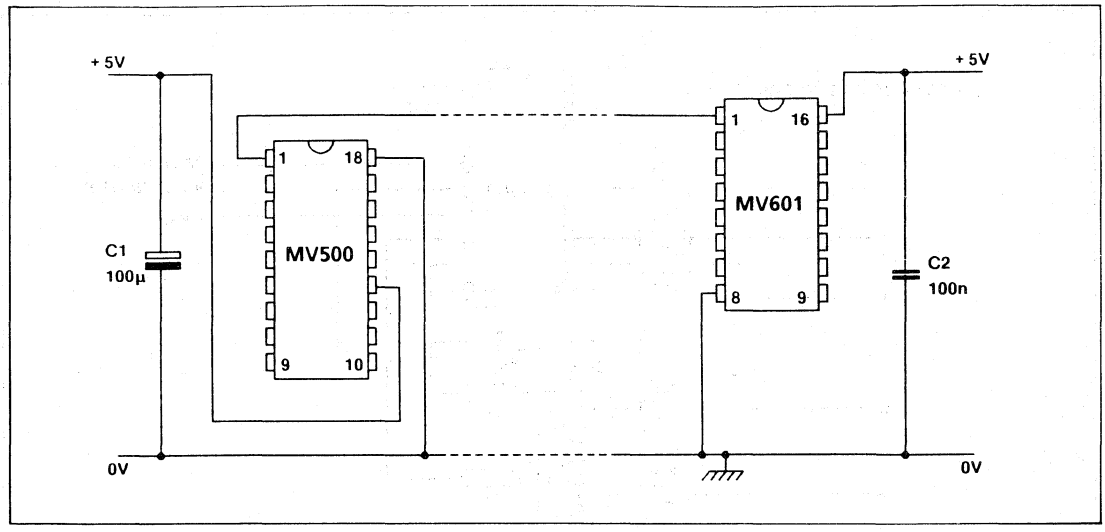


Fig.2 Two wire data link, separate supply

DATA TRANSMISSION OVER FIXED WIRE LINK

The MV500 is normally used to transmit remote data via an infra-red link, however, transmission over a dedicated wire link is possible. By using it in conjunction with an MV601 receiver, the MV500 may be connected via a simple two wire link as shown in Fig.2. The maximum distance between transmitter and receiver will be limited mainly by the noise picked up from the environment in which it is used.

The circuit of Fig.2 assumes that separate power supplies are available at the transmitter and the receiver, however it is necessary to common the two ground supplies of the transmitter and receiver.

If separate supplies are not available and a three wire link is undesirable, it is possible to use a two wire link for both power and data transmission. The circuit of Fig.3 shows how this may be achieved. Power for the MV500 is supplied along the line, with C1 keeping the supply to the MV500 constant. Output pulses from the MV500 turn TR1 on which shorts the power supply together temporarily and creates short negative going pulses at the input to the MV601 device. D1 isolates the supply to the MV500. Resistor R1 acts as the terminating impedance for the 100Ω twisted pair line, which allows communication over a reasonable distance.

INTERFACE TO LOGIC SYSTEM

One particular characteristic of the MV500 in its standard application is that if more than one key is pressed, the output code will be the logical OR of the separate codes for each key. Utilising this characteristic enables the MV500 to interface to a logic system and be driven from a binary code input. This is considerably simpler than attempting to simulate an 8 x 4 keypad.

Fig.4 shows how this may be achieved with the addition of just a few extra components. By driving the rate inputs directly, all three data rates may be utilised, giving the possibility of up to 96 separate codes. Driving both rate inputs low forces the device into its power down mode, simulating the 'all switches open circuit' condition. The circuit may be driven from standard CMOS outputs from the logic system.

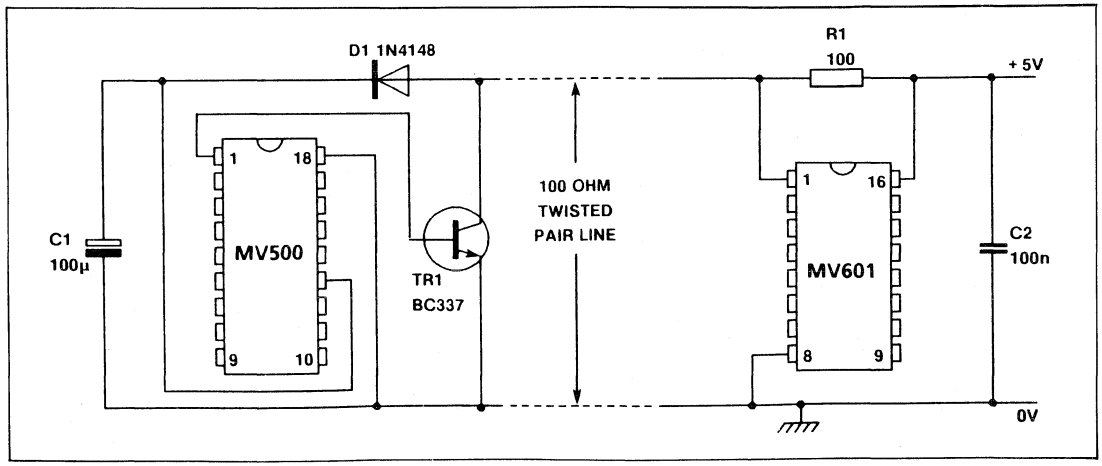


Fig.3 Two wire supply and data link

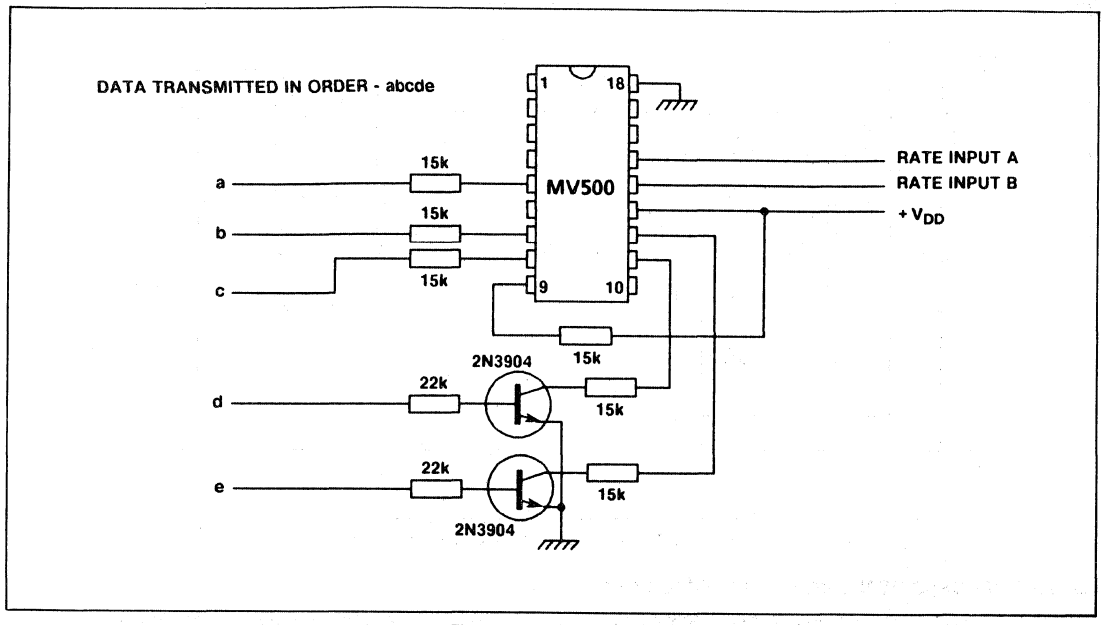
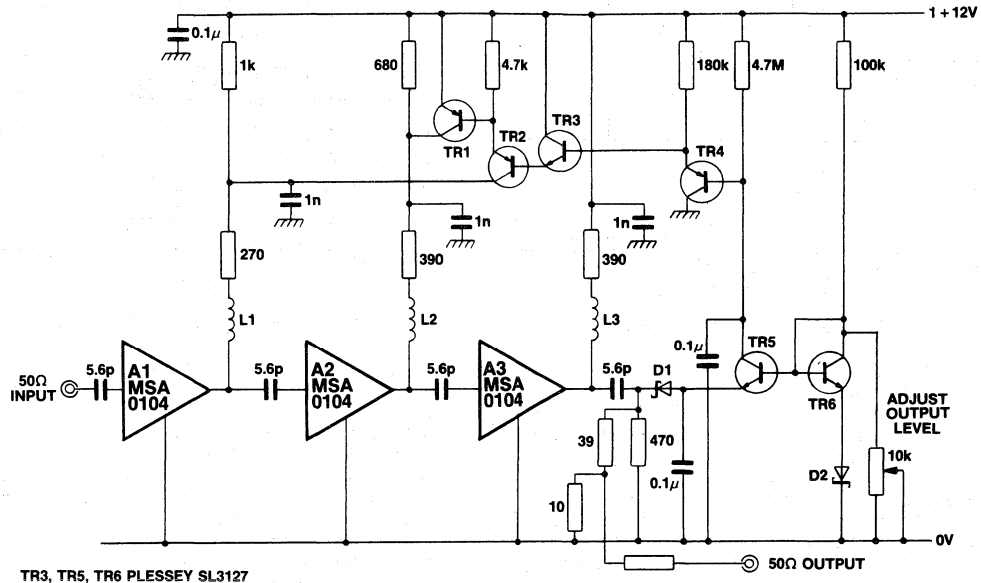


Fig.4 Binary coded input

A 600MHz AGC Controller IF Amplifier for the SL1455

From the SL1455 data sheet and application note, it will be seen that the degree of threshold extension and the video bandwidth are determined by the input level. For best results some method of accurately setting the input level and maintaining it under varying signal conditions is desirable. Various methods of controlling signal level are possible including the use of PIN diode attenuators, limiting amplifiers, etc. but the AGC system described here appears to offer a low cost flexible system with adjustable output level and wide AGC range (up to 45dB) which cannot be easily obtained by other means.



TR3, TR5, TR6 PLESSEY SL3127
TR1 2N3906
TR2 ZTX650
TR4 BC559
L1, 2, 3, 6½T 28 SWG 3mm DIA
D1, D2 BAT83

Max. gain without output attenuator typically 45dB
AGC control range typically 45dB
Max. output level 0dBm before attenuator

Fig.1

Gain is provided by a cascade of three Avantek MSA-0104 amplifiers with a gain of about 15dB per stage. The output from the third stage is detected and the resulting DC used to control the gain of the first two amplifier stages.

In order to allow detection at the low signal levels required by the SL1455, and to allow a degree of temperature compensation in the AGC point, a balanced arrangement of two transistors and Schottky diodes is used, increasing signal levels at the output producing an increasingly negative output at D1 anode. The negative output from the diode turns on TR5 which decreases the current in the first amplifier stage via the emitter followers TR2, 3 and 4 thus reducing the gain and maintaining constant output.

As the input signal is increased further, current in the first amplifier reduces until TR2 is no longer passing sufficient current to hold TR1 on, at which point the supply current to amplifier two is reduced, continuing the AGC action until TR1 is fully switched off.

The 1k and 680Ω resistors in parallel with TR1 and TR2 set a minimum current level in the amplifiers which is designed to allow a minimum gain level consistent with sufficient signal handling to drive subsequent stages. This together with the sequencing of the gain reduction system prevents overload in any of the amplifiers for all input signal levels within the dynamic range.

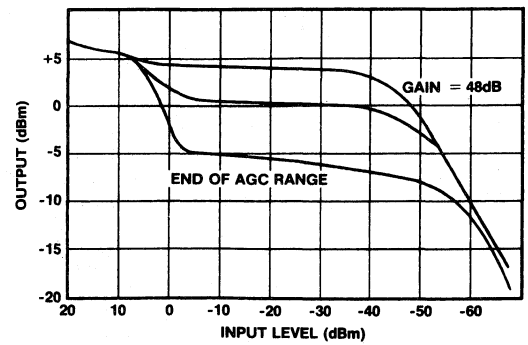


Fig.2 Characteristics of IF strip with AGC at 610MHz

Despite the balanced detector arrangement, it is still not possible to provide reliable AGC detection at the typical -20dBm level required for best threshold performance in the SL1455 and therefore a fixed T type attenuator is used to reduce the output level. Fine control of output level is provided by the potentiometer RV1 which allows adjustment for IC and other component tolerances.

An AGC System for Satellite Receiver IF Strips using the SL1451

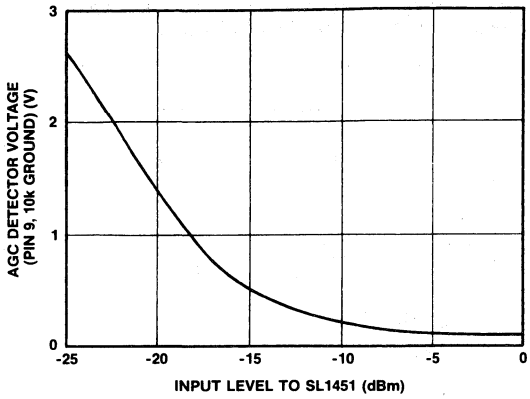


Fig.1 SL1451 AGC output characteristic

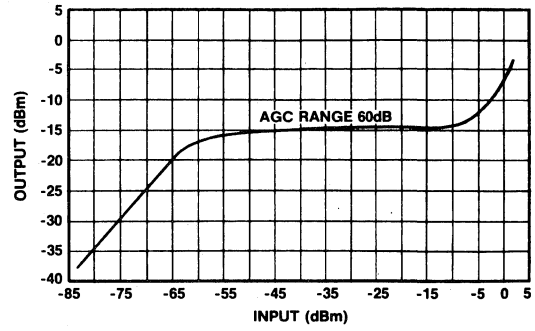


Fig.2 AGC characteristic of 612MHz IF strip

The detector output from the Plessey SL1451 has a characteristic described by Fig.1.

This characteristic can be used in an AGC circuit as shown in Fig.3. The maximum gain of the IF circuit is 45dB and this occurs when TR1 is switched off, hence TR2, TR3, TR4 provide the current for the first two amplifying stages. the gain of these stages can be reduced by reducing their supply current. As TR1 is gradually turned on the current supply to the first amplifier is reduced until all the current is supplied via the 1k resistor, then the second stage current is reduced until all the current for it is supplied via the 680Ω resistor. As the gain is reduced the detector output level increases and TR1 is switched further off, thus stabilising at a given output level. The gain of the system is set by the 100Ω and 180k resistors and the system is damped by the 180k and 4.7μF time constant. The output level is adjusted by altering the switch on point of TR1. This is done by varying the base bias of TR1 (via the 2.2k variable resistor). -15dB is the optimum level for the input to the SL1451.

The IF filter can either be situated after the IF strip or between amplifying stages. It may be advantageous to place the filter before the final amplifying stage as this reduces the out of band noise and adjacent channel levels which could deteriorate the performance of the final amplifier.

The IF strip provides a 60dB AGC range which is more than adequate for all satellite receiver applications (see Fig.2).

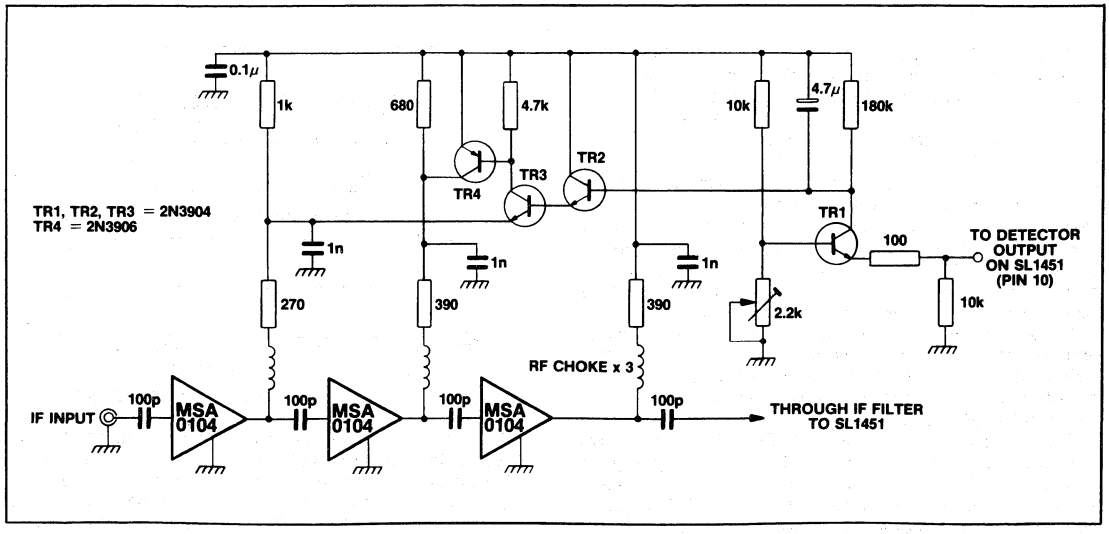


Fig.3 IF strip for satellite receiver, incorporating an AGC using the detector from the SL1451 (AGC range 60dB)

More Codes from the MV601

The Plessey MV500/MV601 form a remote control transmitter/receiver pair normally giving 32 codes. Where more than 32 codes are required, there are various methods of obtaining more provided the use of a shift key is acceptable. Using this method, a single transmitter could be used to control two pieces of equipment, each requiring up to 32 codes. The shift function uses a latched switch on the transmitter to select a different transmission rate. Alternatively this same shift function can be utilised in a single piece of equipment with two modes of operation, for instance in a combined TV receiver and video recorder where the same set of transmitter switches could be used to control both TV and video recorder, reducing the complexity and cost of the transmitter circuit.

The most obvious method of achieving this form of operation is to use an MV601 circuit for each 32 code set, and where a single transmitter is used for several equipments, this is essential. Selection of the various transmission rates is achieved simply by hard wiring the rate inputs on the MV601s to match the transmitter.

When a single piece of equipment with several operating modes is being designed, some economies in the circuit are possible as shown in the circuit diagrams Figs. 1 to 3. Fig.1 shows a scheme which can use up to three MV601 circuits with three shift levels at the transmitter giving a total of 96 possible codes. The MV601 PPM inputs are connected in parallel to a single SL486 and only a single ceramic resonator is used since the oscillator output of one circuit can drive the oscillator inputs of the other two. Only a single RC time constant is required for power on clear as again these inputs can be connected in parallel. The outputs from the MV601 form a 15 bit bus which could be read by a microprocessor when interrupted by the combined data ready signal.

Fig.3 shows a slightly modified system where the data ready outputs from each chip are connected to the output enable inputs forcing the data outputs into the high impedance state when no valid data is received. The data outputs of the three chips can now be connected in parallel since only one rate can be transmitted at any one time and only the receiver set to that rate will respond. Which chip is responding can be determined from the separate data ready signals.

When only a single shift function is required giving two sets of 32 codes, a simpler circuit using only a single MV601 is possible as shown in Fig.3.

The output from the Plessey SL486 pulse stretched output is fed to the base of TR1 which provides an inverted lower impedance output which is fed to the MV601 PPM input. TR1 output is also fed to a simple filter, R2, R3 and C1 which produces a DC level dependent on the rate of received IR pulses. When the input rate is sufficient, the voltage rises to a level at which TR2 is switched on and TR3 off, taking the B rate input to the MV601 high. Using this method with automatic switching of the rate inputs dependent on the data transmission rate, the MV601 can be made to respond to the highest and lowest data rates selectable, provided care is taken with selection of the time constants in the SL486 pulse stretch circuit and in the filter components R2, R3 and C1. TR3 also provides the sixth output bit giving the indication of shift state. The values shown are correct for use with 500kHz ceramic resonators on the MV500 and MV601. At the fastest rate setting, when transmitting an all ones code, the SL486 pulse stretch capacitor should give approximately a 1:1 mark space ratio at the SL486 stretch output. Due to noise received by the SL486, the output from TR3 may bounce when no signal is transmitted, but provided the data is only used when data ready is true, the circuit operation should not be affected.

A transmitter circuit with single shift function giving 64 codes and suitable for use with the single MV601 application shown in Fig.3 is shown in Fig.4. An additional shift switch connected to pin 15 will allow the transmitter to be used with three levels of shift providing up to 96 codes from the applications shown in Figs.1 and 2.

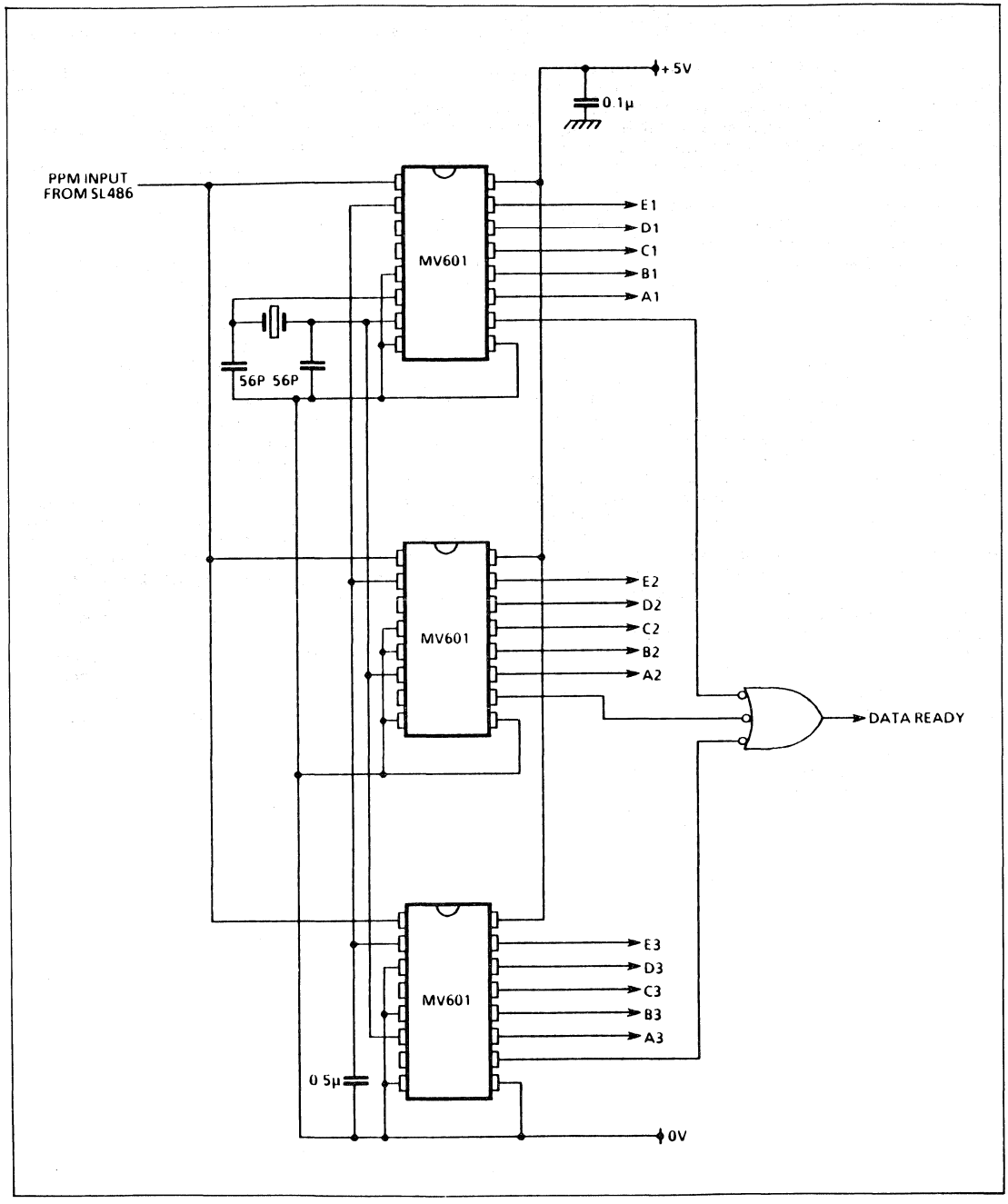

+5V
0.1µ
PPM INPUT
FROM SL486
MV601
E1
D1
C1
B1
A1
56P 56P
MV601
E2
D2
C2
B2
A2
DATA READY
MV601
E3
D3
C3
B3
A3
0.5µ
0V

Fig.1

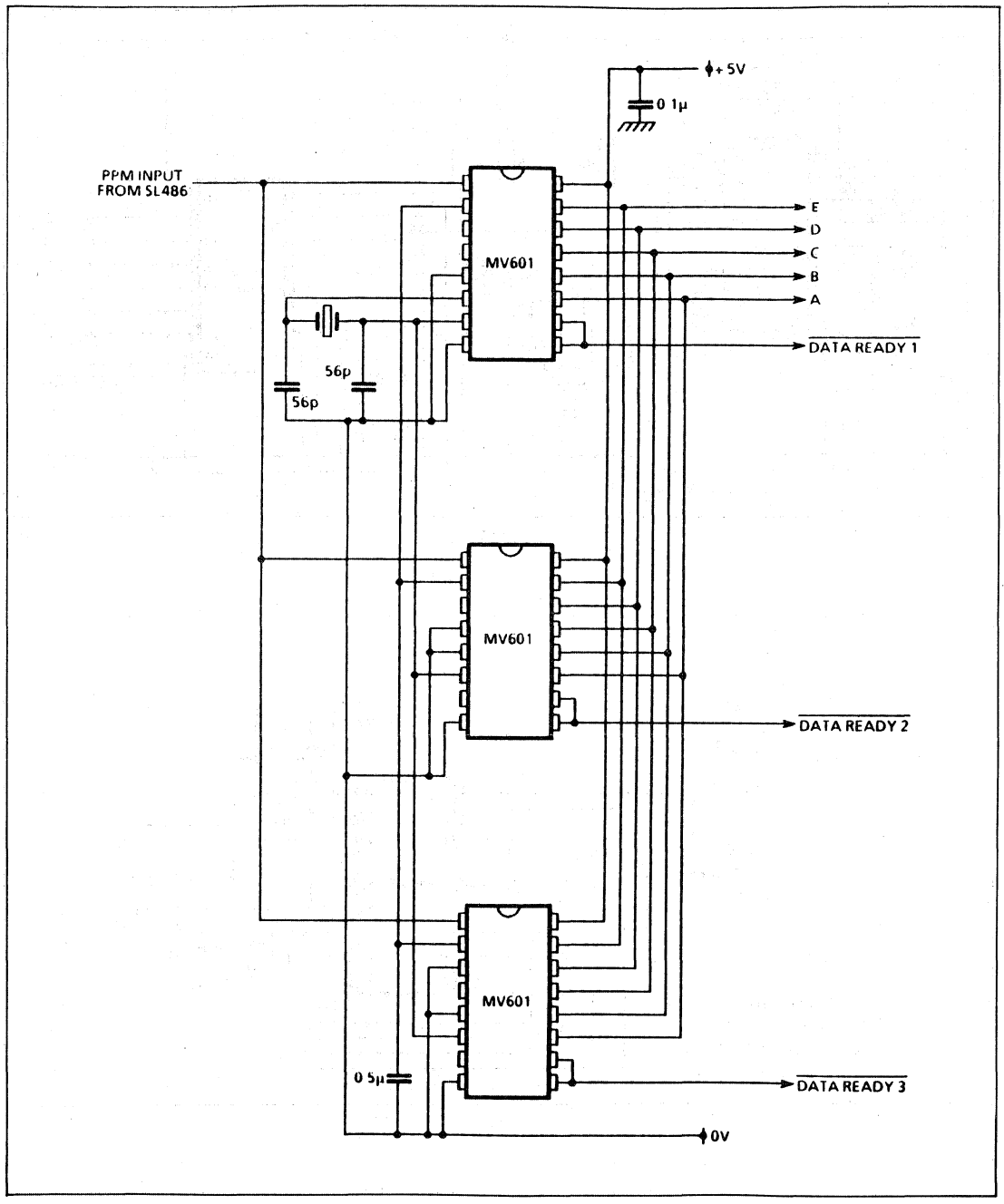

+5V
0 1µ
PPM INPUT
FROM SL486
MV601
E
D
C
B
A
DATA READY 1
56p
56p
MV601
DATA READY 2
MV601
0 5µ
DATA READY 3
0V

Fig.2

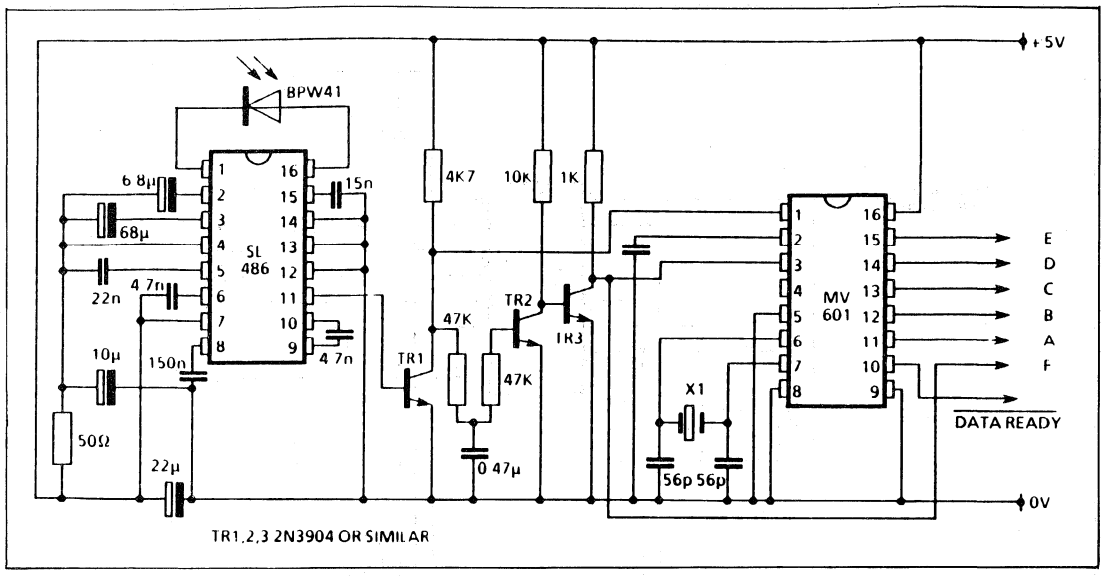

+5V
BPW41
6 8µ
68µ
22n
4 7n
10µ
150n
50Ω
22µ
15n
4 7n
SL 486
4K7
10K
1K
47K
47K
TR1
TR2
TR3
0 47µ
X1
56p 56p
MV 601
E
D
C
B
A
F
DATA READY
0V
TR1,2,3 2N3904 OR SIMILAR

Fig.3

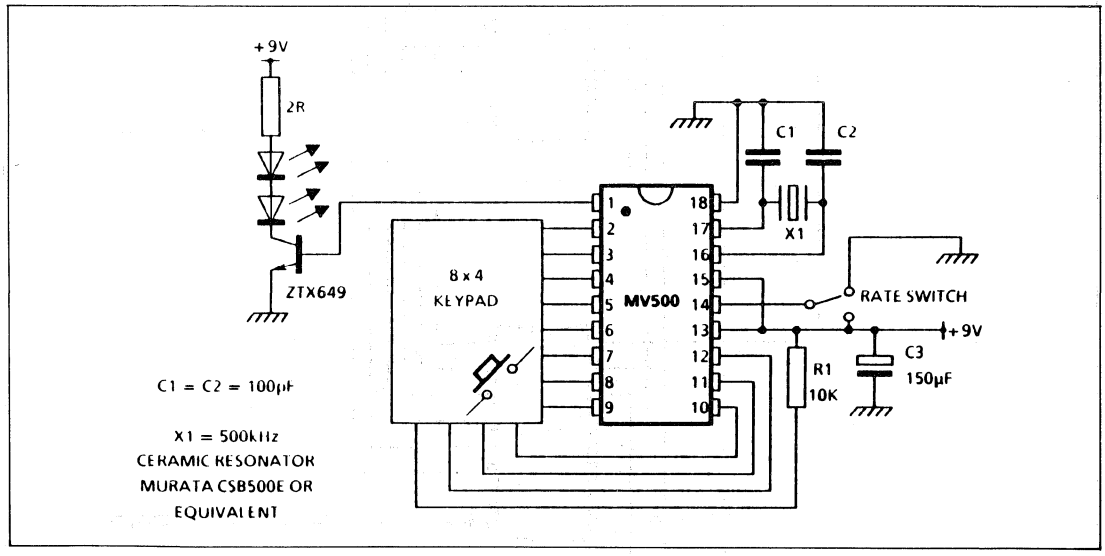

+9V
2R
ZTX649
8 x 4
KEYPAD
MV500
C1
C2
X1
RATE SWITCH
+9V
R1
10K
C3
150µF
C1 = C2 = 100pF
X1 = 500kHz
CERAMIC RESONATOR
MURATA CSB500E OR
EQUIVALENT

Fig.4

MV1812 Interface to an IBM PC

The Plessey MV1812 is a high speed device for decoding Teletext data from a sliced video signal to an 8-bit data bus. The design allows an easy interface to a computer bus. This note describes the interface of the MV1812 Teletext decoder to an IBM PC or equivalent. The complete board is capable of receiving all pages and packets being transmitted to the 'World System Teletext Specifications'. This includes packet 31, Datacast, being received at the same time as standard packets.

The circuit, (Fig.1), has been designed to use, as far as possible, the hardware already present on an IBM PC. These include a DMA channel (channel 1) and an interrupt request line (IRQ3). These two functions are normally used by a second serial port, therefore if present, this must be removed before the Teletext board can be used.

All control of the MV1812 is via the Expansion bus. The MV1812 requires sixteen addresses on the I/O port. No line buffers are required as the circuit uses HCT chips with a maximum load of two per line. The circuit used around the MV1812 is the standard circuit for the chip and is covered in other application notes. The interface to the bus can use a single chip to generate the valid address e.g. 240 (hex). As the MV1812 has a R/$\overline{W}$ line the $\overline{IOR}$ and $\overline{IOW}$ signals must also be used to generate the valid chip enable for the MV1812.

A board has been manufactured to the specification described in this application note, which is available for demonstration use. All the development work was carried out on an Amstrad PC1512 running at an equivalent speed of 6MHz. All references to an IBM PC refer equally to a clone of this computer.

The video signal is decoded using the Plessey SL9100 data slicer. The video signal can be in the range 1.5V to 4.5V p-p, it should be coupled with a 680nF capacitor. The SYNC OUT signal from the SL9100 is stretched using an RC network to ensure that the $\overline{VALIN}$ signal only goes high at the start of the clock run-in or soon after. This ensures that the MV1812 does not use any noise on the line as the start of the clock run-in signal. Typical values for the RC network are 50kΩ preset and 1nF. The MV1812 is programmed using the microprocessor (details of internal registers are given in the data sheet). When the MV1812 detects a new page being transmitted, it starts to transfer data into the data buffer, at the same time pulling the $\overline{EVENT}$ line low interrupting the microprocessor. The microprocessor must respond by reading the $\overline{EVENT}$ register to detect a valid header. If it decides to accept the page, the DMA is programmed for 42 bytes continuous transfer of data. The DMA must not transfer more than 42 bytes of data otherwise memory corruption will occur.

Once programmed, the DMA waits for a request on the DREQ1 line. This request to transfer data is only generated if both the WLINE and OPVAL are high when the VALIN goes low. WLINE is high when the line being received is part of the requested page. OPVAL will go high on the 15th byte of data unless a byte with an uncorrectable Hamming error is received. It is reset at the end of every line. In the event of an uncorrectable Hamming failure, it is likely that some data may have already been latched into the data buffer. If WLINE or OPVAL are not both high when $\overline{VALIN}$ goes low, the Q output of the D type stays low thus pulling the MR pin of the data buffer low for the length of the $\overline{VALIN}$ signal. When the DMA receives the DREQ1 request, it starts to transfer 42 bytes of data from the data buffer to memory. The DREQ1 request is cancelled when the DMA pulls the EOP (end of process) flag low. Once the DMA has transferred all 42 bytes, it pulls the EOP line low resetting the DMA request. Control of the data buffer during the data transfer must be by the DMA chip controlling both CO and $\overline{OE}$ lines of the data buffer. It should be noted that when $\overline{OE}$ goes low, the first byte of valid data is available on the outputs of the data buffer. This byte of data must be read before data is shifted by CO. DREQ1 request.

The software to drive the board has been written exclusively in 8088 assembler code to produce fast code and direct access to I/O ports and internal registers. The normal PC is still slow in certain parts of the program. To ensure that these section of the program will work all interrupts have been disabled and the memory refresh cycles have been reduced in priority during the critical part of the program.

A typical program to control the MV1812 is split into 7 parts. SETUP, PAGE SELECT, EVENT HANDLING, DMA RESET, DISPLAY. All addresses given are in HEX. The sections are described in the order that they would normally work. If the decoder is going to be used just to receive packet 31, certain sections will not be required as explained in 'Notes on receiving just packet 31', below.

SETUP

This section sets up the IBM PC to control the MV1812. The main sections that need setting up are the DMA interface and the Interrupt handling device. These two devices are the INTEL 8237 and 8259 respectively. For detailed information on these devices see the relevant data sheets. The DMA controller is set up for channel 1 to transfer 42 bytes to a start address of 00. The segment that the DMA transfers the data to, is set using register 83. The command register that effects all DMA channels is modified to allow rotating priority. This effectively gives the DMA request from the MV1812 board, higher priority than memory refresh. As the DMA transfers from channel 1 only occupy a small percentage of the clock time, the system remains uncorrupted. The mode register for channel 1 is set up for: read transfer, autoinitialization disabled, address increment, and demand mode. The $\overline{EVENT}$ interrupt is IRQ 0C. The procedure to execute this interrupt needs to be pointed to by the interrupt controller, and the interrupt enabled.

PAGE SELECT

The MV1812 receives a page as selected in the three PGREQ registers and the SELCON register. Full details are given in the data sheet. If just packet 31 is required the magazine should be set to the required magazine and the page can be set to, say, BB. This is normally a non-existent page so the MV1812 will only receive Packets 31 and Packet 30.

EVENT HANDLING

This section responds to the hardware interrupt 0C. The routine reads the event register on the MV1812 to determine the start of page. All other events are returned without any further processing. If a start of page is detected the program unmasks the DMA channel allowing data transfer to occur. At the end of any interrupt the program should normally clear the interrupt request on the 8259 interrupt controller and unmask the interrupt register. As the program requires as much speed at this point as possible this is not done. The interrupt request is cleared but the interrupt is left unmasked to ensure that no new interrupts affect the transfer of data.

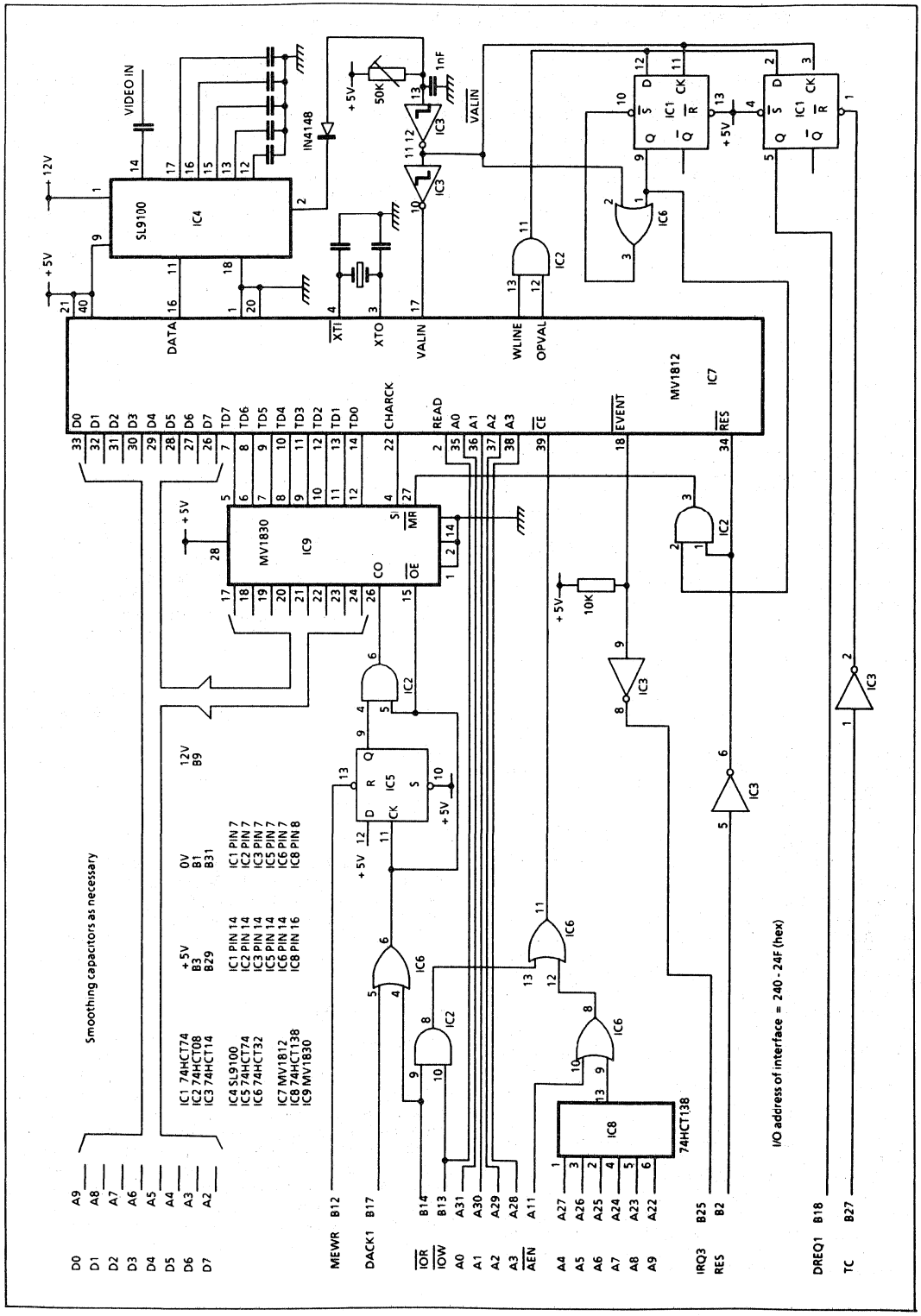


Fig.1 Circuit diagram for connection of MV1812 to IBM PC or equivalent

DMA RESET/MAIN PROGRAM

This section is not a separate procedure as are the other sections. It runs as part of the main program to ensure that the greatest speed is obtained. The program waits for an event to indicate the reception of a new packet. This is indicated by the setting of bit 01 in register DS. Once the new page indicator has been set, the program will reset the DMA whenever the EOP is detected for channel 1 by reading the register 08.

DISPLAY

The Teletext data consists of eight bit data bytes. This data is typically either odd parity ASCII data or Hamming encoded data, plus a few special bytes in certain packets. The Hamming bytes need to be decoded. This is done using a look-up table. ASCII characters need to have the eighth (parity) bit removed to generate normal ASCII characters. As the IBM PC does not have a Teletext display mode, the control codes 00 - 1F have to be individually programmed.

NOTES ON RECEIVING JUST PACKET 31

If the decoder is to receive packet 31 exclusively, there is no need to use the interrupt. The MV1812 is programmed as described above and the DMA mask removed immediately. This allows the IBM PC to receive all packets 30 and 31 as they are received. It may be possible not to use the DMA interface at all if only one packet per TV frame is to be received, as is current transmission practice, by reading data directly out of the MV1830. This method is not generally recommended due to possibe future plans to transmit more than one packet 30 or 31 per frame, typically at night.

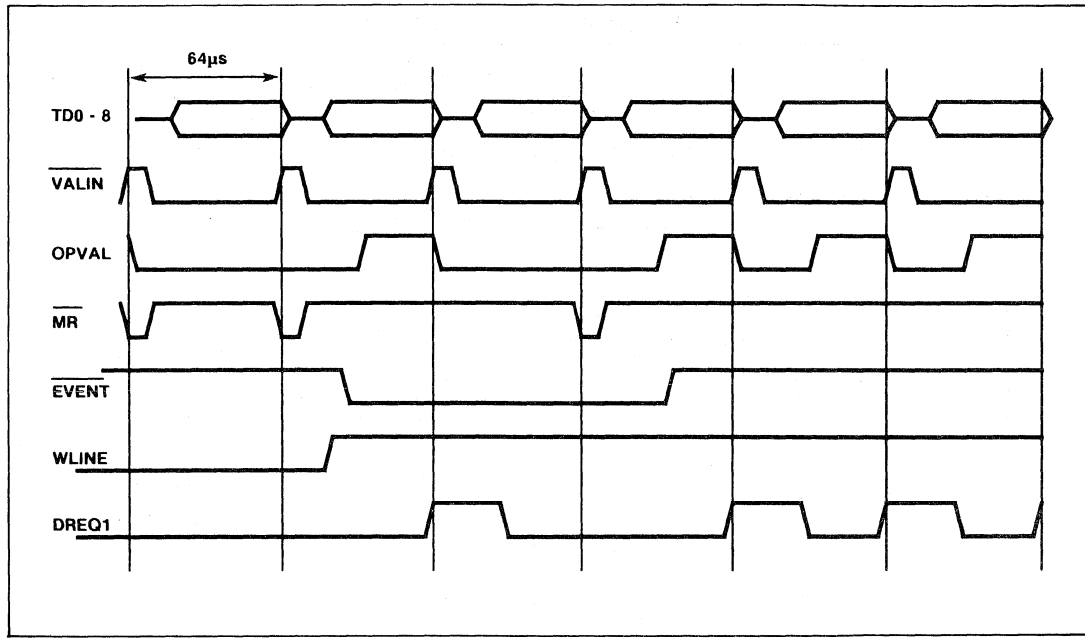


Fig.2 Example timing diagram

MV1812 DMA Interface

The Plessey MV1812 is a high speed CMOS circuit capable of decoding any World System 625 line Teletext transmissions. The circuit operates on serial Teletext data provided by the Plessey SL9100 Data Slicer and provides parallel words of data if the transmitted data matches the selection criteria set in the internal registers.

Teletext data is received by the MV1812 at a rate of 6.9375Mbit/sec. If connected directly to a microprocessor, a cycle time of less than 170ns would be required just to transfer data from the MV1812 to memory without allowing any time for data conversion. The other alternative is to have memory that is capable of receiving data at 770kbytes/sec. If Teletext is only being transmitted on 6 lines, it is possible to use five low cost Teletext Data Buffers, MV1830, that allow the host microprocessor to process the data during the rest of the TV field.

Full-field Teletext is now being used in a variety of applications where a high throughput of data over a low cost transmission medium is required. Due to this high data rate, a DMA (Direct Memory Access) device should be used to transfer data from a single data buffer to memory. This method only requires the ttention of the microprocessor once during each line received. A single data buffer is still used to ensure that only valid data is transferred to the memory.

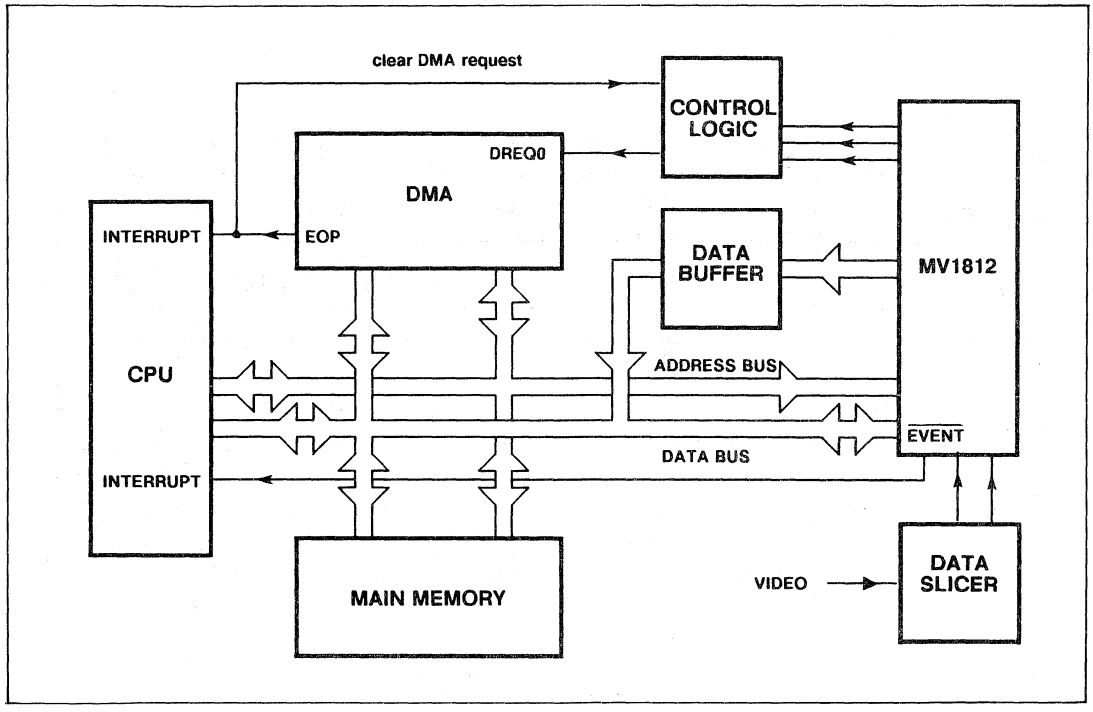


Fig.1 DMA transfer block diagram

This application note describes in more detail the circuit for DMA data transfer. Fig.1 shows a block diagram of a DMA circuit. The following notes assume that the MV1812 is to operate in a system which conforms to the principles of teletext transmissions as described in the 'World System Teletext Specification'. The circuit shown in Fig.2 shows the basic DMA interface to the MV1812 using an INTEL 8051 microprocessor. The actual circuit details of the CPU, memory and DMA chips have been omitted as this depends upon the microprocessor used.

A video signal is decoded using the SL9100 data slicer. The video signal can be in the range 1.5V to 4.5V p-p, it should be coupled with a 680nF capacitor. The SYNC OUT signal from the SL9100 is stretched using an RC network to ensure that the VALIN signal only goes high within the clock run-in or soon after. This ensures that the MV1812 does not use any noise on the line as the start of the clock run in signal. Typical values for the RC network are 8.2kΩ and 1nF. The MV1812 is programmed using the microprocessor (details of internal registers are given in the data sheet). When the MV1812 detects a new page being transmitted, it starts to transfer data into the data buffer, at the same time pulling the $\overline{\text{EVENT}}$ line low interrupting the microprocessor. The microprocessor must respond by reading the $\overline{\text{EVENT}}$ register to detect a valid header. If it decides to accept the page, the DMA is programmed for 42 bytes continuous transfer of data. The DMA must not transfer more than 42 bytes of data otherwise memory corruption will occur.

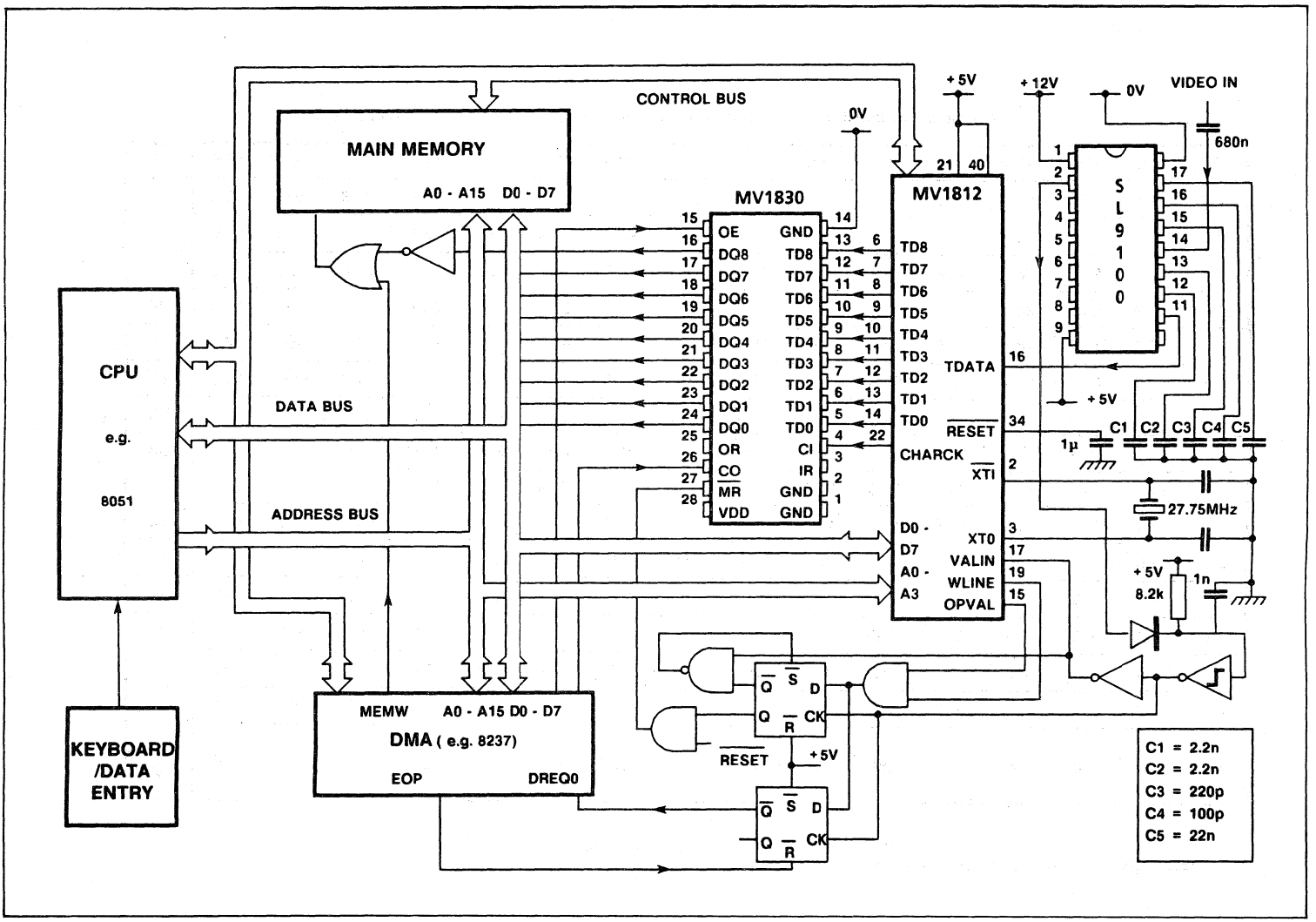


Fig.2 MV1812 DMA application circuit

Byte Number 4

Byte 5	HAMM BYTE	15	02	49	5E	64	73	38	2F	D0	C7	8C	9B	A1	B6	FD	EA
	15	0-0	1-0	2-0	3-0	4-0	5-0	6-0	7-0	0-1	1-1	2-1	3-1	4-1	5-1	6-1	7-1
	02	0-2	1-2	2-2	3-2	4-2	5-2	6-2	7-2	0-3	1-3	2-3	3-3	4-3	5-3	6-3	7-3
	49	0-4	1-4	2-4	3-4	4-4	5-4	6-4	7-4	0-5	1-5	2-5	3-5	4-5	5-5	6-5	7-5
	5E	0-6	1-6	2-6	3-6	4-6	5-6	6-6	7-6	0-7	1-7	2-7	3-7	4-7	5-7	6-7	7-7
	64	0-8	1-8	2-8	3-8	4-8	5-8	6-8	7-8	0-9	1-9	2-9	3-9	4-9	5-9	6-9	7-9
	73	0-10	1-10	2-10	3-10	4-10	5-10	6-10	7-10	0-11	1-11	2-11	3-11	4-11	5-11	6-11	7-11
	38	0-12	1-12	2-12	3-12	4-12	5-12	6-12	7-12	0-13	1-13	2-13	3-13	4-13	5-13	6-13	7-13
	2F	0-14	1-14	2-14	3-14	4-14	5-14	6-14	7-14	0-15	1-15	2-15	3-15	4-15	5-15	6-15	7-15
	D0	0-16	1-16	2-16	3-16	4-16	5-16	6-16	7-16	0-17	1-17	2-17	3-17	4-17	5-17	6-17	7-17
	C7	0-18	1-18	2-18	3-18	4-18	5-18	6-18	7-18	0-19	1-19	2-19	3-19	4-19	5-19	6-19	7-19
	8C	0-20	1-20	2-20	3-20	4-20	5-20	6-20	7-20	0-21	1-21	2-21	3-21	4-21	5-21	6-21	7-21
	9B	0-22	1-22	2-22	3-22	4-22	5-22	6-22	7-22	0-23	1-23	2-23	3-23	4-23	5-23	6-23	7-23
	A1	0-24	1-24	2-24	3-24	4-24	5-24	6-24	7-24	0-25	1-25	2-25	3-25	4-25	5-25	6-25	7-25
	B6	0-26	1-26	2-26	3-26	4-26	5-26	6-26	7-26	0-27	1-27	2-27	3-27	4-27	5-27	6-27	7-27
	FD	0-28	1-28	2-28	3-28	4-28	5-28	6-28	7-28	0-29	1-29	2-29	3-29	4-29	5-29	6-29	7-29
	EA	0-30	1-30	2-30	3-30	4-30	5-30	6-30	7-30	0-31	1-31	2-31	3-31	4-31	5-31	6-31	7-31

Table 1 Received Hamming bytes 4 and 5 showing their conversion to magazine-packet number

Once programmed, the DMA waits for a request on the DREQ0 line. This request to transfer data is only generated if both the WLINE and OPVAL are high when the $\overline{VALIN}$ goes low. WLINE is high when the line being received is part of the requested page. OPVAL will go high on the 15th byte of data unless a byte with an uncorrectable Hamming error is received. It is reset at the end of every line. See Fig.3 for timing diagram. In the event of an uncorrectable Hamming failure, it is likely that some data may have already been latched into the data buffer. If WLINE or OPVAL are not both high when $\overline{VALIN}$ goes low, the Q output of the D type stays low thus pulling the $\overline{MR}$ pin of the data buffer low for the length of the $\overline{VALIN}$ signal. When the DMA receives the DREQ0 request, it starts to transfer 42 bytes of data from the data buffer to memory. The DREQ0 request is cancelled when the DMA pulls the EOP (end of process) flag low.

Control of the data buffer during the data transfer must be by the DMA chip controlling both CO and $\overline{OE}$ lines of the data buffer. It should be noted that when $\overline{OE}$ goes low, the first byte of valid data is available on the outputs of the data buffer. This byte of data must be read before data is shifted by CO.

Once the DMA has transferred all 42 bytes, it pulls the EOP line low resetting the DREQ0 request and interrupting the microprocessor indicating that another line of valid data has been transferred to memory. The microprocessor should reset the DMA chip ready for the next line of data unless an $\overline{EVENT}$ has been signalled to the microprocessor indicating the end of the page.

The TD8 signal is used by the MV1812 to indicate a valid word of data by checking the parity of the incoming data. A high on this line indicates valid data. If parity is disabled on the MV1812 this pin will still be high. By logically ORing this signal with the $\overline{WR}$ signals of the CPU and DMA, it is possible to ensure that only correct data is placed in memory.

The speed of the programs must be carefully monitored to ensure that no data is lost. The most critical timing is at the start of a new page. The microprocessor must receive and process an $\overline{EVENT}$ interrupt and program the DMA chip while still allowing time for data transfer from data buffer to memory during the transmission of one line i.e. 64μs. The microprocessor used on this demonstration board was an INTEL 8051 with a clock frequency of 12MHz which gives ample processing power for this requirement.

The data stored in external memory still contains some Hamming encoded bytes. In packet zero, bytes four to thirteen are Hamming encoded and in packets 1 to 24 only bytes 4 and 5 are Hamming encoded. Bytes 1 to 3 of each packet are not available from the MV1812 as these are only used for clock run in and framing. Table 2 gives the Hamming code for hex and decimal values. Table 1 shows the relationship between the Hamming codes in bytes 4 and 5 and the packet and magazine being received. By using a software look-up table, the microprocessor has time to convert each line of data as it is transferred to memory into decoded data.

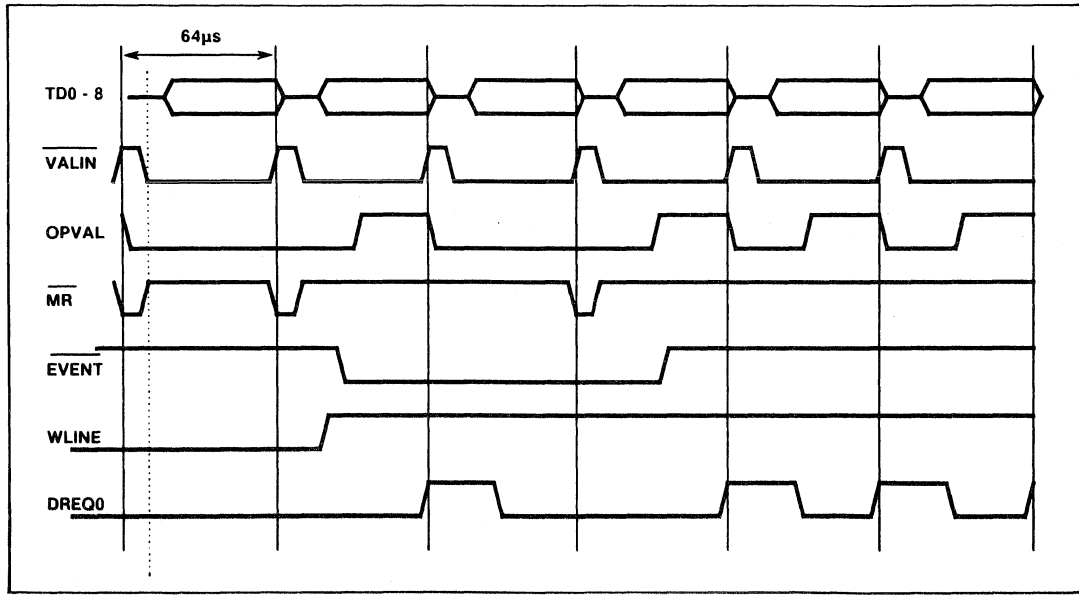
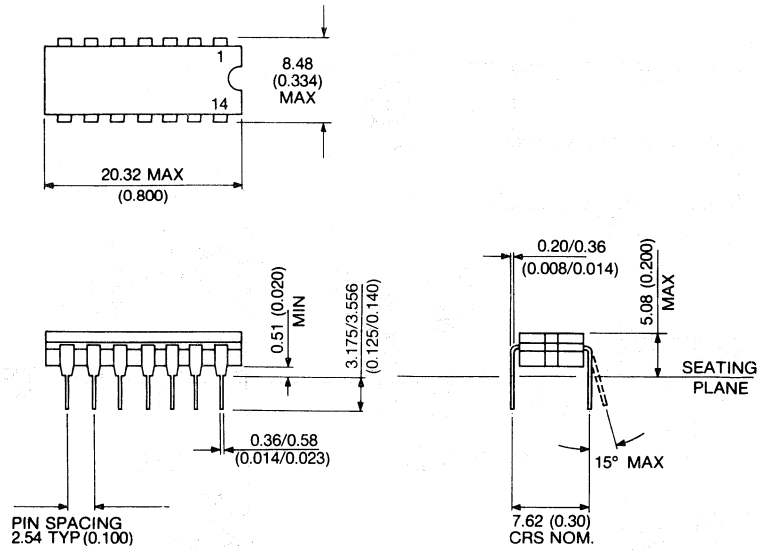


Fig.3 Example timing diagram

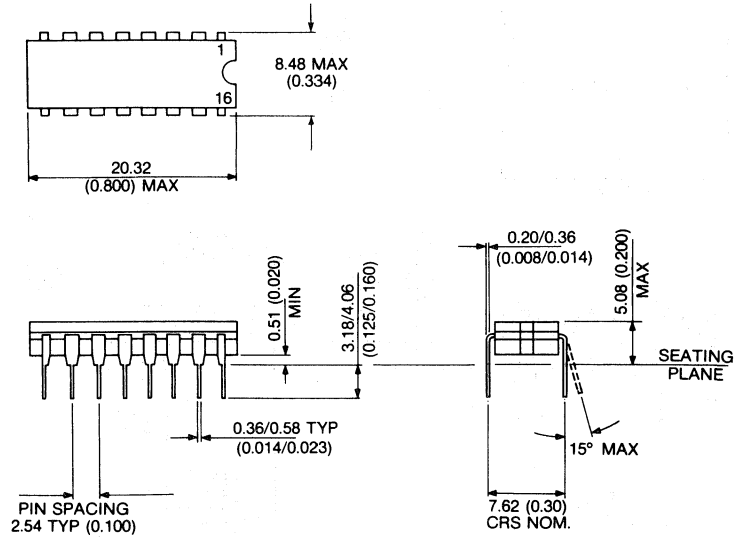
HAMMING CODE	15	02	49	5E	64	73	38	2F	D0	C7	8C	9B	A1	B6	FD	EA
DECIMAL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Table 2

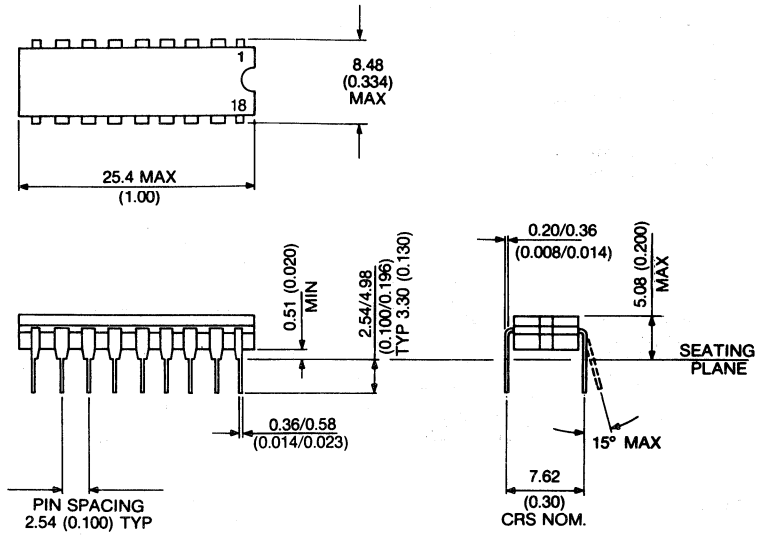
Package Outlines



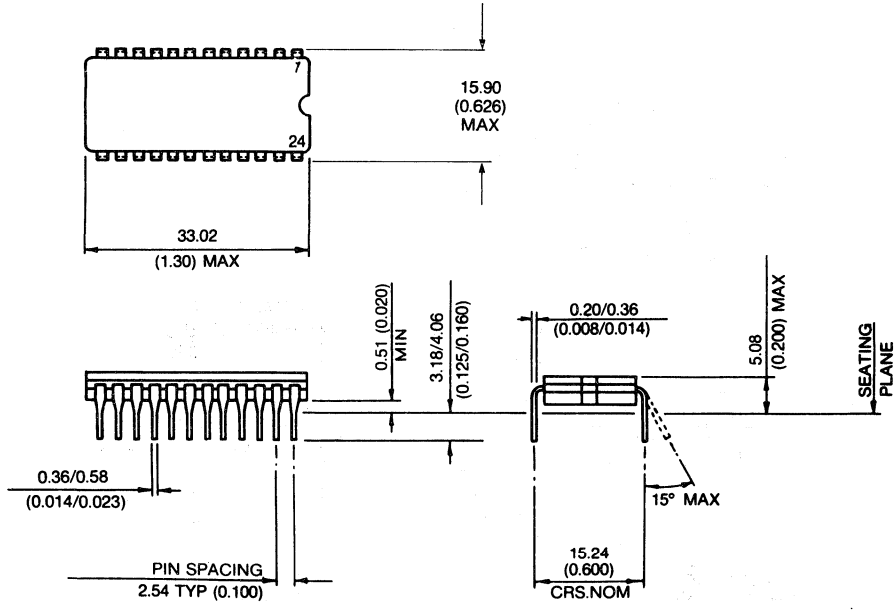
14-LEAD CERAMIC DIL - DG14



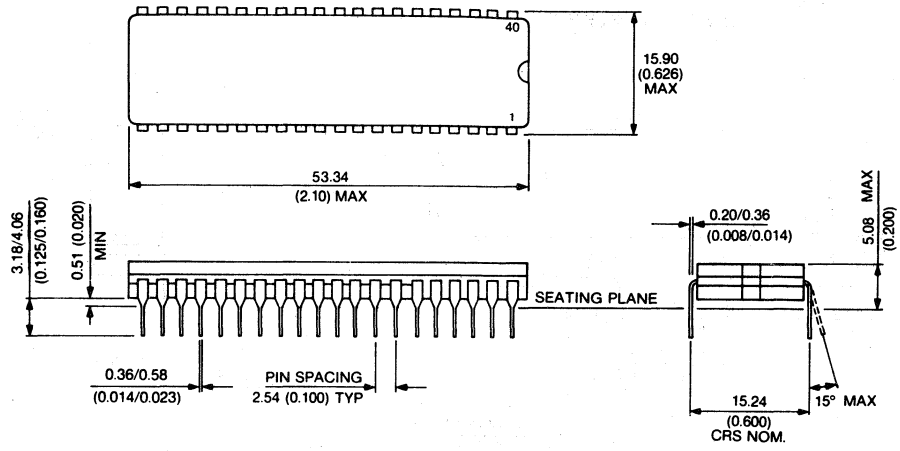
16-LEAD CERAMIC DIL - DG16



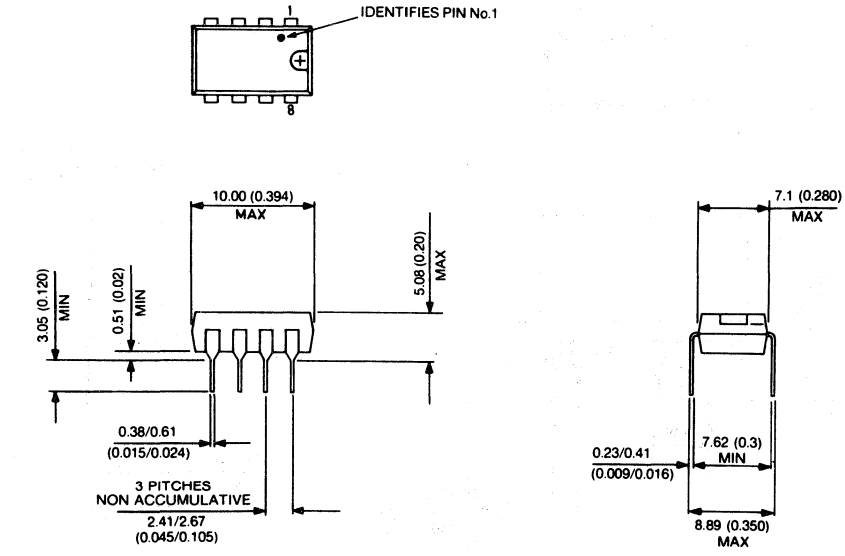
18-LEAD CERAMIC DIL - DG18



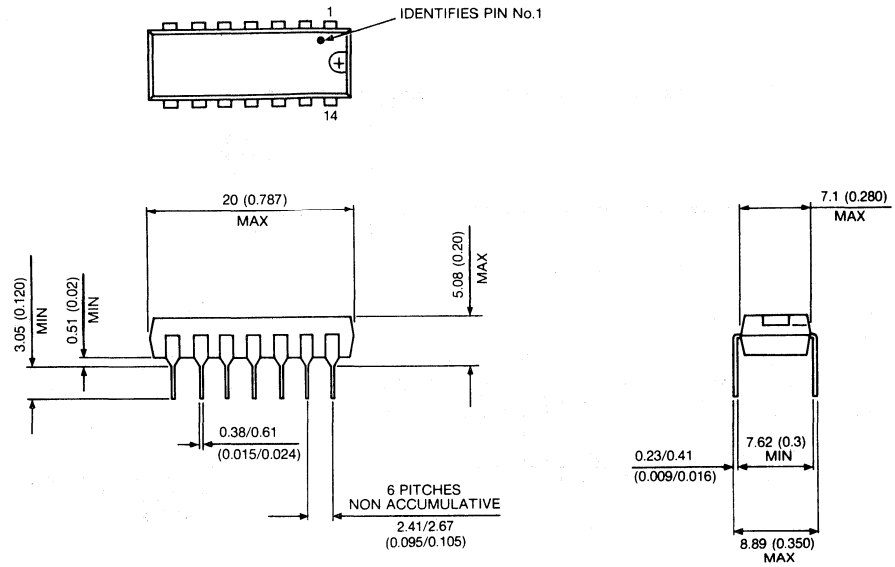
24 LEAD CERAMIC DIL
CERDIP - DG24



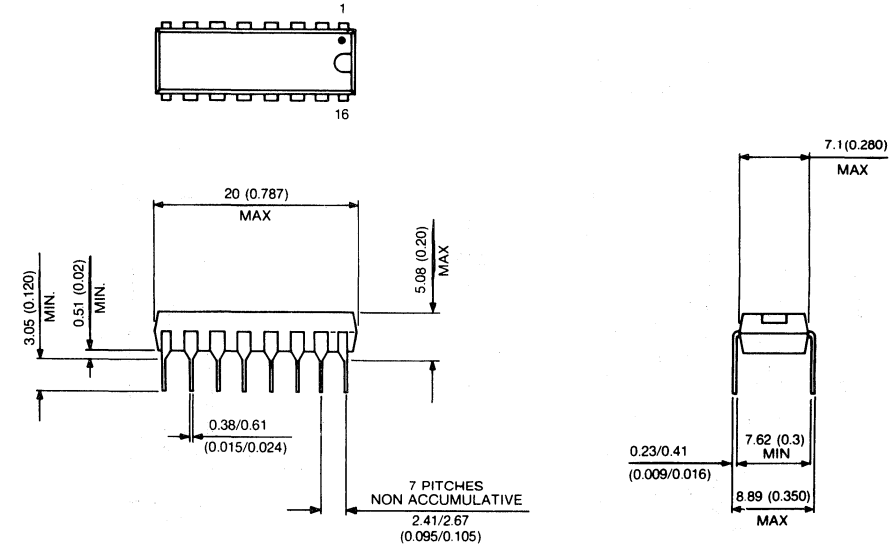
40-LEAD CERAMIC DIL CERDIP - DG40



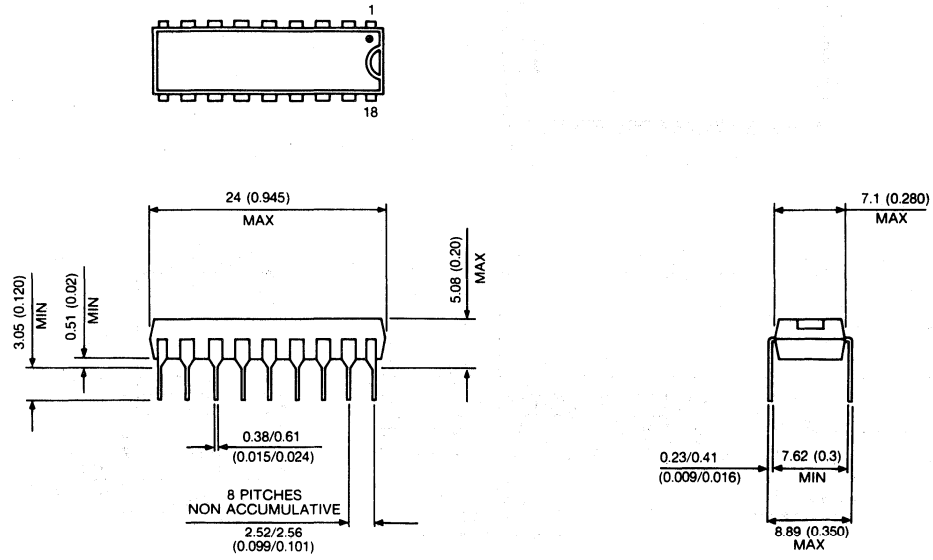
8-LEAD PLASTIC DIL - DP8



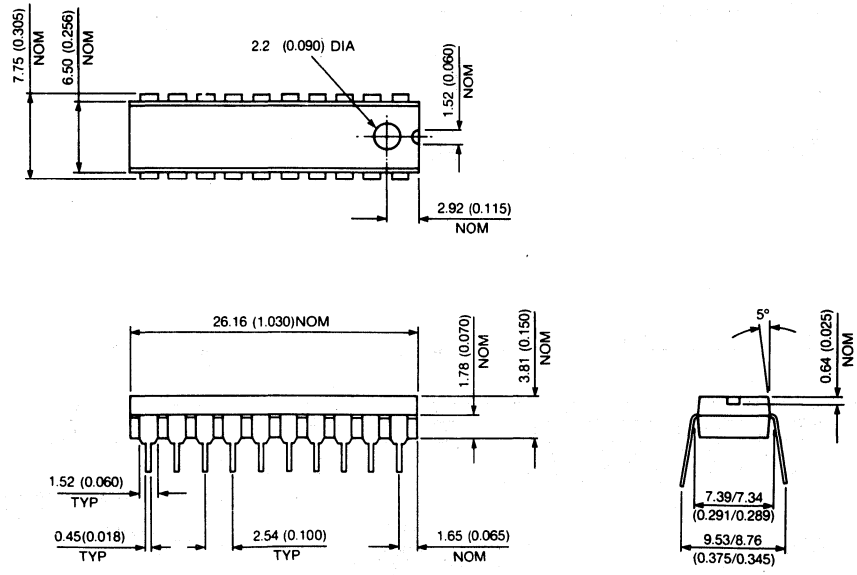
14-LEAD PLASTIC DIL - DP14



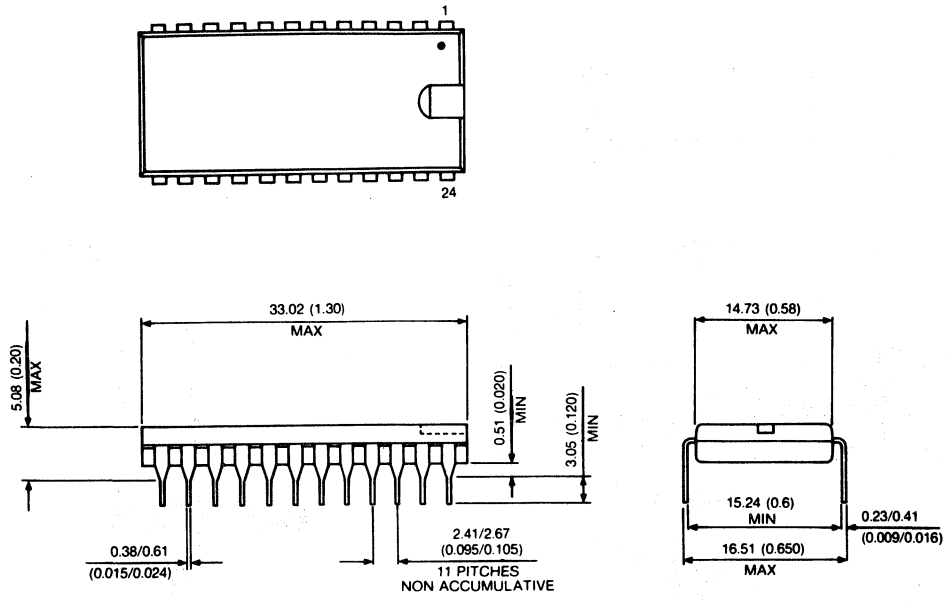
16-LEAD PLASTIC DIL - DP16



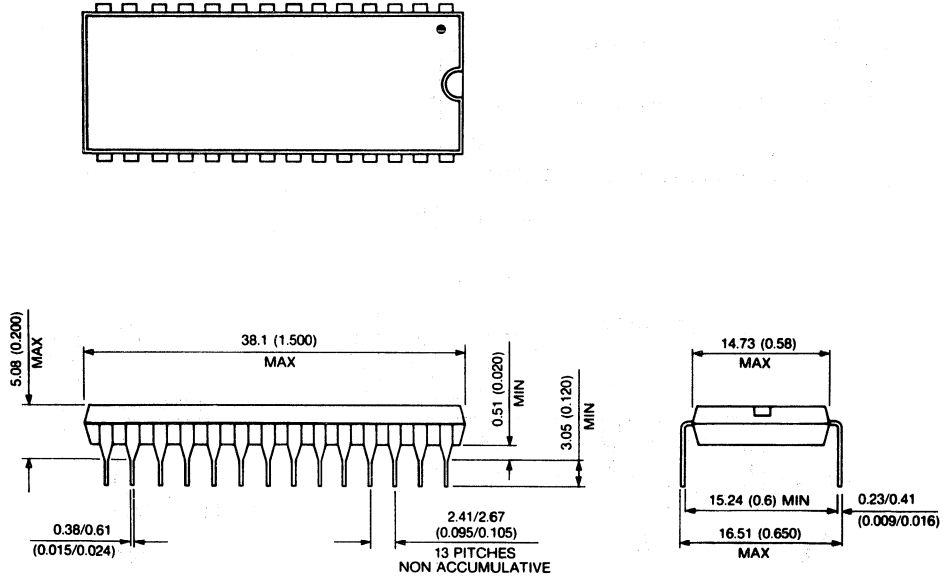
18-LEAD PLASTIC DIL - DP18



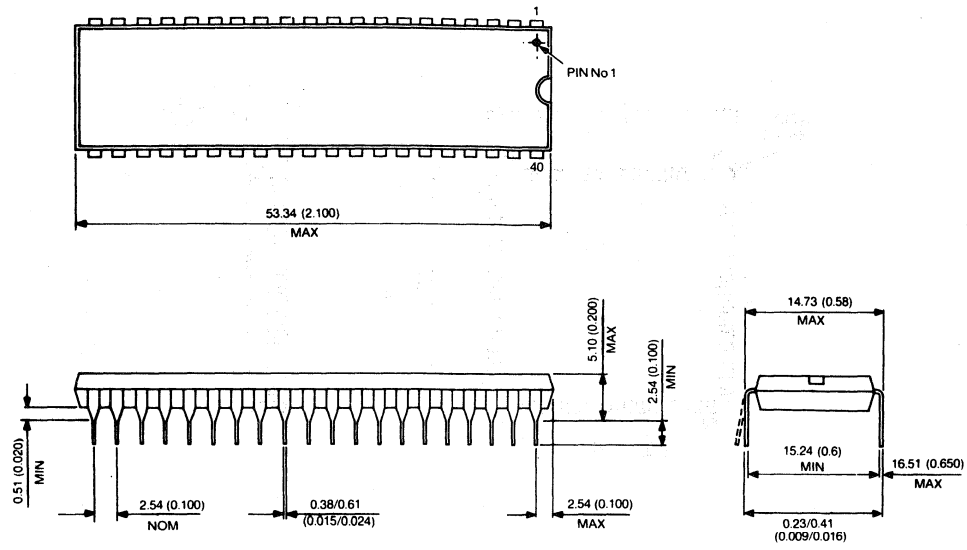
20 LEAD PLASTIC DIL – DP20



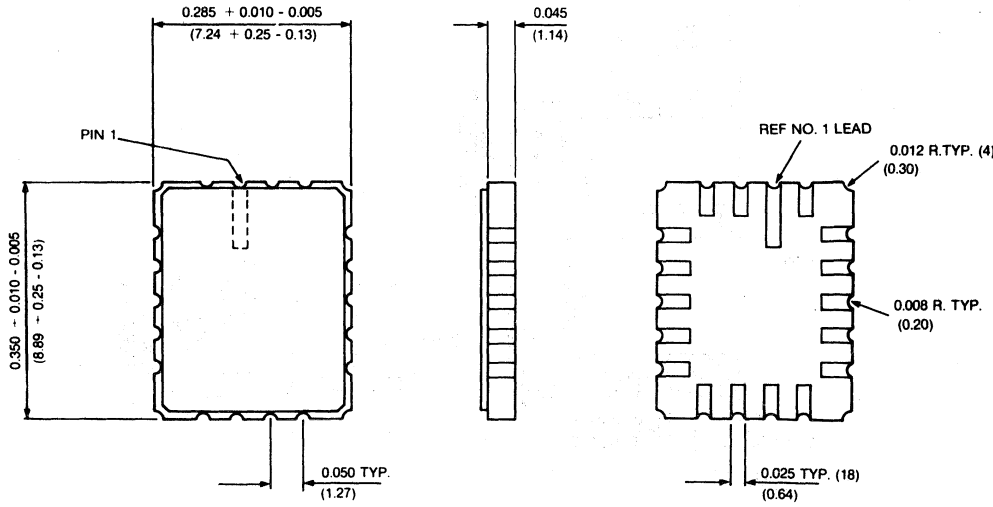
24-LEAD PLASTIC DIL - DP24



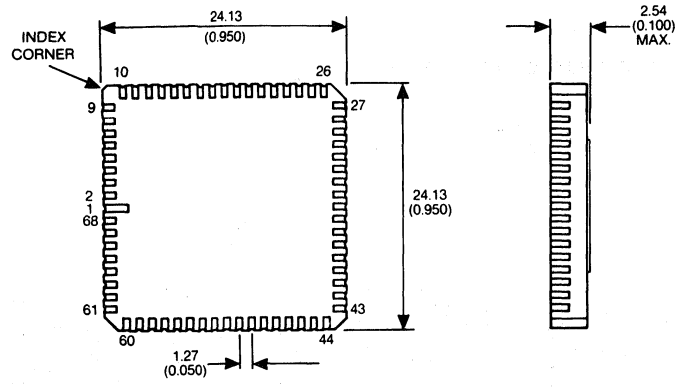
28-LEAD PLASTIC DIL - DP28



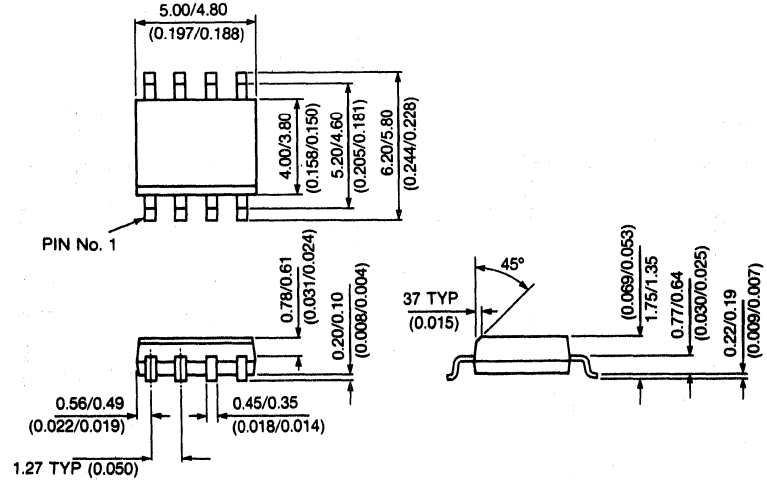
40 LEAD PLASTIC DIL - DP40



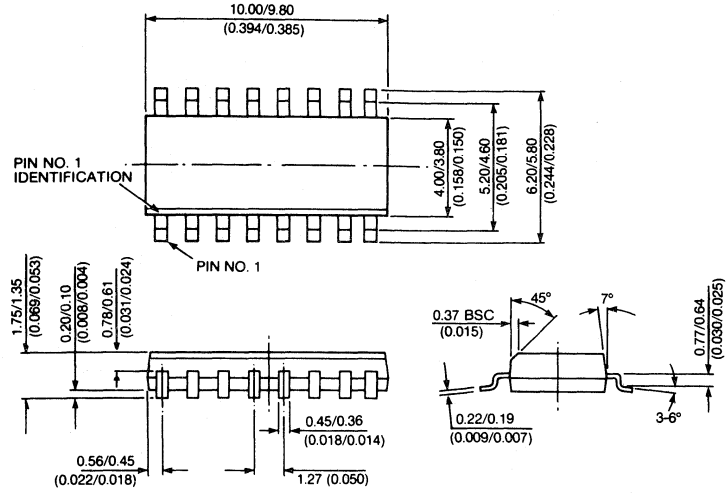
18-PIN LEADLESS CHIP CARRIER - LC18
(HERMETIC)



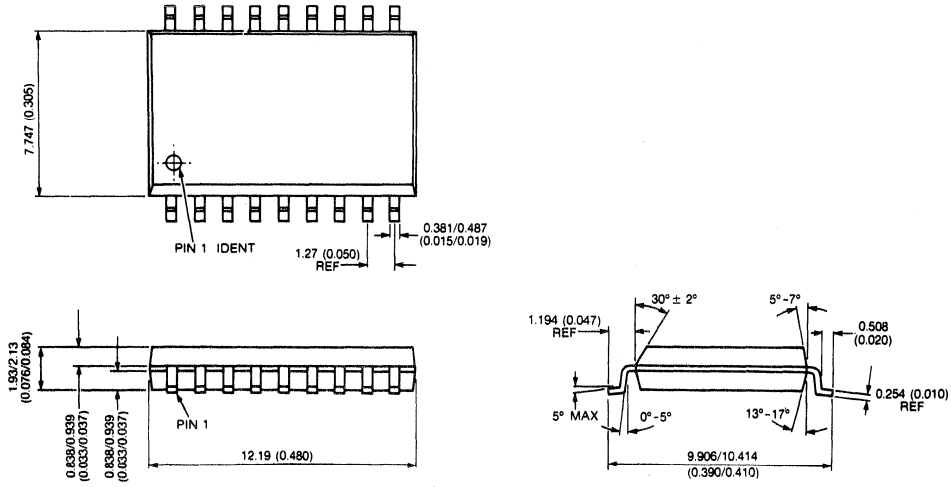
68 CONTACT LCC PACKAGE — LC68



8-LEAD MINIATURE PLASTIC DIL - MP8



16-LEAD MINIATURE PLASTIC DIL - MP16



18-LEAD MINIATURE PLASTIC DIL - MP18

Stop Press

PLESSEY
Semiconductors

MV1826

SINGLE CHIP VIDEO PROGRAMMING SERVICE (VPS) DECODER

The MV1826 is a CMOS decoder for 625 line VPS bi-phase encoded transmissions. The chip also includes an adaptive data slicer. The VPS data is decoded from line 16 of the TV picture and is read via the I²C bus interface.

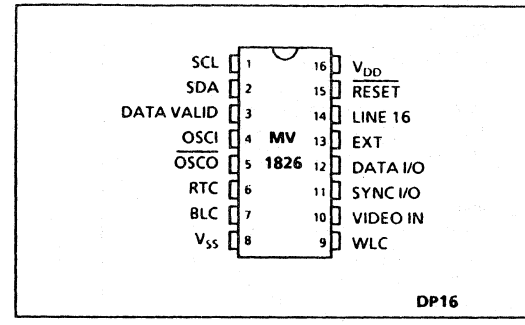


Fig 1 Pin Connections - top view

FEATURES

- Single chip solution
- Very low component count
- Adaptive sync and data slicing levels
- 0.5-3.0 V video input
- I²C bus for low cost microprocessor interface
- Advanced CMOS technology for low power dissipation and high reliability

ABSOLUTE MAXIMUM RATINGS

Supply Voltage VDD	-0.3 to 7V
Input voltage (all pins)	-0.3V to + VDD +0.3V
Storage temperature range	-40°C to +125°C
Operating temperature range	0°C to +70°C
Relative Humidity	85%

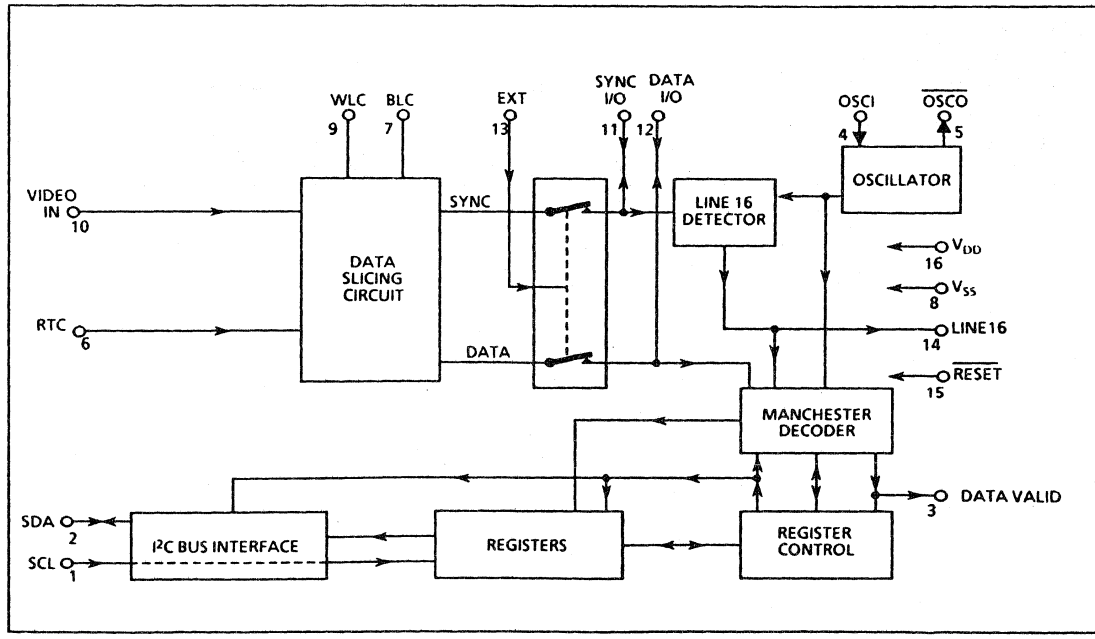


Fig.2 MV1826 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = 4.5 to 5.5V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	16		15		mA	VDD = 5V EXT = 0 V
				500	µA	VDD = 5V EXT = 5 V OSCI = 0
Video Input Pin	10					
Input voltage		0.50	1	3.0	V	(peak to peak)
SDA Pin	2					
SDA Output Low Current		13	26		mA	V_{OL} = 0.4V
Input Low Voltage (VIL)				1	V	
Input High Voltage(VIH)		2			V	
Threshold Voltage (rising)			1.85		V	
Threshold Voltage (falling)			1.05		V	
SCL Pin	1					
Input Low Voltage (VIL)				1.5	V	
Input High Voltage (VIH)		2			V	
Threshold Voltage (rising)			1.85		V	
Threshold Voltage (falling)			1.05		V	
Sync. I/O Pin	11					
Output Low Current		6	13		mA	V_{OL} = 0.4V
Output High Current		-10	22		mA	V_{OH} = 2.4V
Input Low Voltage				1.5	V	
Input High Voltage		3.5			V	
Data I/O Pin	12					
Output Low Current		6	13		mA	V_{OL} = 0.4V
Output High Current		-10	22		mA	V_{OH} = 2.4V
Input Low Voltage				1.5	V	
Input High Voltage		3.5			V	
Line 16 Output Pin	14					
Low Output Current		6	13		mA	V_{OL} = 0.4V
High Output Current		-10	22		mA	V_{OH} = 2.4V
Framing Pulse Output	3					V_{OL} = 0.4V
Low Output Current		6	13		mA	V_{OH} = 2.4V
High Output Current		-10	22		mA	

OPERATIONAL DESCRIPTION

Data encoded on TV line 16 is extracted from the video input using an analog data slicer. Two levels are generated on chip to determine the slicing level. The white level and black level are calculated from the incoming video signal and the two external capacitors connected to pins 7 and 9 and the resistor connected to pin 6. The slicing level is set to the mean voltage between the white and black levels of the incoming video signal.

The VPS decoder can process data from either the internal data slicer or an external data and sync source.

The VPS data, consisting of 15 eight bit words is decoded by the Manchester decoder. Word 1 acts as a "run in" code to synchronise the decoder whilst word 2, the framing code is checked for validity and if an error is found the circuit is reset until the next line 16. A valid framing code causes pin 3 to go high. Words 5,11,12,13 and 14 are stored in five eight bit registers until word 14 is complete, they are then parallel loaded into the serial output register and made available via the I²C bus. The device will be reset, pulling pin 3, low if there is a biphase error in any of these words. The parallel load to the output register is arranged such that the words are written to the I²C bus in the order 11,12,13,14, and 5 with the most significant bit first.

The MV1826 is a slave transmitter on the I²C bus with address 21 (HEX.). When a start condition is recognised, the following 8 clock pulses on the SCL line from the master will clock seven address and one read bit out of the MV1826 onto the SDA line (see Fig 4). If the address is incorrect, the interface is reset until the next start condition. On receipt of a correct address, the SDA pin is pulled low during the ninth clock pulse as an acknowledge to the master receiver. Clock pulses 10 to 17 read word 11 through the SDA pin, and during clock pulse 18. the MV1826 interface monitors this pin for an acknowledge from the master that the data has been received. If the SDA pin is pulled low, (acknowledge) by the master during the 18th clock pulse, the following eight clock pulses will read the next 8 bits on the SDA line (word 12). This process will be repeated until all 40 bits have been read, when further requests for data will result in the data FF (HEX.) being sent until a no-acknowledge followed by a stop condition is received. Data transmission can be halted at the end of any word by the master sending a no-aknowledge followed by a stop condition. New data will only be transferred to the output register of the MV1826 when the I²C interface is reset by a stop condition.

PIN DESCRIPTION

1. **SCL**. This pin is the I²C bus clock input.
2. **SDA**. This is the I²C bus data pin.
3. **DATA VALID.** A high output will be produced when a valid framing code is received. The output will return to a logic low at the end of line 16 or if a biphase error occurs in any valid words.
4. **OSCI.** The input of the crystal oscillator.
5. **OSCO.** The output of the crystal oscillator circuit. A 20MHz crystal is connected to the oscillator input (pin 4).
6. **RTC** Time constant resistor. A 10K resistor is required to V_{DD}
7. **BLC.** Black level capacitor. A 10nF capacitor connected to ground is required.
8. V_{SS} supply ground.
9. **WLC.** White level capacitor. A 10nF capacitor connected to ground is required.
10. **Video Input.** The video input is connected to this pin, coupled via a 10nF capacitor.
11,12. **Sync I/O and Data I/O.** The two outputs from the internal data slicer are fed via two tri-state buffers to the inputs of the line 16 decoder. These two pins can be used to inject an external data and sync pulse train into the line 16 decoder or to use the output of the internal data-slicer, depending on the state of EXT.
13. **EXT.** When this pin is left open or tied low the line 16 decoder uses the data and sync pulse trains from the internal data slicer. When high it permits external data and sync signals to be fed directly into the line 16 decoder.A 150K resistor is internally connected to ground.
14. **Line 16 output.** This pin outputs a high 5µs after the start of the VPS data line (line 16) and goes low at the start of line 17.
15. **Reset.** General chip reset occurs when this pin is taken low. A 150K resistor is internally connected to V_{DD}.
16. V_{DD}. The positive supply is connected here.

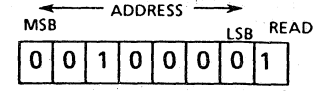


Fig.4 I²C bus address format

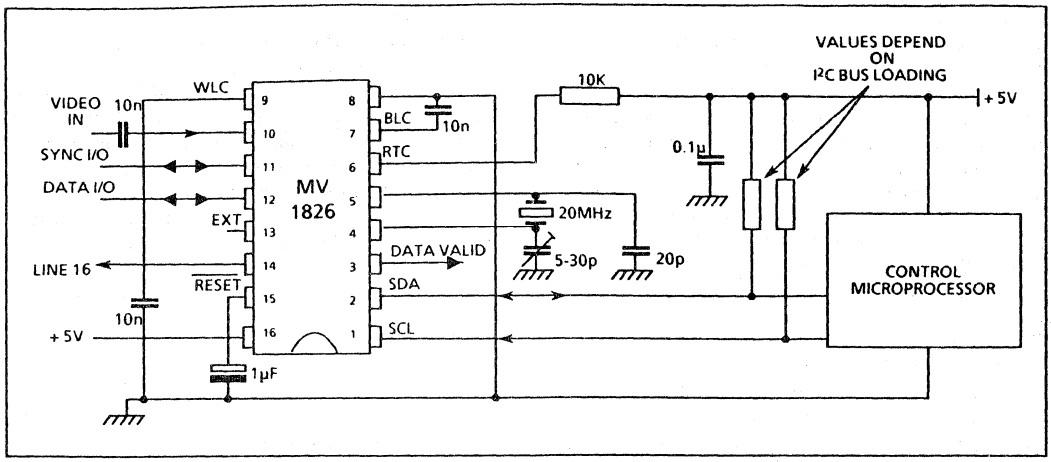
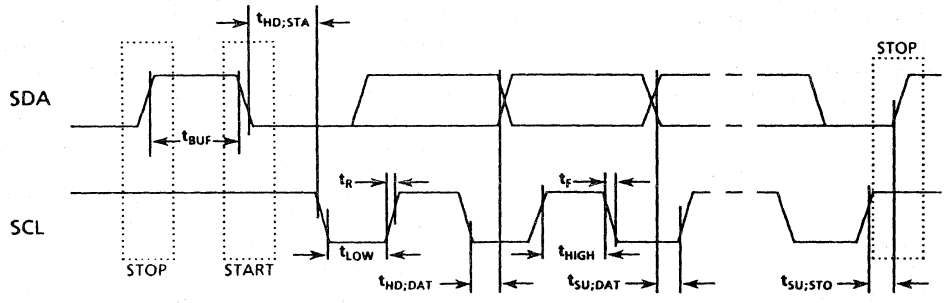


Fig.5 Typical application



All values refer to VIH and VIL levels

Parameter	Symbol	Min	Max	Units
SCL Clock frequency	f_{SCL}	0	100	kHz
Time the bus must be free before a new transission can start	t_{BUF}	4.7		µs
Hold time start condition.After this period the first clock pulse is generated	$t_{HD;STA}$	4.0		µs
LOW period of clock	t_{LOW}	4.7		µs
High period of clock	t_{HIGH}	4.0		µs
Set up time DATA	$t_{SU;DAT}$	250		ns
Rise time of SDA and SCL signals	t_R		1	µs
Fall time of both SDA and SCL signals	t_F		300	ns
Set up time before SCL clock at STOP condition	$t_{SU;STO}$	4.7		µs

Fig.6 I²C bus timing diagram

PLESSEY
Semiconductors

SL1488

VIDEO BUFFER AMPLIFIER WITH AGC AND BLACK LEVEL CLAMP

The SL1488 is a high input impedance video amplifier featuring 6dB of AGC range and dc restoration of the output signal. Two points on the video waveform, (generally the frame sync tips and the black level) can be accurately clamped to adjustable dc levels applied to two device pins, hence controlling the amplitude and dc level of the output video. External gating inputs control the timing of the clamping action. The clamped and amplitude controlled output is available on two isolated pins whilst a third output of similar amplitude but clamped to an internal 4V reference is also provided. A blanking input can be used to switch off the video from this output, the output voltage being held at the 4V clamping level when the video is off.

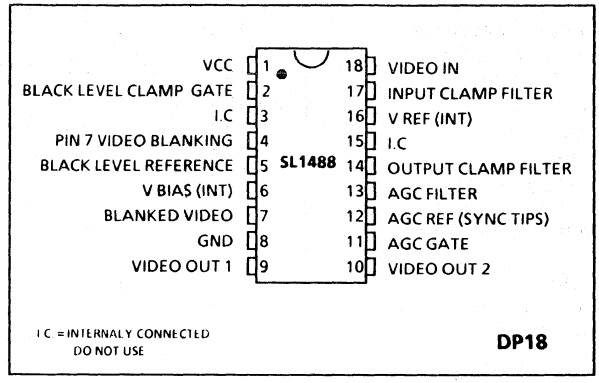


Fig 1 Pin Connections - top view

FEATURES

- 6dB AGC range (minimum)
- D.C. level restoration
- 3 video outputs
- Blanked video output available
- High impedance AC coupled input
- Wide video bandwidth 8MHz at 1dB down
- 30pf drive capability
- Excellent linearity

ABSOLUTE MAXIMUM RATINGS

Supply voltage VCC	15V
Storage temperature	-55°C to + 125°C
Operating temperature	0°C to + 70°C

APPLICATIONS

- Professional video systems
- RGB level control
- Video ADC driver

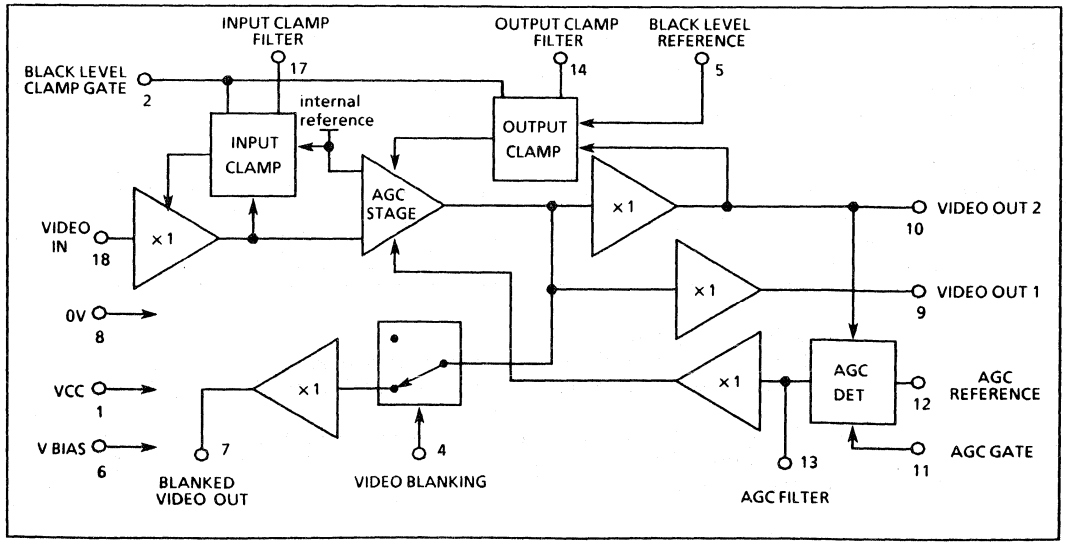


Fig 2 SL1488 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C, V_{CC} = 10.8Vto 13.2V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current I_{CC}	1		56	75	mA	
Video amplifier						
Output impedance	9,10		8		Ω	
Input impedance	18	50	88		Kohm	measured at DC
AGC range	18,9,10	6	8.9		dB	
Gain	18,8,10		1.1	1.4	dB	V18 = 710mVp-p V12 = 2.75V
Gain	18,9,10	2.8	3.2		dB	V18 = 350mVp-p V12 = 2.25V
Bandwidth	18,9,10		8		MHz	0.5dB point
Integral linearity	18,9,10		1		%	1V p-p video
Differential gain	18,9,10		1		%	1V p-p video
Differential phase	18,9,10		0.5		Degree	1V p-p video
Reference Inputs						
Black level reference input range	5	2.5		4.5	V	
AGC reference input range	12	1.6		4	V	
Reference input current	5,12			10	µA	
Blanked Video						
Output gain with reference to pin 10	7	1.1	1.2	1.3		V7/V10
Output bandwidth	7		8		MHz	0.5dB point
Clamp level	7		4		V	Internally generated ref.
Black level clamp						
Gate input high	2	2.5		5.5	V	
Gate input low	2			0.5	V	
High level sink current	2			100	µA	V2 = 2.5V
Low level source current	2			10	µA	V2 = 0.5V
AGC gate input						
High level	11	2.5		5.5	V	
Low level	11			0.5	V	
High level sink current	11			100	µA	V11 = 2.5V
Low level source current	11			10	µA	V11 = 0.5V
Blanking Input						
High level	4	4.0		5.5	V	Blank video to grey
Low level	4			1.5	V	Pass video
High level sink current	4			20	µA	V4 = 4.0V
Low level source current	4			5	µA	V4 = 1.5V

NOTES (Refer to fig 4 opposite)

1. The output clamp will attempt to adjust the video level at pin 10 during the black level gate period to the level set at the black level reference (pin 5).

2. The AGC will attempt to adjust the amplitude of the output at pin 10 such that the video level during the AGC gate period is equal to that set on the AGC reference (pin 12).

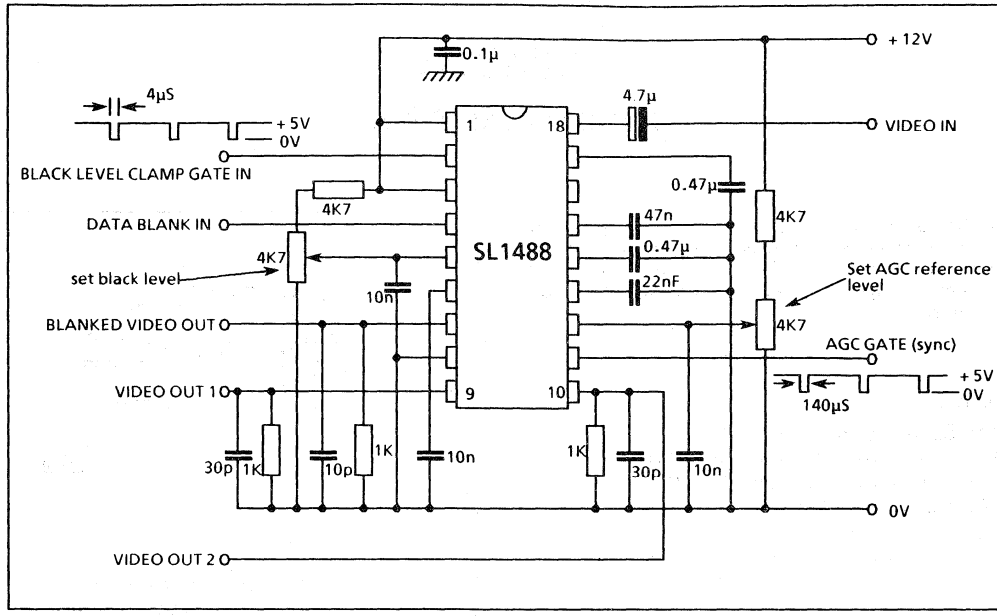


Fig 3 Typical application for PAL video

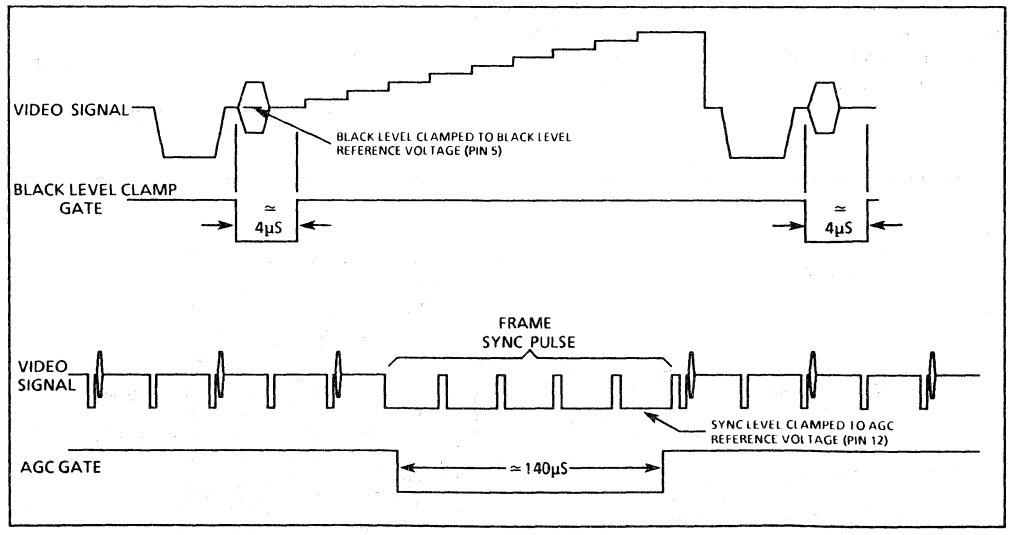


Fig 4 Typical black level clamp and AGC gate waveforms (see note page 2)

PLESSEY
Semiconductors

SP4908

2.5GHz ÷ 8 PRESCALER

The SP4908 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

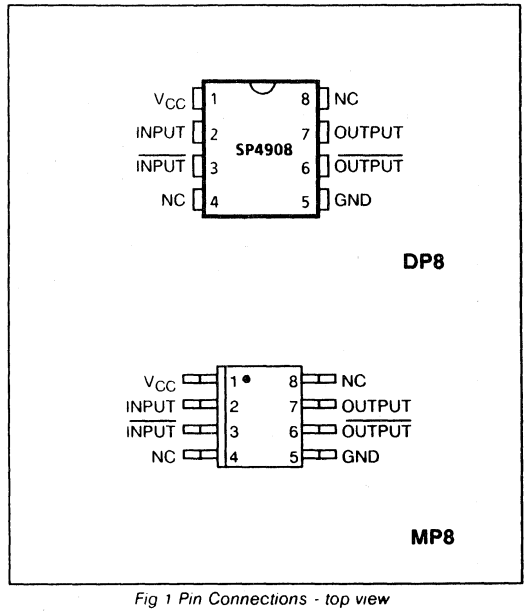


Fig 1 Pin Connections - top view

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

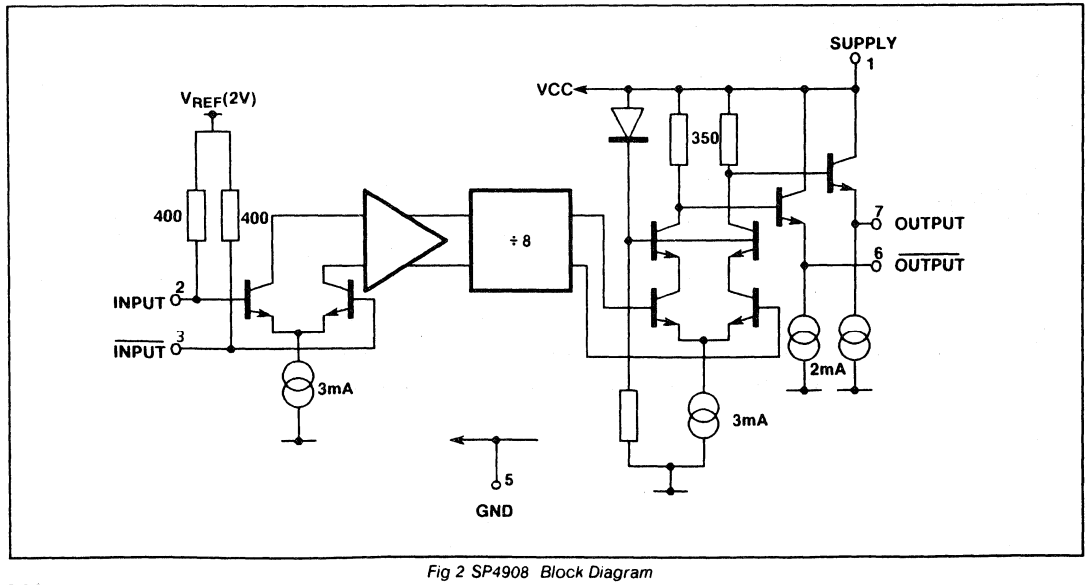


Fig 2 SP4908 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		44		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 2500MHz	6,7		0.7		Vp-p	V_{CC} = 5V Load as fig.4

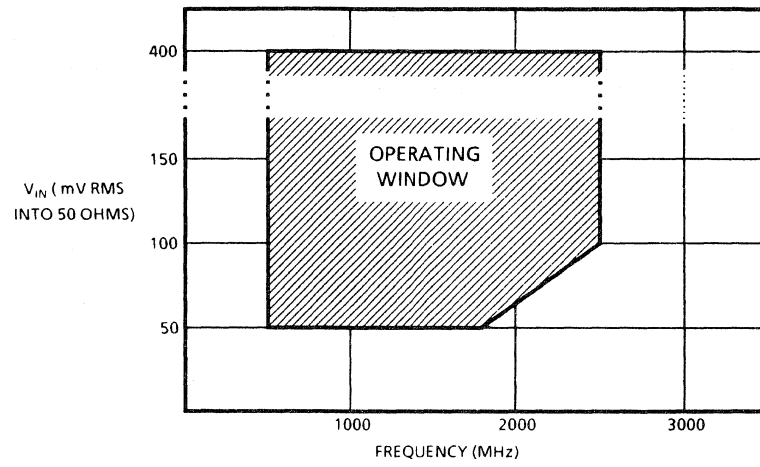


Fig.3 Typical input sensitivity

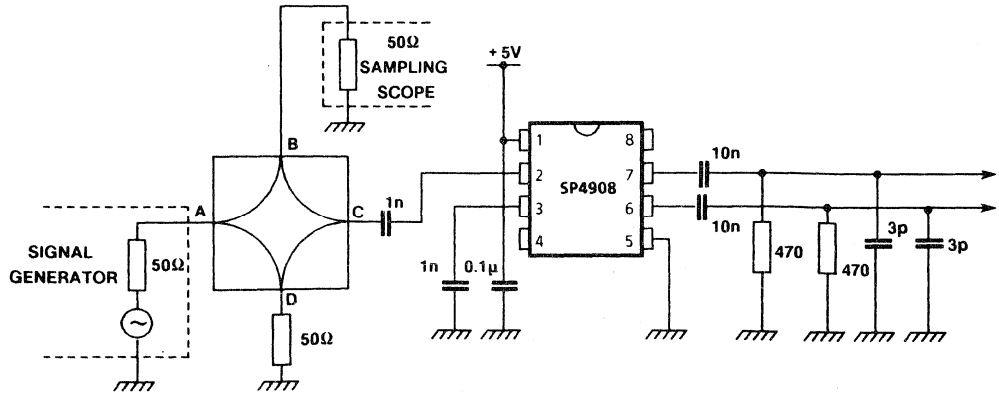


Fig.4 Test circuit

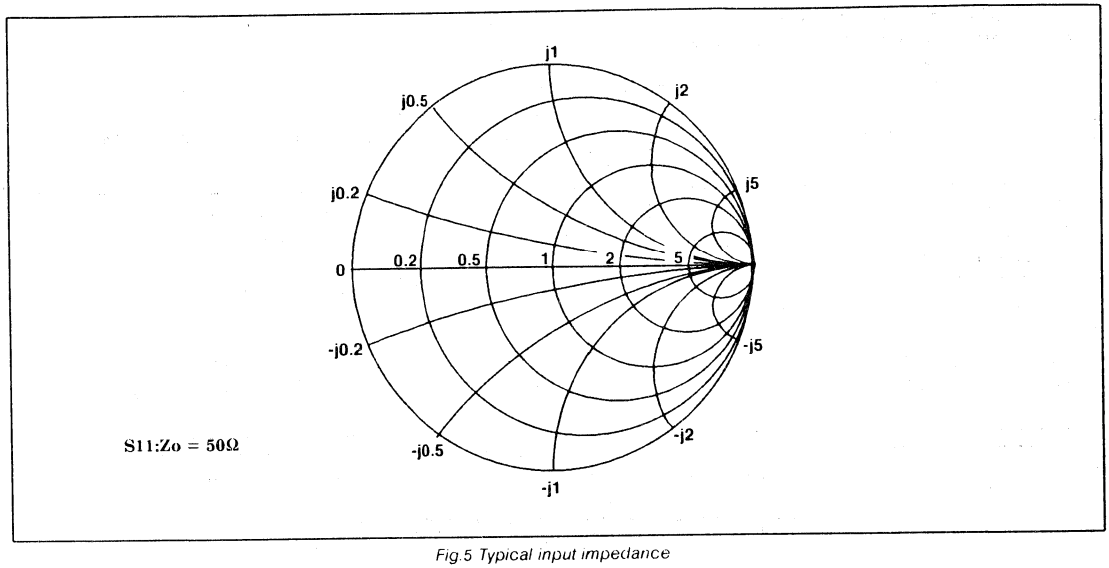


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP4982

2.5GHz ÷8192 PRESCALER

The SP4982 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a cmos compataible output stage.

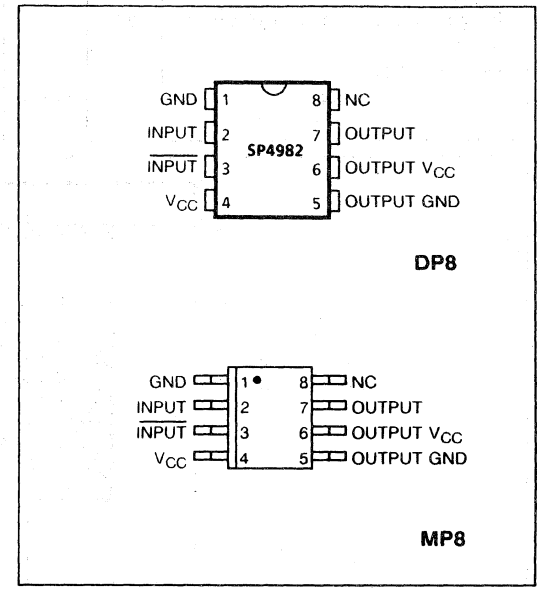


Fig 1 Pin Connections - top view

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

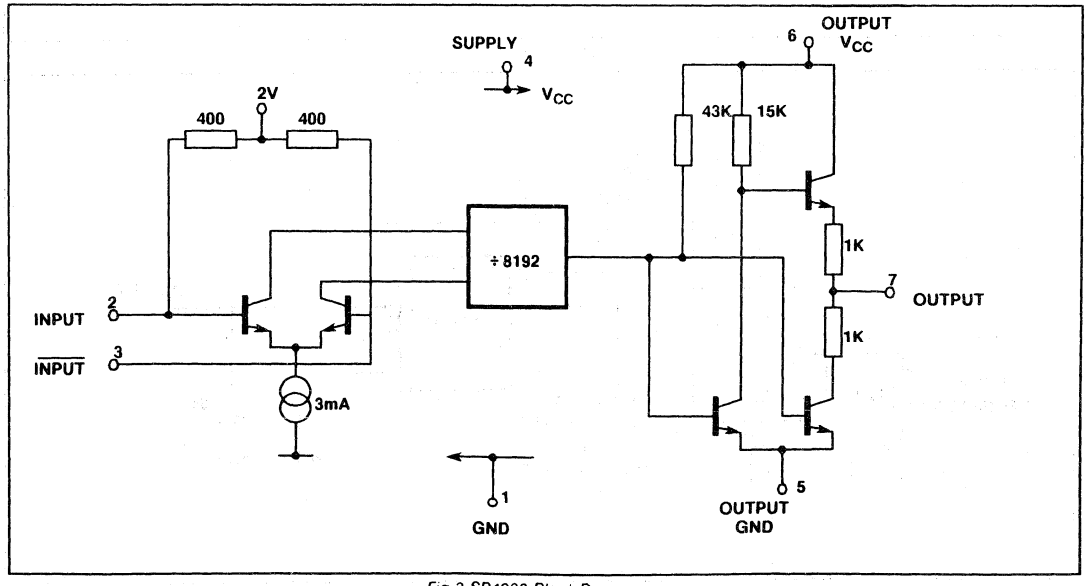


Fig 2 SP4982 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -40°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		44		mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50 ohm system.
2500MHz				100	mV	see figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage						
High		V_{CC}-0.5			V	V_{CC} = 5V Load as fig.4
Low				0.5	V	Frequency = 2.5GHz

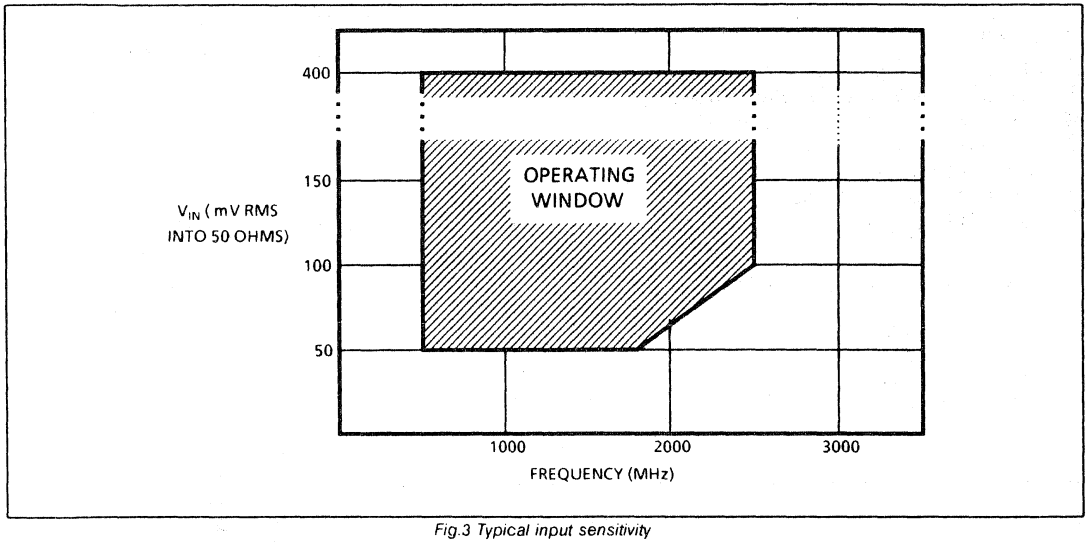


Fig.3 Typical input sensitivity

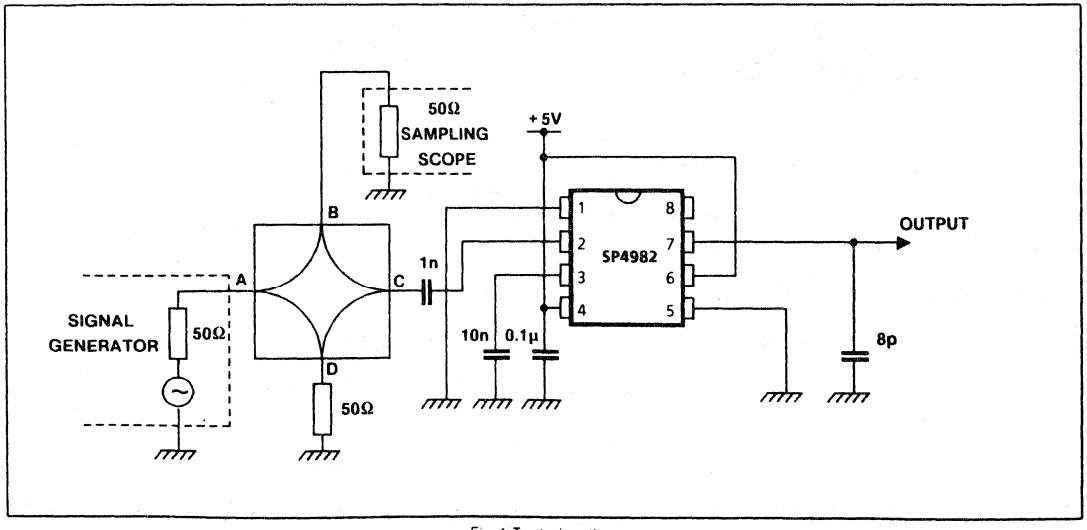


Fig.4 Test circuit

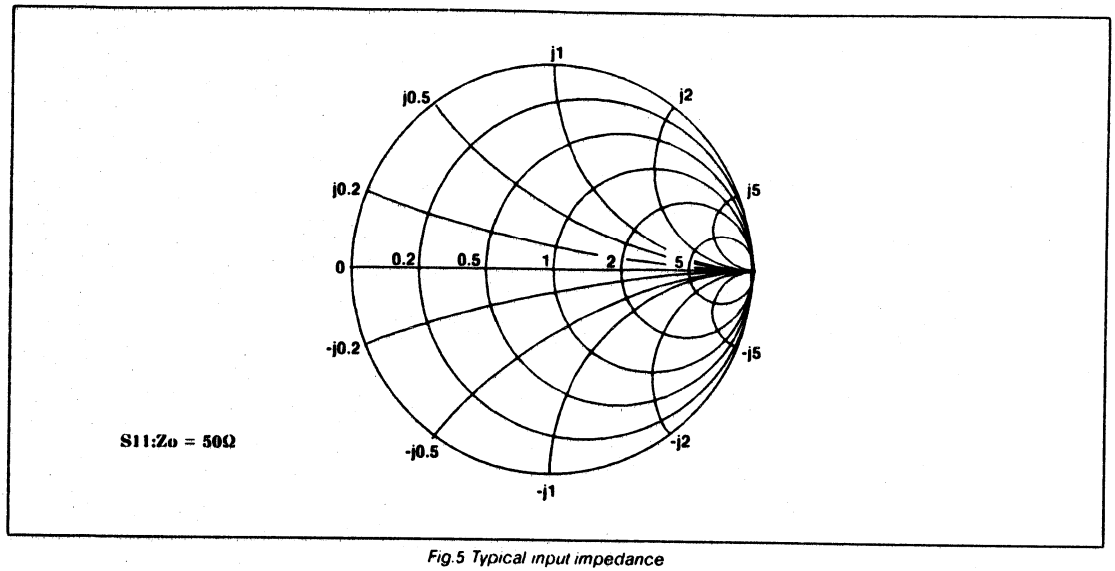


Fig.5 Typical input impedance

Plessey Semiconductors Locations

Main offices

HEADQUARTERS **Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext. 2198.

NORTH AMERICA **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

International marketing centres

BENELUX **Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.

FRANCE **Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.

ITALY **Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.

UNITED KINGDOM (SOUTH) **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666 Ext.250.

UNITED KINGDOM (NORTH) **Plessey Semiconductors Ltd.,** Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.

WEST GERMANY, AUSTRIA and SWITZERLAND **Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.

SOUTH EAST ASIA **Plessey Company plc.,** Room 2204-7 Harbour Centre, 25 Harbour Road, Wanchai, Hong Kong. Tel: 58332111 Tx: 74754 Fax: 58339090.

World-wide agents

AUSTRALIA and NEW ZEALAND **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.

EASTERN EUROPE **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. U.K. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666.

GREECE **Mammeas,** Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR.

INDIA **Semiconductors Ltd.,** 71 Mittal Chambers, Nariman Point, Bombay 400 021. Tel: 2874518 Tx: 11 2781 ADOR IN.

Semiconductors Ltd., Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739.

Semiconductors Ltd., 513, Ashoka Estate, 24, Barakhamba Road, New Delhi — 110001. Tel: 44879 Tx: 31 3369.

Khandelwal Herrmann Electronics Limited, B-207, Neelam Centre, Worli, Bombay-400 025. Tel: 4947476.

JAPAN **Cornes & Company Ltd.,** Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874 Fax: 271-1479.

Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496 Fax: 541-8850.

Microtek Inc., Itoh Bldg., 7-9-17 Nishishinjuku, Shinjuku-ku, Tokyo 160. Tel: 03-371-1811 Tx: J27466 Fax: 03-369-5623.

HONG KONG **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444241-6 Tx: 36590 Fax: 499-3065.

KOREA **Young O Ind Co. Ltd.,** Yeoevido, P.O.Box 149, Seoul. Tel: 782 1707 Tx: K25701. Fax: 784 6786.

KML Corporation, 3rd Floor, Banpo Hall Building, 604-1 Banpo Dong, Kangnam-Ku, P.O.Box 19, Seoul. Tel: (02) 533-9281/2 Tx: KMLCORP K25981 Fax: (02) 533 1986.

MALAYSIA **Plessey Malaysia,** 1602 Pernas International Bldg, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: (03) 2611477 Tlx: 30918 PLESCOMA Direct Fax: (03) 2613385.

SCANDINAVIA

Denmark **Scansupply,** Nannasgade 18, DK-2200 Copenhagen N. Tel: 45 1 83 50 90 Tx: 19037 Fax: 45 1 83 25 40.

Finland **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 90 55 00 02 Tx: 122214 Fax: 055 1117.

Norway **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx. 71963 Fax: 02 643443.

Sweden **Swedesupply AB,** PO Box 1028, 171 21 Solna. Tel: 08/735 81 30 Tx: 13435 Fax: 08/839033.

SINGAPORE **Plessey S.E. Asia Pte Ltd.,** 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013 Direct Fax: 7329036.

SOUTH AFRICA **Plessey South Africa Ltd.,** 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793, Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SPAIN **JR Trading,** Apartado de Correos 8432, Madrid 8 Tel: 248 12 18/248 38 82 Tx: 42701. Fax: 241 4460.

TAIWAN **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.

TURKEY **The Plessey Company plc.,** Koroglu Caddesi 5/4, Gaziosmanpasa, Ankara. Tel: 010 90 41 367352 Fax: 46526.

World-wide distributors

AUSTRALIA
Plessey Semiconductors Australia Pty Ltd., P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney (02) 720133 Tx: AA20384 Direct Fax: (02) 7260669.

AUSTRIA
DAHMS Elektronik Ges. mbH, Wiener Str. 287, A-8051 Graz. Tel: 0316/64030 Tx: 31099. Fax: 0316/6403029.
Othmar Lackner, Landstrasser Hauptstr. 37, A-1030 Wien. Tel: 0222 75 26 18-0 Tx: 111198. Fax: 0222/7526185.

BELGIUM
Master Chips, 4 St. Lazarus Laan, 1030 Brussels. Tel: 02 219 58 62 Tx: 62500. Fax: 02 217 92 01.

FRANCE
Mateleco:
Ile de France, 66, Avenue Augustin Dumont, 92240 Malakoff. Tel: (1) 46 57 70 55 Tx: 203436F.
Rhone-Alpes, 2 Rue Emile Zola, 38130 Echirolles. Tel: 76 40 38 33 Tx: 980837F.
ICC:
Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539F. Fax: 61 48 11 25.
Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41 Tx: 990928F.
Marseille, Z.A. Artizanord II, 13015 Marseille. Tel: 91 03 12 12 Tx: 441313F.
Toulouse, 78 Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10 Tx: 520897F.
CGE Composants S.A.:
Ile de France, 32 Rue Grange Dame Rose, 92360 Meudon la Foret. Tel: (1) 46 30 24 45 Tx: 632253F Fax: 46 30 0081.
Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40 Tx: 571224F.
Bretagne, 9 Rue du General Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311F.
Centre/Pays-de-Loire, Allee de la Detente, 86360 Chaseneuil du Poitou. Tel: 49 52 88 88 Tx: 791525F.
Est, 27 Rue Kleber, 68000 Colmar. Tel: 89 41 15 43 Tx: 870569F.
Midi-Pyrenees, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38 Tx: 530957F.
Nord, 2 Rue de la Creativite, 59650 Villeneuve d'Ascq. Tel: 20 67 04 04 Tx: 136887F.
Provence/Cote d'Azur, Avenue Donadei, bat.B, 06700 St. Laurent du Var. Tel: 93 07 77 67 Tx: 461481F.
Rhone-Alpes, 101 Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29 Tx: 305301F.
ATAC-Diffusion SA, 2 Rue-Lecointre, 7 Ave de l'Europe, 92310 Sevres. Tel: 14 507 11 11 Tx: 203047 Fax: (1) 45341042.

ITALY
Eurelettronica SpA, Via E Fermi 8, 20090 Assago (Milan). Tel: 02-4880022 Tx: 350037. Fax: 488 0275.
Eurelettronica, Via Bertoloni 27, Rome. Tel: 875394 Tx: 610358.
Alta S.R.L., Via Matteo Di Giovanni 6, 50143 Florence. Tel: 055717402 Tx: 571246. Fax: 055/705658.
Adelsi Spa, Via Novara 570, 20153 Milan. Tel: 02 3580641 Tx: 332423 Adelsy I **Fax: 02/3011988.**
ESCO Italiana Spa., Via Modena 1, 20099 Sest S Giovanni. Tel: 02 24 09 241-251 Tx: 322383. Fax: 02/2409255.
Fanton S.R.L., Bologna, Milano, Firenze, Roma, Padora, Torino. Tel: (02) 3287312 Fax: 051/732216.

NETHERLANDS
Heynen B.V., Postbus 10, 6590 AA Gennep. Tel: 8851-96111 Tx: 37282 Fax: 08851 96220.
Tekelek Airtronic BV., Postbus 63-2700 AB, Zoetermeer. Tel: 079 31010 Tx: 33332. Fax: 079 417504.

SOUTH AFRICA
Plessey South Africa Ltd., 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793 Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SWITZERLAND
Aumann & Co. AG, Forrlibuckstrasse 150, CH-8037 Zurich. Tel: 01/443300 Tx: 822966. Fax: 01/44 5023.
Elbatex AG., Hardstr. 72, 5430 Wettingen. Tel: 056 27 51 11 Tx: 58068 Fax: 056/271924.

TAIWAN
Artistex International Inc., B2, 11th Floor, 126, Nanking East Road, Section 4, Taipai, Taiwan, Republic of China. Tel: (02) 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446.

UNITED KINGDOM
Celdis Ltd.,37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171 Tx: 848370 Fax: 0734 509933.
Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311 Tx: 55147 Fax: 0532 633404.
Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878/787848 Tx: 847571 Fax: 0734 776095.
Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
RR Electronics Ltd., St. Martins Way, Cambridge Road, Bedford MK42 0LF. Tel: 0234 47188/270777 Tx: 826251 Fax: 0234 210674.
Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958 Fax: 0895 422044.

	STC Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF.Tel: 0279 626777 Tx: 818801. Fax: 0279 441687.
	Unitel Ltd., Unitel House, Fishers Green Road, Stevenage, Herts. Tel: 0438 312393 Tx: 825637. Fax: 0438 318711.
UK EXPORT (to countries other than those listed)	**Extram (U.K.) Ltd.,** 1A Albert St., Slough, Berks. SL1 2BH. Tel: 0753 824311 Tx: 848441 EXTRAM G Fax: 0753 820250.
WEST GERMANY	**Altron GmbH & Co. KG,** Gaussstr. 10, 3160 Lehrte. Tel: 051 32 5 30 24 Tx: 922383 Fax: 05132/57776.
	API Elektronik Vertriebs GmbH, Augustinerring 27, D-8062 Markt Indersdorf. Tel: 08136/7092 Tx: 5270505 Fax: 08136/7398.
	AS Electronic Vertriebs-GmbH, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
	Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Fax: 089 300 6001.
	Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708. Fax: 07159/5119.
	Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47 Tx: 822538 Fax: 0231/577514.

North American representatives

NATIONAL SALES	Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.
EASTERN REGION	1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344.
NEW ENGLAND REGION	132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 617-543-2994.
WESTERN REGION	4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Tlx: 62217370 Fax: 408-970-0263.
SOUTHEAST REGION	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Tlx: 510-600-3635 Fax: 214-680-9753.
NORTH CENTRAL REGION	1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633.
FLORIDA & DIXIE REGION	541 S.Orlando Ave., Suite 310, Maitland, FL 32751. Tel: (305) 539-0080 Fax: 304-539-0055.
SOUTHWEST REGION	9 Parker, Irvine, CA 92718. Tel: (714) 472-2530 Tlx: 989096 Fax: 714-458-7084.
DISTRIBUTION SALES	9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Tlx: (910) 595-1930 Fax: (714) 770-0627.
CANADA	207 Place Frontenac, Quebec, H9R-4Z7. Tel: (514) 697-0095/96 Fax: 514-697-0681.

North American sales offices

ALABAMA	**DHR Marketing, Inc.,** 904 Bob Wallace Avenue, Suite 222, Huntsville, AL 35801. Tel: (205) 533-5165 Fax: (205) 533-1312.
ARIZONA	**Reptronix/Chaparral,** 4625 South Lakeshore Dr., Tempe, AZ 85282-7127. Tel: (602) 345-4580 Fax: (602) 839-3841.
CALIFORNIA	**Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Fax: 619-450-3681.
	Pinnacle Sales Corp., 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Fax: 408-249-5129.
	Select Electronics, 2109 Brookfield Drive, Thousand Oaks, CA91362.
	Straube Associates, 2551 Casey Avenue, Mountain View, CA 94043. Tel: (415) 969-6060 Fax: (415) 964-6526.
	Select Electronics, 14730 Beach Blvd-Bldg F, Suite 106, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.
COLORADO	**MRC,** 2579 W. Main St. Littleton, CO 80120. Tel: (303) 794-4684 Fax: (303) 794-4644.
CONNECTICUT	**NRG Ltd.,** 63 Duka Avenue, Fairfield, CT 06430. Tel: (203) 384-1112 Fax: (203) 335-2127.
FLORIDA	**Lawrence Associates,** 1131 South U.S.19 Palm Barbor, FL 34684. Tel: (813) 787-2773 Fax: (813) 787-2654.
	Lawrence Associates, 380 Lowndes Square, Casselberry, FL 32707. Tel: (305) 339-3855 Fax: (305) 767-0973.
	Lawrence Associates, 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Fax: 305-394-5442.
GEORGIA	**DHR Marketing, Inc.,** 3100 Breckenridge Blvd. Suite 145, Duluth, GA 30136. Tel: (404) 564-0529 Fax: (404) 564-1127.
IDAHO	**Crown Electronic Sales, Inc.,** 601 W. Hays, Suite 20, Boise, Idaho 83702. Tel: (208) 344-9588 Fax: (208) 344-9550.

INDIANA **Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Fax: 219-484-7491.
Corrao Marsh, Inc., 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446. Fax: (317) 462-6568.

ILLINOIS **Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756 Fax: 312-956-0189.

IOWA **Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666 Fax: 319-377-2273.

KANSAS **Lorenz Sales, Inc.,** 8115 West 63rd Si., Suite 1, Merriam, KS66202. Tel: (913) 384-6556.

MARYLAND **Walker-Houck,** 10706 Reisters Town Rd., Suite D, Owings Mills, MA 21117. Tel: (301) 356-9500 Fax: 301-356-9503.

MASSACHUSETTS **Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537.

MICHIGAN **R.P. Urban & Associates,** 2335 Burton Street SE, P.O. Box 7386, Grand Rapids, MI49510. Tel: (616) 245-0511 Fax: (616) 245-4083.
R.P. Urban & Associates, 24634 Five Mile Road, Detroit, MI48239. Tel: (313) 535-2355 Fax: (313) 7109.

MINNESOTA **Electro Mark Inc.,** Valley Oaks Business Cntr. 7167 Shady Oak Rd., Eden Prairie, MN 55344. Tel: (612) 944-5850 Fax: (612) 944-5855.

MISSOURI **Lorenz Sales, Inc.,** Del Crest Plaza Bldg. Suite 208, 8420 Delmar Blvd., University City, MO 63124. Tel: (314) 997-4558 Fax: 319-337-2273.

NEBRASKA **Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660.

NEW JERSEY **Metz Benham Associates, Inc., (MBA),** Terrace Level, Suite II, 1982 Greentree Road, Cherry Hill, NJ 08003. Tel: (609) 424-0404 Fax: (609) 751-2160.
Metro Logic, 280 Midland Ave., Bldg N-1, Saddle Brook, NJ 07662. Tel: (201) 797-8844 Fax: 201-797-8418.

NEW MEXICO **Reptronix/Chaparral,** 237 C Eubank Blvd., N.E., Albuquerque, NM 87123. Tel: (505) 292-1718 Fax: (505) 299-1611.

NEW YORK **Micro-Tech,** 1350 Buffalo Road, Rochester, NY 14624. Tel: (716) 328-3000 Fax: (716) 328-3003.
Micro-Tech, 401 South Main Street, North Syracuse, NY 13212. Tel: (315) 458-5254 Fax: (315) 458-5919.
Micro-Tech, 10 Guyton Street, Kingston, NY 12401. Tel: (914) 338-7588.

NORTH CAROLINA **DHR Marketing, Inc.,** 4016 Barrett Drive, Suite 201 (27609) P.O. Box 19703, Raleigh, NC 27609. Tel: (919) 781-1961

SOUTH CAROLINA **DHR Marketing, Inc.,** 37 Villa Road, Suite 409, Greenville, SC 29615. Tel: (803) 271-8712 Fax: (803) 271-8712.

OHIO **Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45439. Tel: (513) 294-0539 Fax: (513) 294-4769.
Scott Electronics, Inc., 360 Alpha Park, Cleveland, OH 44143. Tel: (216) 473-5050 Fax: (216) 473 5055.
Scott Electronics, Inc., 6515 East Livingston Avenue, Reynoldsburg, OH 43068 Tel: (614) 1281 Fax: (614) 863-1485.
Scott Electronics, Inc., 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513 Fax: (513) 791-8059.

OREGON **Core II, P.O. Box 5459, Beaverton, OR 96006-0459.** Shipping Address only: 21785 S.W. T.V. Hwy, Unit Q, Beaverton, OR 97006. Tel: (503) 641-0877 Fax: (503) 591-8383.
Crown Electronic Sales, Inc., 17020 S.W. Upper Boones Ferry Rd., Suite 202, Portland, OR 97223. Tel: (503) 620-8320 Fax: 503-639-4023.

TENNESSEE **DHR Marketing, Inc.,** 417 Welchwood, Suite 102, Nashville, TN 37211.Tel: (615) 331-2745.

TEXAS **Oeler & Menelaides, Inc.,** 8340 Meadow Rd., Suite 24, Dallas, TX 75231. Tel: (214) 361-8876 Fax: (214) 692-0235.
Oeler & Menelaides, Inc., 12777 Jones Rd., Suite 175-18, Houston, TX 77070. Tel: (713) 894-5021.
Oeler & Menelaides, Inc., 8705 Shoal Creek Rd., Suite 218, Austin, TX 78758. Tel: (512) 453-0275 Fax: (512) 453-0088.

WASHINGTON **Core II,** 2535 152nd N.E. Suite A, Redmond, WA 98052. Tel: (206) 746-1799 (Home).
Crown Electronic Sales, Inc., 14400 Bel-Red Rd., 108, Bellevue, WA 98007. Tel: (206) 643-8100 Fax: 206-747-6861.

WISCONSIN **Micro Sales, Inc.,** N8 W12920 Leon Road, Suite 115, Menomonee Falls, WI 53051. Tel: (414) 251-0151.

CANADA EASTERN **Gidden-Morton Assoc.Inc.,**7050 Bramalea Road, Suite 27A, Mississauga, Ontario L5S 1T1. Tel: (416) 671-8111 Fax: (416) 671-2422.
Gidden-Morton Assoc.Inc.,3860 Cote-Vertu, Suite 221, St. Larent, Quebec H4R 1N4. Tel: (514) 335-9572 Fax: 514-335-9573.
Gidden-Morton Assoc.Inc.,301 Moodie Drive, Suite 101, Nepean, Ontario K2H 9C4. Tel: (613) 726-0844 Fax: 613-726-0953.

CANADA WESTERN **Dynasty Components, Inc.,** 12618 55A Avenue, Surrey, British Columbia V3W 1C3. Tel: (604) 597-0068 Fax: (604) 597-0043.

American design centres

ARIZONA **CaDel,** 715 N. Constitution Drive, Dueson, AZ 85748. Tel: (602) 296-8591.

CALIFORNIA **Analog Solutions,** 532 Fourth Street, Encinitas, CA 92024. Tel: (619) 944-1657.

Silicon Development Corp., 16162 Beach Boulevard, Suite 304, Huntington Beach, CA 92647. Tel: (714) 847-1992.

CANADA **Ontario Centre for Microelectronics,** 1150 Morrison Drive, Suite 400, Ottawa, K2H 9B8. Tel: (613) 596-6690.

Alberta Microelectronics Center, Suite 200, 1620-29 St., N.W., Calgary, Alberta T2N 4L7. Tel: (403) 289-2043.

COLORADO **Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.

FLORIDA **Silicon Beach Enterprises, Inc.,** 700 U.S. Highway One, Suite C, North Palm Beach, FL 33408. Tel: (305) 844-7805.

ILLINOIS **Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Road, Arlington Heights, IL 60005. Tel: (312) 956-0710.

MARYLAND **MicroCom Design, Inc.,** 9696 Deere Co. Road, Timonium, MD 21093.Tel: (301) 561-4811.

MASSACHUSETTS **Custom Silicon, Inc.,** 600 Suffolk Road, Lowell, MA 01854. Tel: (617) 454-4600.

North American distributors

ALABAMA **Pioneer/Technologies,** 4825 University Square, Huntsville, AL 35805. Tel: (205) 837-9300 Twx: 810-726-2197.

Hammond, 4411 B Evangel Circle. Huntsville, AL 35816. Tel: (205) 830-4764. Fax: (205) 830-4287.

ARIZONA **Insight Electronics,** 1525 W. University Dr., Suite 105, Tempe, AZ 85282. Tel: (602) 829-1800 Twx: 510-601-1618 Fax: (602) 967-2658.

Wyle-Phoenix, 17855 No. Black Canyon Hwy., Phoenix, AZ 85023. Tel: (602) 866-2888 Fax: 602-866-6937.

CALIFORNIA **Cypress Electronics (Corp.),** 2175 Martin Ave., Santa Clara. CA 95050. Tel: (408) 980 2500 Fax: (408) 986-9584.

Cypress Electronics, 6230 Descanso Ave., Buena Park, CA 90620. Tel: (714) 521-5230 Tlx: 5215716 Fax: (714) 521-5716.

Insight Electronics (Corp.), 6885 Flanders Dr., Unit G, San Diego, CA 92121. Tel: (619) 587-0471 Twx: 183035 Fax: (619) 587-1380.

Insight Electronics, 28035 Dorothy Dr., Suite 220, Agoura CA 91301. Tel: (818) 707-2100 Fax: (818) 707-0321.

Insight Electronics, 3505 Cadillac Ave., Unit E-1, Costa Mesa CA 92626. Tel: (714) 556-6890 Twx: 62354990 Fax: (714) 556-6897.

Pacesetter Electronics, 5417 E. La Palma Avenue, Anaheim, CA 92807. Tel: (714) 779-5855.

Wyle-Santa Clara, 3000 Bowers Av., Santa Clara, CA 95051. Tel: (408) 727-2500 Twx: 910-338-0296 Fax: 408-727-5896.

Wyle-Sacramento, 11151 Sun Center Drive, Rancho Cordova, CA 95670. Tel: (916) 638-5282 Fax: 916-638-1491.

Wyle-Irvine, 17872 Cowan Ave., Irvine, CA. Tel: (714) 863-9953 Twx: 3719599 Fax: (714) 863-0473.

Wyle-L.A./San Fernando, 26677 West Agoura Rd., Calabasas, CA 91302. Tel: (818) 880-9000 Twx: 3103720232 Fax: 818-880-5510.

Wyle-San Diego, 9525 Chesapeake Dr., San Diego, CA 92123. Tel: (619) 565-9171 Fax: 619-565-0512.

NORTH CAROLINA **Hammond,** 2923 Pacific Ave., Greensboro, NC 27406. Tel: (919) 275-6391 Tlx: 62894645 Fax: (919) 275-6391.

Pioneer/Technologies, 9801A South Pine Blvd., Charlotte, NC 28210. Tel: (704) 527-8188 Twx: 810-621-0366.

COLORADO **Cypress Electronics,** 12441 West 49th Ave., Wheatridge, CO 80033. Tel: (303) 431-2622 Fax: (303) 431-7191.

Wyle-Denver, 451 East 124th St., Thornton, CO 80241. Tel: (303) 457-9953 Twx: 9109360770 Fax: 303-457-4831.

CONNECTICUT **Jaco Electronics,** 384 Pratt Street, Meriden, CT 06450. Tel: (203) 235-1422.

Pioneer/Standard, 112 Main Street, Norwalk, CT 06851. Tel: (203) 853-1515 Twx: 710 468 3373.

FLORIDA **All American,** 16251 NW 54th Avenue, Miami, FL33014. Tel: (305) 621-3282.

Hammond (Corp.), 6600 N.W. 21st Ave., Ft. Lauderdale, FL 33309. Tel: (305) 973-7103 Twx: (510) 956-9401.

Hammond, 1230 West Central Blvd., Orlando, FL 32802. Tel: (305) 849-6060 Twx: 810-850-4121 Fax: (305) 648-8584.

Pioneer/Technologies, 674 South Military Trail, Deerfield Beach, FL 33442. Tel: (305) 428-8877 Twx: 510-955-9653.

Pioneer/Technologies, 337 South Northlake Blvd., Suite 1000, Altamonte Springs, FL 32701. Tel: (305) 834-9090 Twx: 810-853-0284.

GEORGIA **Hammond,** 5860 Oakbrook Pkwy, Suite 160, Norcross, GA 30093. Tel: (404) 449-1996 Fax: (404) 242-9834.
Pioneer/Technologies, 3100 F Northwoods Pl., Norcross, GA 30071. Tel: (404) 448-1711 Twx: 810-766-4515.

INDIANA **Pioneer/Standard,** 6408 Castleplace Dr., Indianapolis, IN 46250. Tel: (317) 849-7300 Twx: 810-260-1794.

ILLINOIS **Advent Electronics,** Rosamont, IL 60018. Tel: (312) 297-6200 Twx: 910 233 2477.
Pioneer/Standard, 2171 Executive Drive, Addison, ILL 60101. Tel: (312) 495-9680.

KANSAS **Pioneer,** 10551 Lackman Rd., Lenexa, KS 66215. Tel: (913) 492-0500 Twx: 510-601-6411.

MASSACHUSETTS **Emtel Electronics,** 375 Vanderbilt Ave., Norwood, MA 02062. Tel: (617) 769-9500 Fax: (617) 769-8329.
Jaco Electronics, 222 Andover Street, Wilmington, MA 01877. Tel: (617) 273-1860.
Pioneer/Standard, 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200 Twx: 710-326-6617.
Textrel Semi (Die only), 56 Middlesex Turnpike, Burlington, MA 01303. Tel: (617) 270-9246.

MARYLAND **Jaco Electronics,** Rivers Center, 10270 Old Columbia Road, Columbia, MD 21046 Tel: (301) 995-6620.
Pioneer/Tech. Group. Inc., 9100 Gaither Rd., Gaithersburg, MD 20877. Tel: (301) 921-0660 Twx: 710-828-0545 Fax: (301) 921-4255.

MICHIGAN **Pioneer/Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800 Twx: 810-242-3271.
Pioneer, 4505 Broadmoore Ave., S.E., Grand Rapids, MI 49508. Tel: (616) 698-1800 Twx: 510-600-8456.

MINNEAPOLIS **Cypress Electronics,** 7650 Executive Drive, Eden Prairie, MN 55334. Tel: (612) 934-2104 Fax: (612) 934 2057.
Industrial Components, Inc., Minneapolis, MN 55435. Tel: (612) 831-2666 Twx: 910 576 3153.
Pioneer/Standard, 10203 Bren Road East, Minnetonka, MN 55343. Tel: (612) 944-3355 Twx: 910-576-2738.

NEW JERSEY **Jaco Electronics,** 555 Preakness Road, Tontoa, NJ 07512. Tel: (201) 942-4000.
Pioneer/Standard, 45 Rte. 46 Pinebrook, NJ 07058. Tel: (201) 575-3510 Twx: 710-734-4382.
General Components, Inc., 245 D Clifton Ave., W. Berlin, NJ 08091. Tel: (609) 768-6767 Twx: 920-333-3057.

NEW YORK **Add Electronics,** 7 Adler Drive, E. Syracuse, NY 13057. Tel: (315) 437-1835.
Jaco Electronics, Hauppauge, NY 11787. Tel: (516) 273-5500 Twx: 510-227-6232 Fax: (516) 273-5799.
Mast, 95 Oser Ave., Hauppauge, NJ 11788. Tel: (516) 273-4422 Twx: 4974384.
Pioneer/Standard, 68 Corporate Drive. Binghamton, NY 13904. Tel: (607) 722-9300 Twx: 510-252-0893.
Pioneer/Standard, 60 Crossways Park West, Woodbury, NY 11797. Tel: (516) 921-8700 Twx: 510-221-2184 Fax: (516) 921-2143.
Pioneer/Standard, 840 Fairport Park, Fairport Park, NY 14450. Tel: (716) 381-7070 Twx: 510-253-7001.

OHIO **Pioneer/Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600 Twx: 810-421-0011 Fax: (216) 587-3906.
Pioneer, 4433 Interpoint Bl., Dayton, OH 45424. Tel: (513) 236-9900 Twx: 810 459 1622.

OREGON **Cypress Electronics,** 15075 S.W. Coll Parkway, Suite D, Beaverton, OR 97006. Tel: (503) 641-2233 Fax: (503) 643-1237.
Wyle-Portland, 5250 N.E. Elam Young Pkwy., Suite 600, Portland, OR 97123. Tel: (503) 640-6000 Fax: 503-640-5846.

PENNSYLVANIA **Advacom Electronics,** 5620 West Road, McKean, PA 16426. Tel: (814) 476-7774.
Pioneer/Technologies, 261 Gibraltar Rd., Horsham, PA 19044. Tel: (215) 674-4000 Twx: 510-665-6778.
Pioneer/Standard, 259 Kappa Drive, Pittsburg, PA 15238. Tel: (412) 782-2300 Twx: 710-795-3122.

TEXAS **Pioneer/Standard,** 9901 Burnet Road, Austin, TX 78758. Tel: (512) 835-4000 Twx: 910-874-1323.
Pioneer/Standard, 13710 Omega Road, Dallas, TX 75244. Tel: (214) 386-7300 Twx: 910-860-5563 Fax: (214) 490-6419.
Pioneer/Standard, 5853 Point West Drive, Houston, TX 77056. Tel: (713) 988-5555 Twx: 910-881-1606 Fax: (713) 988-1732.
Wyle-Dallas, 1810 North Greenville Ave., Richardson, TX 75083. Tel: (214) 235-9953 Fax: 214-644-5064.
Wyle-Houston, 11001 So. Hilcrest, Suite 100, Houston, TX 77099. Tel: (713) 879-9953 Fax: 713-879-6540.
Wyle-Austin, 2120 F West Braker Lane, Austin, TX 78758. Tel: (512) 834-9957 Fax: 512-834-0981.

UTAH **Wyle-Salt Lake City,** 1325 West 2200 South, Suite E, West Valley, Utah 84119. Tel: (801) 974-9953 Fax: 801-972-2524.

WASHINGTON **Cypress Electronics,** 22125 17th Ave., S.E., Suite 114, Bothell, WA 98021. Tel: (206) 483-1144 Fax: (206) 485-1512.

	Wyle-Seattle, 15385 N.E. 90th Street, Redmond, WA 98052. Tel: (206) 881-1150 Twx: 3103724260 Fax: (206) 881-1567.
CANADA EASTERN	**Carsten Electronics,** 3791 Victoria Park Avenue, Scarborough, Ontario, M1K3K6. Tel: (416) 495-7705.
	Semad, 243 Place Frontenac, Pointe Claire, P.Q. N9R 4Z7. Tel: (514) 694-0860 Twx: 05821861 Fax: (514) 694-0965.
	Semad, 1827 Woodward Dr., Suite 303, Ottawa, Ontario K2C 0R3. Tel: (613) 727-8325 Twx: 0533943 Fax: (613) 727 9489.
CANADA WESTERN	**Semad,** 75 Glendeer Dr., SE., Suite 210, Calgary, Alberta T2H 2S8. Tel: (403) 252-5664 Twx: 03824775.
	Semad, 3700 Gilmore, Suite 210, Burnaby, BC V5G 4M1. Tel: (604) 438-2515 Twx: 04356625.
	Semad, 85 Spy Court, Markham, Ontario, L3R 4Z4. Tel: (416) 475-3922 Twx: 06966600. Fax: (416) 475 4158.

Primary semi-custom design centres

AUSTRALIA	**Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.
BENELUX	**Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.
FRANCE	**Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.
ITALY	**Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.
WEST GERMANY	**Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.
TAIWAN	**Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan. Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.
UNITED KINGDOM	**Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW. United Kingdom Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext: 2198.
	Plessey Semiconductors Ltd., Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.
UNITED STATES OF AMERICA	**Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

Our world-wide distribution network is continually being updated; please check with your local Plessey Sales office for latest information.

Publication No. P.S.2020 October 1988


PLESSEY
Plessey Semiconductors